

- **Organization:**
  - TM2TR64EPH . . . 2 097 152 x 64 Bits
  - TM4TR64EPH . . . 4 194 304 x 64 Bits
  - TM2TR72EPH . . . 2 097 152 x 72 Bits
  - TM4TR72EPH . . . 4 194 304 x 72 Bits
- **Single 3.3-V Power Supply ( $\pm 10\%$  Tolerance)**
- **Designed for 100-MHz 4-Clock Systems**
- **TM2TR64EPH — Uses Eight 16M-Bit Synchronous Dynamic RAMs (SDRAMs) ( $2M \times 8$ -Bit) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM4TR64EPH — Uses Sixteen 16M-Bit SDRAMs ( $2M \times 8$ -Bit) in Plastic TSOPs**
- **TM2TR72EPH — Uses Nine 16M-Bit SDRAMs ( $2M \times 8$ -Bit) in Plastic TSOPs**
- **TM4TR72EPH — Uses Eighteen 16M-Bit SDRAMs ( $2M \times 8$ -Bit) in Plastic TSOPs**
- **Byte-Read/Write Capability**
- **Performance Ranges:**
  - **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
  - **High-Speed, Low-Noise, Low-Voltage TTL (LVTTTL) Interface**
  - **Read Latencies 2 and 3 Supported**
  - **Support Burst-Interleave and Burst-Interrupt Operations**
  - **Burst Length Programmable to 1, 2, 4, and 8**
  - **Two Banks for On-Chip Interleaving (Gapless Access)**
  - **Ambient Temperature Range 0°C to 70°C**
  - **Gold-Plated Contacts**
  - **Pipeline Architecture**
  - **Serial Presence Detect (SPD) Using EEPROM**

|              | SYNCHRONOUS<br>CLOCK CYCLE<br>TIME |                       | ACCESS TIME<br>CLOCK TO<br>OUTPUT |                       | REFRESH<br>INTERVAL |
|--------------|------------------------------------|-----------------------|-----------------------------------|-----------------------|---------------------|
|              | $t_{CK3}$<br>(CL = 3) <sup>†</sup> | $t_{CK2}$<br>(CL = 2) | $t_{AC3}$<br>(CL = 3)             | $t_{AC2}$<br>(CL = 2) |                     |
| 'xTRxxEPH-8  | 8 ns                               | 10 ns                 | 6 ns                              | 6 ns                  | 64 ms               |
| 'xTRxxEPH-8A | 8 ns                               | 15 ns                 | 6 ns                              | 7.5 ns                | 64 ms               |

<sup>†</sup> CL = CAS latency

## description

The TM2TR64EPH is a 16M-byte, 168-pin DIMM. The DIMM is composed of eight TMS626812BDGE 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS626812B data sheet (literature number SMOS693).

The TM4TR64EPH is a 32M-byte, 168-pin DIMM. The DIMM is composed of sixteen TMS626812BDGE 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors.

The TM2TR72EPH is an 16M-byte, 168-pin DIMM. The DIMM is composed of nine TMS626812BDGE 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors.

The TM4TR72EPH is a 32M-byte, 168-pin DIMM. The DIMM is composed of eighteen TMS626812BDGE 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
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# TM2TR64EPH, TM4TR64EPH TM2TR72EPH, TM4TR72EPH SYNCHRONOUS DYNAMIC RAM MODULES

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## operation

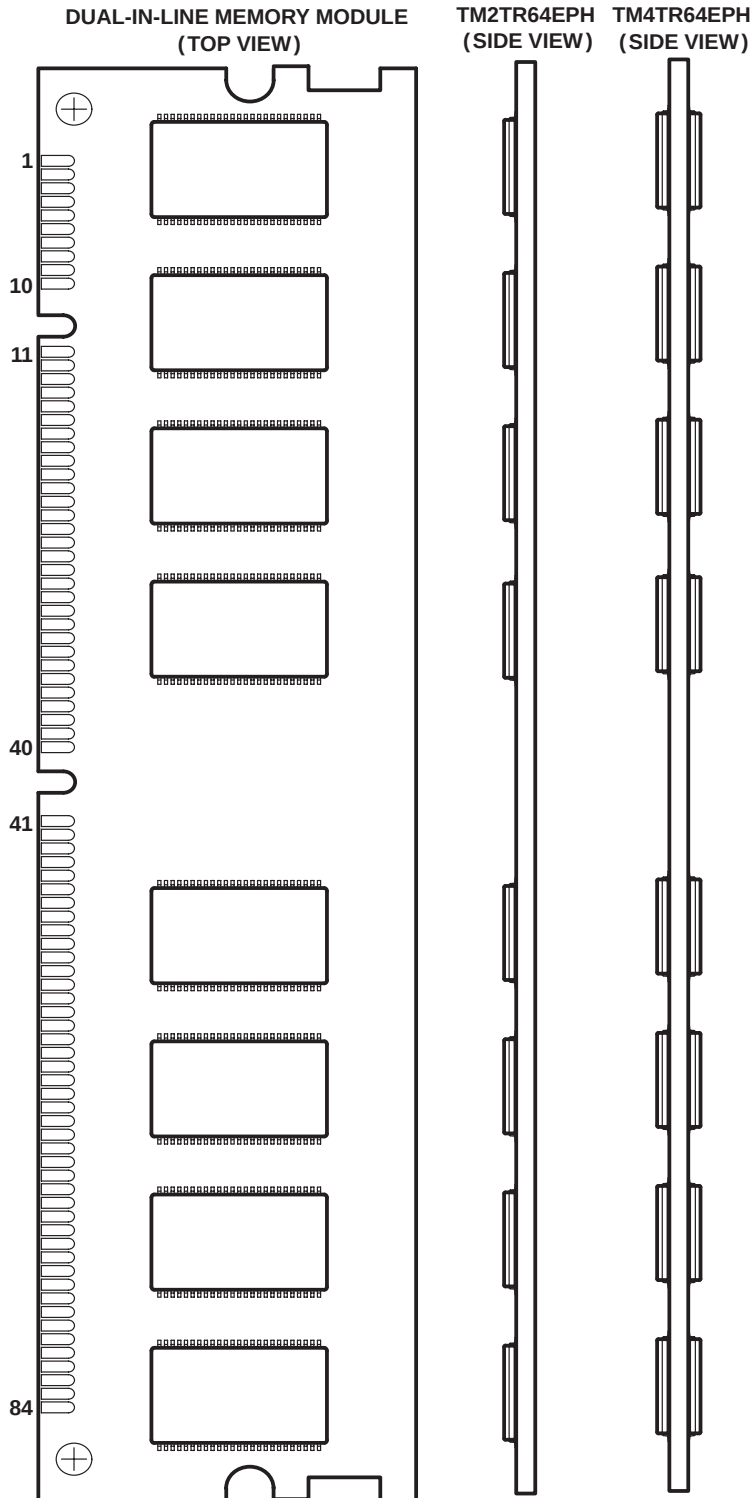
The TM2TR64EPH operates as eight TMS626812BDGE devices that are connected as shown in the TM2TR64EPH functional block diagram. The TM4TR64EPH operates as sixteen TMS626812BDGE devices connected as shown in the TM4TR64EPH functional block diagram.

The TM2TR72EPH operates as nine TMS626812BDGE devices that are connected as shown in the TM2TR72EPH functional block diagram. The TM4TR72EPH operates as eighteen TMS626812BDGE devices connected as shown in the TM4TR72EPH functional block diagram.



# TM2TR64EPH, TM4TR64EPH TM2TR72EPH, TM4TR72EPH SYNCHRONOUS DYNAMIC RAM MODULES

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## PIN NOMENCLATURE

|                         |                              |
|-------------------------|------------------------------|
| A[0:10]                 | Row-Address Inputs           |
| A[0:8]                  | Column-Address Inputs        |
| A11/BA0                 | Bank-Select Zero             |
| $\overline{\text{CAS}}$ | Column-Address Strobe        |
| CB[0:7]                 | Check Bit In/Check Bit Out   |
| CKE[0:1]                | Clock Enable                 |
| CK[0:3]                 | System Clock                 |
| DQ[0:63]                | Data-In/Data-Out             |
| DQMB[0:7]               | Data-In/Data-Out             |
|                         | Mask Enable                  |
| NC                      | No Connect                   |
| $\overline{\text{RAS}}$ | Row-Address Strobe           |
| S[0:3]                  | Chip-Select                  |
| SA[0:2]                 | Serial Presence Detect (SPD) |
|                         | Device Address Input         |
| SCL                     | SPD Clock                    |
| SDA                     | SPD Address/Data             |
| V <sub>DD</sub>         | 3.3-V Supply                 |
| V <sub>SS</sub>         | Ground                       |
| WE                      | Write Enable                 |
| WP                      | SPD Write-Protect            |

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**Pin Assignments**

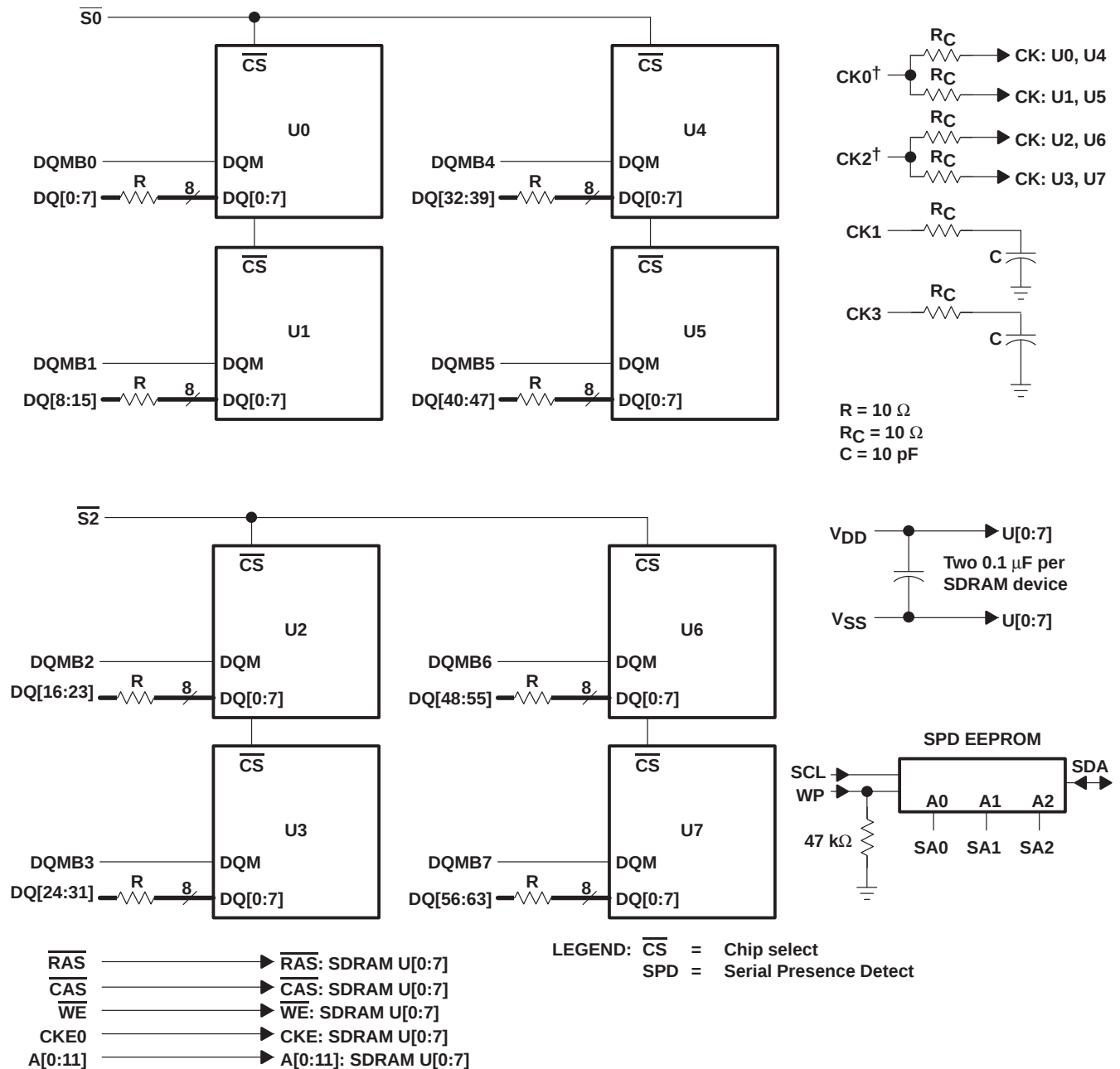
| NO. | PIN<br>NAME     | NO. | PIN<br>NAME     | NO. | PIN<br>NAME      | NO. | PIN<br>NAME     |
|-----|-----------------|-----|-----------------|-----|------------------|-----|-----------------|
| 1   | V <sub>SS</sub> | 43  | V <sub>SS</sub> | 85  | V <sub>SS</sub>  | 127 | V <sub>SS</sub> |
| 2   | DQ0             | 44  | NC              | 86  | DQ32             | 128 | CKE0            |
| 3   | DQ1             | 45  | $\overline{S2}$ | 87  | DQ33             | 129 | $\overline{S3}$ |
| 4   | DQ2             | 46  | DQMB2           | 88  | DQ34             | 130 | DQMB6           |
| 5   | DQ3             | 47  | DQMB3           | 89  | DQ35             | 131 | DQMB7           |
| 6   | V <sub>DD</sub> | 48  | NC              | 90  | V <sub>DD</sub>  | 132 | NC              |
| 7   | DQ4             | 49  | V <sub>DD</sub> | 91  | DQ36             | 133 | V <sub>DD</sub> |
| 8   | DQ5             | 50  | NC              | 92  | DQ37             | 134 | NC              |
| 9   | DQ6             | 51  | NC              | 93  | DQ38             | 135 | NC              |
| 10  | DQ7             | 52  | CB2             | 94  | DQ39             | 136 | CB6             |
| 11  | DQ8             | 53  | CB3             | 95  | DQ40             | 137 | CB7             |
| 12  | V <sub>SS</sub> | 54  | V <sub>SS</sub> | 96  | V <sub>SS</sub>  | 138 | V <sub>SS</sub> |
| 13  | DQ9             | 55  | DQ16            | 97  | DQ41             | 139 | DQ48            |
| 14  | DQ10            | 56  | DQ17            | 98  | DQ42             | 140 | DQ49            |
| 15  | DQ11            | 57  | DQ18            | 99  | DQ43             | 141 | DQ50            |
| 16  | DQ12            | 58  | DQ19            | 100 | DQ44             | 142 | DQ51            |
| 17  | DQ13            | 59  | V <sub>DD</sub> | 101 | DQ45             | 143 | V <sub>DD</sub> |
| 18  | V <sub>DD</sub> | 60  | DQ20            | 102 | V <sub>DD</sub>  | 144 | DQ52            |
| 19  | DQ14            | 61  | NC              | 103 | DQ46             | 145 | NC              |
| 20  | DQ15            | 62  | NC              | 104 | DQ47             | 146 | NC              |
| 21  | CB0             | 63  | CKE1            | 105 | CB4              | 147 | NC              |
| 22  | CB1             | 64  | V <sub>SS</sub> | 106 | CB5              | 148 | V <sub>SS</sub> |
| 23  | V <sub>SS</sub> | 65  | DQ21            | 107 | V <sub>SS</sub>  | 149 | DQ53            |
| 24  | NC              | 66  | DQ22            | 108 | NC               | 150 | DQ54            |
| 25  | NC              | 67  | DQ23            | 109 | NC               | 151 | DQ55            |
| 26  | V <sub>DD</sub> | 68  | V <sub>SS</sub> | 110 | V <sub>DD</sub>  | 152 | V <sub>SS</sub> |
| 27  | $\overline{WE}$ | 69  | DQ24            | 111 | $\overline{CAS}$ | 153 | DQ56            |
| 28  | DQMB0           | 70  | DQ25            | 112 | DQMB4            | 154 | DQ57            |
| 29  | DQMB1           | 71  | DQ26            | 113 | DQMB5            | 155 | DQ58            |
| 30  | $\overline{S0}$ | 72  | DQ27            | 114 | $\overline{S1}$  | 156 | DQ59            |
| 31  | NC              | 73  | V <sub>DD</sub> | 115 | $\overline{RAS}$ | 157 | V <sub>DD</sub> |
| 32  | V <sub>SS</sub> | 74  | DQ28            | 116 | V <sub>SS</sub>  | 158 | DQ60            |
| 33  | A0              | 75  | DQ29            | 117 | A1               | 159 | DQ61            |
| 34  | A2              | 76  | DQ30            | 118 | A3               | 160 | DQ62            |
| 35  | A4              | 77  | DQ31            | 119 | A5               | 161 | DQ63            |
| 36  | A6              | 78  | V <sub>SS</sub> | 120 | A7               | 162 | V <sub>SS</sub> |
| 37  | A8              | 79  | CK2             | 121 | A9               | 163 | CK3             |
| 38  | A10             | 80  | NC              | 122 | A11/BA0          | 164 | NC              |
| 39  | NC              | 81  | WP              | 123 | NC               | 165 | SA0             |
| 40  | V <sub>DD</sub> | 82  | SDA             | 124 | V <sub>DD</sub>  | 166 | SA1             |
| 41  | V <sub>DD</sub> | 83  | SCL             | 125 | CK1              | 167 | SA2             |
| 42  | CK0             | 84  | V <sub>DD</sub> | 126 | NC               | 168 | V <sub>DD</sub> |



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- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

### TM2TR64EPH functional block diagram

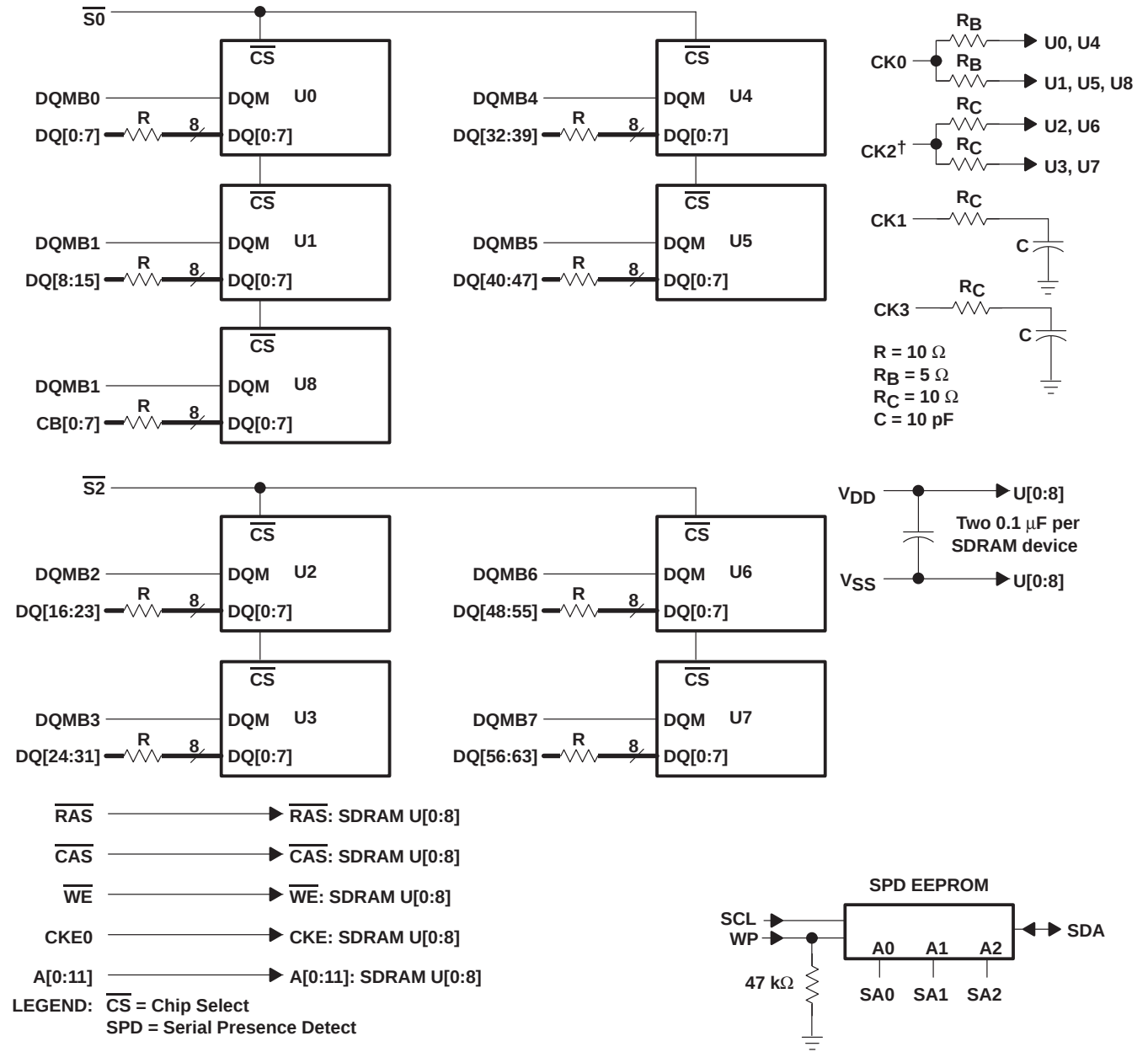


<sup>†</sup> Additional 3.3 pF capacity is used to balance loads among clocks.

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## TM2TR72EPH functional block diagram

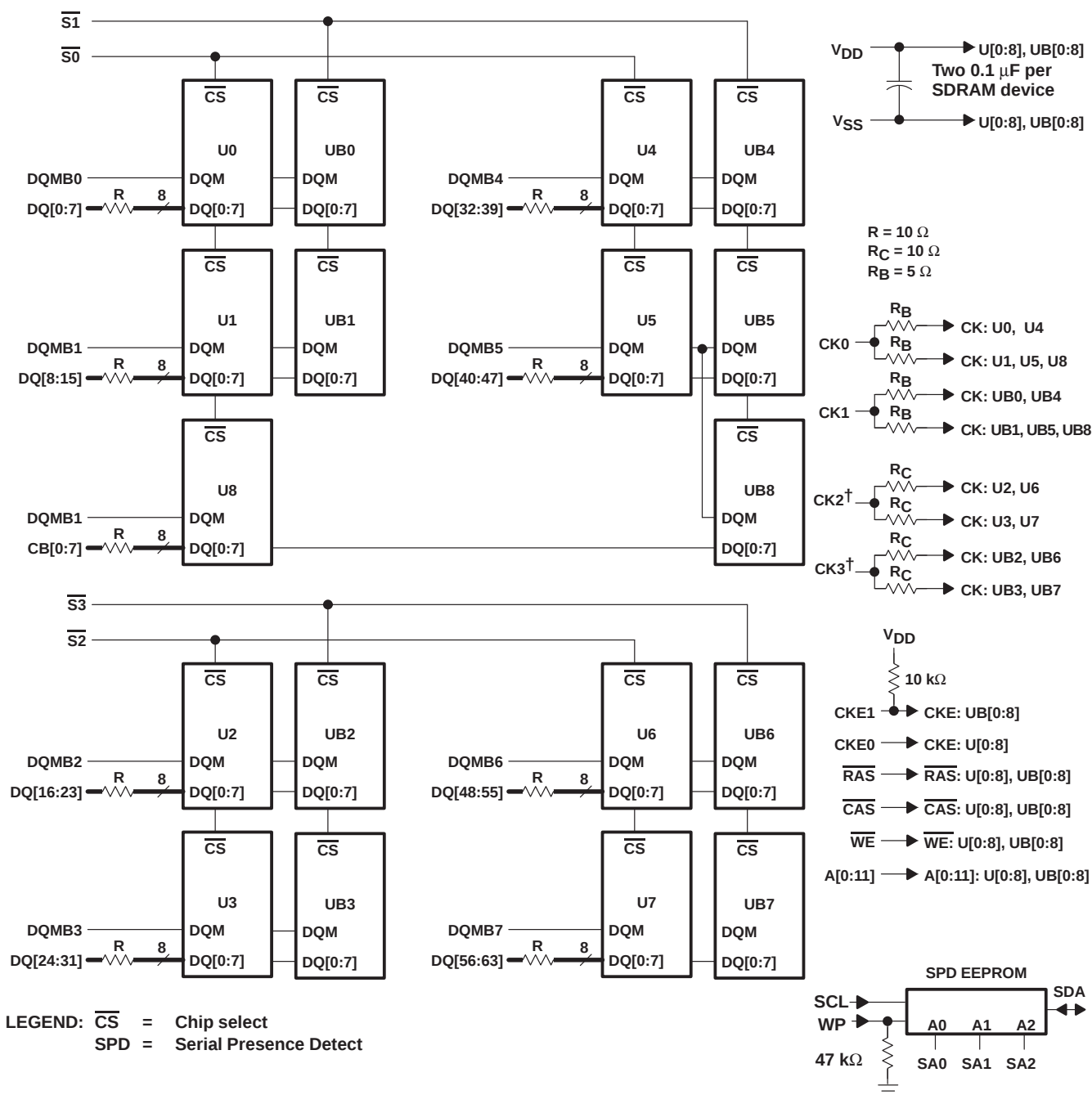


† Additional 3.3 pF capacity is used to balance loads among clocks.

# TM2TR64EPH, TM4TR64EPH TM2TR72EPH, TM4TR72EPH SYNCHRONOUS DYNAMIC RAM MODULES

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## TM4TR72EPH functional block diagram



$^\dagger$  Additional 3.3 pF capacity is used to balance loads among clocks.

**absolute maximum ratings over operating ambient temperature range (unless otherwise noted)<sup>†</sup>**

|                                            |                  |
|--------------------------------------------|------------------|
| Supply voltage range, $V_{DD}$             | –0.5 V to 4.6 V  |
| Voltage range on any pin (see Note 1)      | – 0.5 V to 4.6 V |
| Short-circuit output current               | 50 mA            |
| Power dissipation: TM2TR64EPH              | 8 W              |
| TM4TR64EPH                                 | 16 W             |
| TM2TR72EPH                                 | 9 W              |
| TM4TR72EPH                                 | 18 W             |
| Operating ambient temperature range, $T_A$ | 0°C to 70°C      |
| Storage temperature range, $T_{stg}$       | – 55°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

**recommended operating conditions<sup>‡</sup>**

|                                                          | MIN                | NOM | MAX            | UNIT |
|----------------------------------------------------------|--------------------|-----|----------------|------|
| $V_{DD}$ Supply voltage                                  | 3                  | 3.3 | 3.6            | V    |
| $V_{SS}$ Supply voltage                                  |                    | 0   |                | V    |
| $V_{IH}$ High-level input voltage                        | 2                  |     | $V_{DD} + 0.3$ | V    |
| $V_{IH-SPD}$ High-level input voltage for the SPD device | $0.7 \cdot V_{DD}$ |     | $V_{DD} + 0.5$ | V    |
| $V_{IL}$ Low-level input voltage                         | –0.3               |     | 0.8            | V    |
| $T_A$ Operating ambient temperature                      | 0                  |     | 70             | °C   |

<sup>‡</sup> The overshoot and undershoot voltage duration is less than or equal to 3 ns with no input clamp diode.

**capacitance over recommended ranges of supply voltage and ambient temperature,  $f = 1$  MHz (see Note 2)<sup>§</sup>**

| PARAMETER                                                                                                              | TMxTRxxEPH |     | UNIT |
|------------------------------------------------------------------------------------------------------------------------|------------|-----|------|
|                                                                                                                        | MIN        | MAX |      |
| $C_i(CK)$ Input capacitance, CK input                                                                                  | 2.5        | 4   | pF   |
| $C_i(AC)$ Input capacitance, address and control inputs: A0–A11, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ | 2.5        | 5   | pF   |
| $C_i(CKE)$ Input capacitance, CKE input                                                                                |            | 5   | pF   |
| $C_o$ Output capacitance                                                                                               | 4          | 6.5 | pF   |
| $C_i(DQMBx)$ Input capacitance, DQMBx input                                                                            | 2.5        | 5   | pF   |
| $C_i(Sx)$ Input capacitance, Sx input                                                                                  | 2.5        | 5   | pF   |
| $C_{i/o}(SDA)$ Input/output capacitance, SDA input                                                                     |            | 9   | pF   |
| $C_i(SPD)$ Input capacitance, SA0, SA1, SA2, SCL inputs                                                                |            | 7   | pF   |

<sup>§</sup> Specifications in this table represent a single SDRAM device.

NOTE 2:  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ . Bias on pins under test is 0 V.

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**electrical characteristics over recommended ranges of supply voltage and operating ambient temperature (unless otherwise noted) (see Note 3)<sup>†</sup>**

| PARAMETER          |                                                     | TEST CONDITIONS                                                                                                                                         | 'xTRxxEPH-8     |     | 'xTRxxEPH-8A |     | UNIT |
|--------------------|-----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|--------------|-----|------|
|                    |                                                     |                                                                                                                                                         | MIN             | MAX | MIN          | MAX |      |
| V <sub>OH</sub>    | High-level output voltage                           | I <sub>OH</sub> = − 4 mA                                                                                                                                | 2.4             |     | 2.4          |     | V    |
| V <sub>OL</sub>    | Low-level output voltage                            | I <sub>OL</sub> = 4 mA                                                                                                                                  | 0.4             |     | 0.4          |     | V    |
| I <sub>I</sub>     | Input current (leakage)                             | 0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub> + 0.3 V,<br>All other pins = 0 V to V <sub>DD</sub>                                                              | ± 10            |     | ± 10         |     | μA   |
| I <sub>O</sub>     | Output current (leakage)                            | 0 V ≤ V <sub>O</sub> ≤ V <sub>DD</sub> , Output disabled                                                                                                | ± 10            |     | ± 10         |     | μA   |
| I <sub>CC1</sub>   | Operating current                                   | Burst length = 1,<br>t <sub>RC</sub> ≥ t <sub>RC</sub> MIN<br>I <sub>OH</sub> /I <sub>OL</sub> = 0 mA, one bank<br>activated<br>(see Notes 3, 4, and 5) | CAS latency = 2 |     | 95           |     | mA   |
|                    |                                                     | CAS latency = 3                                                                                                                                         |                 | 100 |              |     |      |
| I <sub>CC2P</sub>  | Precharge standby current in<br>power-down mode     | CKE ≤ V <sub>IL</sub> MAX, t <sub>CK</sub> = 15 ns (see Note 6)                                                                                         | 1               |     | 1            |     | mA   |
| I <sub>CC2PS</sub> |                                                     | CKE and CK ≤ V <sub>IL</sub> MAX, t <sub>CK</sub> = ∞ (see Note 7)                                                                                      | 1               |     | 1            |     |      |
| I <sub>CC2N</sub>  | Precharge standby current in<br>non-power-down mode | CKE ≥ V <sub>IH</sub> MIN, t <sub>CK</sub> = 15 ns (see Note 6)                                                                                         | 30              |     | 30           |     | mA   |
| I <sub>CC2NS</sub> |                                                     | CKE ≥ V <sub>IH</sub> MIN, CK ≤ V <sub>IL</sub> MAX, t <sub>CK</sub> = ∞<br>(see Note 7)                                                                | 2               |     | 2            |     |      |
| I <sub>CC3P</sub>  | Active standby current in<br>power-down mode        | CKE ≤ V <sub>IL</sub> MAX, t <sub>CK</sub> = 15 ns (see Notes 3 and 6)                                                                                  | 3               |     | 3            |     | mA   |
| I <sub>CC3PS</sub> |                                                     | CKE and CK ≤ V <sub>IL</sub> MAX, t <sub>CK</sub> = ∞<br>(see Notes 3 and 7)                                                                            | 3               |     | 3            |     |      |
| I <sub>CC3N</sub>  | Active standby current in<br>non-power-down mode    | CKE ≥ V <sub>IH</sub> MIN, t <sub>CK</sub> = 15 ns (see Notes 3 and 6)                                                                                  | 40              |     | 40           |     | mA   |
| I <sub>CC3NS</sub> |                                                     | CKE ≥ V <sub>IH</sub> MIN, CK ≤ V <sub>IL</sub> MAX, t <sub>CK</sub> = ∞<br>(see Notes 3 and 7)                                                         | 10              |     | 10           |     |      |
| I <sub>CC4</sub>   | Burst current                                       | Page burst, I <sub>OH</sub> /I <sub>OL</sub> = 0 mA<br>All banks activated,<br>n <sub>CCD</sub> = one cycle<br>(see Notes 8 and 9)                      | CAS latency = 2 |     | 140          |     | mA   |
|                    |                                                     | CAS latency = 3                                                                                                                                         |                 | 150 |              |     |      |
| I <sub>CC5</sub>   | Auto-refresh current                                | t <sub>RC</sub> ≤ t <sub>RC</sub> MIN (see Note 7)                                                                                                      | CAS latency = 2 |     | 90           |     | mA   |
|                    |                                                     |                                                                                                                                                         | CAS latency = 3 |     | 95           |     |      |
| I <sub>CC6</sub>   | Self-refresh current                                | CKE ≤ V <sub>IL</sub> MAX                                                                                                                               | 0.4             |     | 0.4          |     | mA   |

<sup>†</sup> Specifications in this table represent a single SDRAM device.

NOTES: 3. Only one bank is activated.

4. t<sub>RC</sub> = MIN

5. Control, DQ, and address inputs change state only twice during t<sub>RC</sub>.

6. Control, DQ, and address inputs change state only once every 30 ns.

7. Control, DQ, and address inputs do not change state (stable).

8. Control, DQ, and address inputs change state only once every cycle.

9. Continuous burst access, n<sub>CCD</sub> = 1 cycle.

**ac timing requirements†‡§**

|                                                                                                   | 'xTRxxEPH-8                                  |         | 'xTRxxEPH-8A |         | UNIT  |
|---------------------------------------------------------------------------------------------------|----------------------------------------------|---------|--------------|---------|-------|
|                                                                                                   | MIN                                          | MAX     | MIN          | MAX     |       |
| t <sub>CK2</sub> Cycle time, CLK, CAS latency = 2                                                 | 10                                           |         | 15           |         | ns    |
| t <sub>CK3</sub> Cycle time, CLK, CAS latency = 3                                                 | 8                                            |         | 8            |         | ns    |
| t <sub>CH</sub> Pulse duration, CLK high                                                          | 3                                            |         | 3            |         | ns    |
| t <sub>CL</sub> Pulse duration, CLK low                                                           | 3                                            |         | 3            |         | ns    |
| t <sub>AC2</sub> Access time, CLK high to data out, CAS latency = 2 (see Note 10)                 |                                              | 6       |              | 7.5     | ns    |
| t <sub>AC3</sub> Access time, CLK high to data out, CAS latency = 3 (see Note 10)                 |                                              | 6       |              | 6       | ns    |
| t <sub>OH</sub> Hold time, CLK high to data out with 50-pF load                                   | 3                                            |         | 3            |         | ns    |
| t <sub>OHN</sub> Hold time, CLK high to data out with 0-pF load                                   | 2                                            |         | 2            |         | ns    |
| t <sub>LZ</sub> Delay time, CLK high to DQ in low-impedance state (see Note 11)                   | 1                                            |         | 1            |         | ns    |
| t <sub>HZ</sub> Delay time, CLK high to DQ in high-impedance state (see Note 12)                  |                                              | 8       |              | 8       | ns    |
| t <sub>IS</sub> Setup time, address, control, and data input                                      | 2                                            |         | 2            |         | ns    |
| t <sub>IH</sub> Hold time, address, control, and data input                                       | 1                                            |         | 1            |         | ns    |
| t <sub>CESP</sub> Power-down/self-refresh exit time                                               | 8                                            |         | 8            |         | ns    |
| t <sub>RAS</sub> Delay time, ACTV command to DEAC or DCAB command                                 | 48                                           | 100 000 | 48           | 100 000 | ns    |
| t <sub>RC</sub> Delay time, ACTV, REFR, or SLFR exit to ACTV, MRS, REFR, or SLFR command          | 68                                           |         | 68           |         | ns    |
| t <sub>RCD</sub> Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 13)    | 20                                           |         | 20           |         | ns    |
| t <sub>RP</sub> Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command              | 20                                           |         | 20           |         | ns    |
| t <sub>RRD</sub> Delay time, ACTV command in one bank to ACTV command in the other bank           | 16                                           |         | 16           |         | ns    |
| t <sub>RSA</sub> Delay time, MRS command to ACTV, MRS, REFR, or SLFR command                      | 16                                           |         | 16           |         | ns    |
| t <sub>APR</sub> Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command           | t <sub>RP</sub> – (CL – 1) * t <sub>CK</sub> |         |              |         | ns    |
| t <sub>APW</sub> Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command             | t <sub>RP</sub> + 1 t <sub>CK</sub>          |         |              |         | ns    |
| t <sub>T</sub> Transition time (see Note 14)                                                      | 1                                            | 5       | 1            | 5       | ns    |
| t <sub>REF</sub> Refresh interval                                                                 |                                              | 64      |              | 64      | ms    |
| n <sub>CCD</sub> Delay time, READ or WRT command to an interrupting command                       | 1                                            |         | 1            |         | cycle |
| n <sub>CDD</sub> Delay time, $\overline{\text{CS}}$ low or high to input enabled or disabled      | 0                                            | 0       | 0            | 0       | cycle |
| n <sub>CLE</sub> Delay time, CKE high or low to CLK enabled or disabled                           | 1                                            | 1       | 1            | 1       | cycle |
| n <sub>CWL</sub> Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P           | 1                                            |         | 1            |         | cycle |
| n <sub>DID</sub> Delay time, ENBL or MASK command to enabled or masked data in                    | 0                                            | 0       | 0            | 0       | cycle |
| n <sub>DOD</sub> Delay time, ENBL or MASK command to enabled or masked data out                   | 2                                            | 2       | 2            | 2       | cycle |
| n <sub>HZP2</sub> Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2 |                                              | 2       |              | 2       | cycle |
| n <sub>HZP3</sub> Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3 |                                              | 3       |              | 3       | cycle |
| n <sub>WCD</sub> Delay time, WRT command to first data in                                         | 0                                            | 0       | 0            | 0       | cycle |
| n <sub>WR</sub> Delay time, final data in of WRT operation to DEAC or DCAB command                | 1                                            |         | 1            |         | cycle |

† See Parameter Measurement Information for load circuits in the TMS626812B data sheet (literature number SMOS693).

‡ All references are made to the rising transition of CLK, unless otherwise noted.

§ Specifications in this table represent a single SDRAM device.

NOTES: 10. t<sub>AC</sub> is referenced from the rising transition of CLK that precedes the data-out cycle. For example, the first data-out t<sub>AC</sub> is referenced from the rising transition of CLK0 that is CAS latency minus one cycle after the READ command. Access time is measured at output reference level 1.4 V.

11. t<sub>LZ</sub> is measured from the rising transition of CLK that is CAS latency minus one cycle after the READ command.

12. t<sub>HZ</sub> MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.

13. For read or write operations with automatic deactivate, t<sub>RCD</sub> must be set to satisfy minimum t<sub>RAS</sub>.

14. Transition time, t<sub>T</sub>, is measured between V<sub>IH</sub> and V<sub>IL</sub>.

# TM2TR64EPH, TM4TR64EPH TM2TR72EPH, TM4TR72EPH SYNCHRONOUS DYNAMIC RAM MODULES

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## serial presence detect

The serial presence detect (SPD) is contained in a 256-byte serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see Table 1 – Table 4). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the Texas Instruments *Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

SPD contents of each TMxTRxxEPH device are listed in the following tables:

Table 1—TM2TR64EPH      Table 2—TM4TR64EPH  
Table 3—TM2TR72EPH      Table 4—TM4TR72EPH

**Table 1. Serial Presence Detect Data for the TM2TR64EPH**

| BYTE NO. | DESCRIPTION OF FUNCTION                                                        | TM2TR64EPH-8                                                              |      | TM2TR64EPH-8A                                                                                     |      |
|----------|--------------------------------------------------------------------------------|---------------------------------------------------------------------------|------|---------------------------------------------------------------------------------------------------|------|
|          |                                                                                | ITEM                                                                      | DATA | ITEM                                                                                              | DATA |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                                                                 | 80h  | 128 bytes                                                                                         | 80h  |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                                                                 | 08h  | 256 bytes                                                                                         | 08h  |
| 2        | Fundamental memory type (FPM, EDO, SDRAM, . . .)                               | SDRAM                                                                     | 04h  | SDRAM                                                                                             | 04h  |
| 3        | Number of row addresses on this assembly                                       | 11                                                                        | 0Bh  | 11                                                                                                | 0Bh  |
| 4        | Number of column addresses on this assembly                                    | 9                                                                         | 09h  | 9                                                                                                 | 09h  |
| 5        | Number of module rows on this assembly                                         | 1 bank                                                                    | 01h  | 1 bank                                                                                            | 01h  |
| 6        | Data width of this assembly                                                    | 64 bits                                                                   | 40h  | 64 bits                                                                                           | 40h  |
| 7        | Data width continuation                                                        |                                                                           | 00h  |                                                                                                   | 00h  |
| 8        | Voltage interface standard of this assembly                                    | LVTTL                                                                     | 01h  | LVTTL                                                                                             | 01h  |
| 9        | SDRAM cycle time at maximum supported CAS latency (CL), CL = X                 | t <sub>CK</sub> = 8 ns                                                    | 80h  | t <sub>CK</sub> = 8 ns                                                                            | 80h  |
| 10       | SDRAM access from clock at CL = X                                              | t <sub>AC</sub> = 6 ns                                                    | 60h  | t <sub>AC</sub> = 6 ns                                                                            | 60h  |
| 11       | DIMM configuration type (non-parity, parity, error correcting code [ECC])      | Non-Parity                                                                | 00h  | Non-Parity                                                                                        | 00h  |
| 12       | Refresh rate / type                                                            | 15.6 μs/<br>self-refresh                                                  | 80h  | 15.6 μs/<br>self-refresh                                                                          | 80h  |
| 13       | SDRAM width, primary DRAM                                                      | x8                                                                        | 08h  | x8                                                                                                | 08h  |
| 14       | Error-checking SDRAM data width                                                | N/A                                                                       | 00h  | N/A                                                                                               | 00h  |
| 15       | Minimum clock delay, back-to-back random column addresses                      | 1 CK cycle                                                                | 01h  | 1 CK cycle                                                                                        | 01h  |
| 16       | Burst lengths supported                                                        | 1, 2, 4, 8                                                                | 0Fh  | 1, 2, 4, 8                                                                                        | 0Fh  |
| 17       | Number of banks on each SDRAM device                                           | 2 banks                                                                   | 02h  | 2 banks                                                                                           | 02h  |
| 18       | CAS latencies supported                                                        | 2, 3                                                                      | 06h  | 2, 3                                                                                              | 06h  |
| 19       | CS latency                                                                     | 0                                                                         | 01h  | 0                                                                                                 | 01h  |
| 20       | Write latency                                                                  | 0                                                                         | 01h  | 0                                                                                                 | 01h  |
| 21       | SDRAM module attributes                                                        | Non-buffered/<br>Non-registered                                           | 00h  | Non-buffered/<br>Non-registered                                                                   | 00h  |
| 22       | SDRAM device attributes: general                                               | V <sub>DD</sub> tolerance =<br>(+10%)<br>precharge all,<br>auto precharge | 0Eh  | V <sub>DD</sub> tolerance =<br>(+10%),<br>Burst read / write,<br>precharge all,<br>auto precharge | 0Eh  |
| 23       | Minimum clock cycle time at CL = X – 1                                         | t <sub>CK</sub> = 10 ns                                                   | A0h  | t <sub>CK</sub> = 15 ns                                                                           | F0h  |



**serial presence detect (continued)**

**Table 1. Serial Presence Detect Data for the TM2TR64EPH (Continued)**

| BYTE NO. | DESCRIPTION OF FUNCTION                                            | TM2TR64EPH-8             |            | TM2TR64EPH-8A            |            |
|----------|--------------------------------------------------------------------|--------------------------|------------|--------------------------|------------|
|          |                                                                    | ITEM                     | DATA       | ITEM                     | DATA       |
| 24       | Maximum data-access time from clock at CL = X – 1                  | t <sub>AC</sub> = 6 ns   | 60h        | t <sub>AC</sub> = 7.5 ns | 75h        |
| 25       | Minimum clock cycle time at CL = X – 2                             | N/A                      | 00h        | N/A                      | 00h        |
| 26       | Maximum data-access time from clock at CL = X – 2                  | N/A                      | 00h        | N/A                      | 00h        |
| 27       | Minimum row-precharge time                                         | t <sub>RP</sub> = 20 ns  | 14h        | t <sub>RP</sub> = 20 ns  | 14h        |
| 28       | Minimum row-active to row-active delay                             | t <sub>RRD</sub> = 16 ns | 10h        | t <sub>RRD</sub> = 16 ns | 10h        |
| 29       | Minimum $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ delay | t <sub>RCD</sub> = 20 ns | 14h        | t <sub>RCD</sub> = 20 ns | 14h        |
| 30       | Minimum $\overline{\text{RAS}}$ pulse width                        | t <sub>RAS</sub> = 48 ns | 30h        | t <sub>RAS</sub> = 48 ns | 30h        |
| 31       | Density of each bank on module                                     | 16M Bytes                | 04h        | 16M Bytes                | 04h        |
| 32       | Command and address signal input setup time                        | t <sub>IS</sub> = 2 ns   | 20h        | t <sub>IS</sub> = 2 ns   | 20h        |
| 33       | Command and address signal input hold time                         | t <sub>IH</sub> = 1 ns   | 10h        | t <sub>IH</sub> = 1 ns   | 10h        |
| 34       | Data signal input setup time                                       | t <sub>IS</sub> = 2 ns   | 20h        | t <sub>IS</sub> = 2 ns   | 20h        |
| 35       | Data signal input hold time                                        | t <sub>IH</sub> = 1 ns   | 10h        | t <sub>IH</sub> = 1 ns   | 10h        |
| 36–61    | Superset features (may be used in the future)                      |                          |            |                          |            |
| 62       | SPD revision                                                       | Rev. 1.2                 | 12h        | Rev. 1.2                 | 12h        |
| 63       | Checksum for byte 0–62                                             | 80                       | 50h        | 181                      | B5h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP – 106E                        | 97h                      | 9700...00h | 97h                      | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>                                | TBD                      |            | TBD                      |            |
| 73       | Manufacturer's part number                                         | T                        | 54h        | T                        | 54h        |
| 74       | Manufacturer's part number                                         | M                        | 4Dh        | M                        | 4Dh        |
| 75       | Manufacturer's part number                                         | 2                        | 32h        | 2                        | 32h        |
| 76       | Manufacturer's part number                                         | T                        | 54h        | T                        | 54h        |
| 77       | Manufacturer's part number                                         | R                        | 52h        | R                        | 52h        |
| 78       | Manufacturer's part number                                         | 6                        | 36h        | 6                        | 36h        |
| 79       | Manufacturer's part number                                         | 4                        | 34h        | 4                        | 34h        |
| 80       | Manufacturer's part number                                         | E                        | 45h        | E                        | 45h        |
| 81       | Manufacturer's part number                                         | P                        | 50h        | P                        | 50h        |
| 82       | Manufacturer's part number                                         | H                        | 4Eh        | H                        | 4Eh        |
| 83       | Manufacturer's part number                                         | –                        | 2Dh        | –                        | 2Dh        |
| 84       | Manufacturer's part number                                         | 8                        | 38h        | 8                        | 38h        |
| 85       | Manufacturer's part number                                         | SPACE                    | 20h        | A                        | 41h        |
| 86–90    | Manufacturer's part number                                         | SPACE                    | 20h        | SPACE                    | 20h        |
| 91       | Die revision code <sup>†</sup>                                     | TBD                      |            | TBD                      |            |
| 92       | PCB revision code <sup>†</sup>                                     | TBD                      |            | TBD                      |            |
| 93–94    | Manufacturing date <sup>†</sup>                                    | TBD                      |            | TBD                      |            |
| 95–98    | Assembly serial number <sup>†</sup>                                | TBD                      |            | TBD                      |            |
| 99–125   | Manufacturer-specific data <sup>†</sup>                            | TBD                      |            | TBD                      |            |
| 126      | Clock frequency                                                    | 100 MHz                  | 64h        | 100 MHz                  | 64h        |
| 127      | SDRAM component and clock interconnection details                  | 199                      | C7h        | 199                      | C7h        |
| 128–166  | System-integrator-specific data <sup>‡</sup>                       | TBD                      |            | TBD                      |            |
| 167–255  | Open                                                               |                          |            |                          |            |

<sup>†</sup> TBD indicates values that are determined at manufacturing time and are module-dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

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**serial presence detect (continued)**

**Table 2. Serial Presence Detect Data for the TM4TR64EPH**

| BYTE NO. | DESCRIPTION OF FUNCTION                                                        | TM4TR64EPH-8                                                                         |      | TM4TR64EPH-8A                                                                         |      |
|----------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|------|---------------------------------------------------------------------------------------|------|
|          |                                                                                | ITEM                                                                                 | DATA | ITEM                                                                                  | DATA |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                                                                            | 80h  | 128 bytes                                                                             | 80h  |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                                                                            | 08h  | 256 bytes                                                                             | 08h  |
| 2        | Fundamental memory type (FPM, EDO, SDRAM, . . .)                               | SDRAM                                                                                | 04h  | SDRAM                                                                                 | 04h  |
| 3        | Number of row addresses on this assembly                                       | 11                                                                                   | 0Bh  | 11                                                                                    | 0Bh  |
| 4        | Number of column addresses on this assembly                                    | 9                                                                                    | 09h  | 9                                                                                     | 09h  |
| 5        | Number of module rows on this assembly                                         | 2 banks                                                                              | 02h  | 2 banks                                                                               | 02h  |
| 6        | Data width of this assembly                                                    | 64 bits                                                                              | 40h  | 64 bits                                                                               | 40h  |
| 7        | Data width continuation                                                        |                                                                                      | 00h  |                                                                                       | 00h  |
| 8        | Voltage interface standard of this assembly                                    | LVTTTL                                                                               | 01h  | LVTTTL                                                                                | 01h  |
| 9        | SDRAM cycle time at maximum supported CAS latency (CL), CL = X                 | $t_{CK} = 8 \text{ ns}$                                                              | 80h  | $t_{CK} = 8 \text{ ns}$                                                               | 80h  |
| 10       | SDRAM access from clock at CL = X                                              | $t_{AC} = 6 \text{ ns}$                                                              | 60h  | $t_{AC} = 6 \text{ ns}$                                                               | 60h  |
| 11       | DIMM configuration type (non-parity, parity, error correcting code [ECC])      | Non-Parity                                                                           | 00h  | Non-Parity                                                                            | 00h  |
| 12       | Refresh rate/type                                                              | 15.6 $\mu\text{s}$ /self-refresh                                                     | 80h  | 15.6 $\mu\text{s}$ /self-refresh                                                      | 80h  |
| 13       | SDRAM width, primary DRAM                                                      | x8                                                                                   | 08h  | x8                                                                                    | 08h  |
| 14       | Error-checking SDRAM data width                                                | N/A                                                                                  | 00h  | N/A                                                                                   | 00h  |
| 15       | Minimum clock delay, back-to-back random column addresses                      | 1 CK cycle                                                                           | 01h  | 1 CK cycle                                                                            | 01h  |
| 16       | Burst lengths supported                                                        | 1, 2, 4, 8                                                                           | 0Fh  | 1, 2, 4, 8                                                                            | 0Fh  |
| 17       | Number of banks on each SDRAM device                                           | 2 banks                                                                              | 02h  | 2 banks                                                                               | 02h  |
| 18       | CAS latencies supported                                                        | 2, 3                                                                                 | 06h  | 2, 3                                                                                  | 06h  |
| 19       | CS latency                                                                     | 0                                                                                    | 01h  | 0                                                                                     | 01h  |
| 20       | Write latency                                                                  | 0                                                                                    | 01h  | 0                                                                                     | 01h  |
| 21       | SDRAM module attributes                                                        | Non-buffered/<br>Non-registered                                                      | 00h  | Non-buffered/<br>Non-registered                                                       | 00h  |
| 22       | SDRAM device attributes: general                                               | $V_{DD}$ tolerance = (+10%)<br>Burst read/write,<br>precharge all,<br>auto precharge | 0Eh  | $V_{DD}$ tolerance = (+10%),<br>Burst read/write,<br>precharge all,<br>auto precharge | 0Eh  |
| 23       | Minimum clock cycle time at CL = X – 1                                         | $t_{CK} = 10 \text{ ns}$                                                             | A0h  | $t_{CK} = 15 \text{ ns}$                                                              | F0h  |
| 24       | Maximum data-access time from clock at CL = X – 1                              | $t_{AC} = 6 \text{ ns}$                                                              | 60h  | $t_{AC} = 7.5 \text{ ns}$                                                             | 75h  |
| 25       | Minimum clock cycle time at CL = X – 2                                         | N/A                                                                                  | 00h  | N/A                                                                                   | 00h  |
| 26       | Maximum data-access time from clock at CL = X – 2                              | N/A                                                                                  | 00h  | N/A                                                                                   | 00h  |

**serial presence detect (continued)**

**Table 2. Serial Presence Detect Data for the TM4TR64EPH (Continued)**

| BYTE NO. | DESCRIPTION OF FUNCTION                                            | TM4TR64EPH-8              |            | TM4TR64EPH-8A             |            |
|----------|--------------------------------------------------------------------|---------------------------|------------|---------------------------|------------|
|          |                                                                    | ITEM                      | DATA       | ITEM                      | DATA       |
| 27       | Minimum row-precharge time                                         | $t_{RP} = 20 \text{ ns}$  | 14h        | $t_{RP} = 20 \text{ ns}$  | 14h        |
| 28       | Minimum row-active to row-active delay                             | $t_{RRD} = 16 \text{ ns}$ | 10h        | $t_{RRD} = 16 \text{ ns}$ | 10h        |
| 29       | Minimum $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ delay | $t_{RCD} = 20 \text{ ns}$ | 14h        | $t_{RCD} = 20 \text{ ns}$ | 14h        |
| 30       | Minimum $\overline{\text{RAS}}$ pulse width                        | $t_{RAS} = 48 \text{ ns}$ | 30h        | $t_{RAS} = 48 \text{ ns}$ | 30h        |
| 31       | Density of each bank on module                                     | 16M Bytes                 | 04h        | 16M Bytes                 | 04h        |
| 32       | Command and address signal input setup time                        | $t_{IS} = 2 \text{ ns}$   | 20h        | $t_{IS} = 2 \text{ ns}$   | 20h        |
| 33       | Command and address signal input hold time                         | $t_{IH} = 1 \text{ ns}$   | 10h        | $t_{IH} = 1 \text{ ns}$   | 10h        |
| 34       | Data signal input setup time                                       | $t_{IS} = 2 \text{ ns}$   | 20h        | $t_{IS} = 2 \text{ ns}$   | 20h        |
| 35       | Data signal input hold time                                        | $t_{IH} = 1 \text{ ns}$   | 10h        | $t_{IH} = 1 \text{ ns}$   | 10h        |
| 36–61    | Superset features (may be used in the future)                      |                           |            |                           |            |
| 62       | SPD revision                                                       | Rev. 1.2                  | 12h        | Rev. 1.2                  | 12h        |
| 63       | Checksum for byte 0–62                                             | 81                        | 51h        | 182                       | B6h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP–106E                          | 97h                       | 9700...00h | 97h                       | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>                                | TBD                       |            | TBD                       |            |
| 73       | Manufacturer's part number                                         | T                         | 54h        | T                         | 54h        |
| 74       | Manufacturer's part number                                         | M                         | 4Dh        | M                         | 4Dh        |
| 75       | Manufacturer's part number                                         | 4                         | 34h        | 4                         | 34h        |
| 76       | Manufacturer's part number                                         | T                         | 54h        | T                         | 54h        |
| 77       | Manufacturer's part number                                         | R                         | 52h        | R                         | 52h        |
| 78       | Manufacturer's part number                                         | 6                         | 36h        | 6                         | 36h        |
| 79       | Manufacturer's part number                                         | 4                         | 34h        | 4                         | 34h        |
| 80       | Manufacturer's part number                                         | E                         | 45h        | E                         | 45h        |
| 81       | Manufacturer's part number                                         | P                         | 50h        | P                         | 50h        |
| 82       | Manufacturer's part number                                         | H                         | 4Eh        | H                         | 4Eh        |
| 83       | Manufacturer's part number                                         | –                         | 2Dh        | –                         | 2Dh        |
| 84       | Manufacturer's part number                                         | 8                         | 38h        | 8                         | 38h        |
| 85       | Manufacturer's part number                                         | SPACE                     | 20h        | A                         | 41h        |
| 86–90    | Manufacturer's part number                                         | SPACE                     | 20h        | SPACE                     | 20h        |
| 91       | Die revision code <sup>†</sup>                                     | TBD                       |            | TBD                       |            |
| 92       | PCB revision code <sup>†</sup>                                     | TBD                       |            | TBD                       |            |
| 93–94    | Manufacturing date <sup>†</sup>                                    | TBD                       |            | TBD                       |            |
| 95–98    | Assembly serial number <sup>†</sup>                                | TBD                       |            | TBD                       |            |
| 99–125   | Manufacturer-specific data <sup>†</sup>                            | TBD                       |            | TBD                       |            |
| 126      | Clock frequency                                                    | 100 MHz                   | 64h        | 100 MHz                   | 64h        |
| 127      | SDRAM component and clock interconnection details                  | 247                       | F7h        | 247                       | F7h        |
| 128–166  | System-integrator-specific data <sup>‡</sup>                       | TBD                       |            | TBD                       |            |
| 167–255  | Open                                                               |                           |            |                           |            |

<sup>†</sup> TBD indicates values that are determined at manufacturing time and are module-dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

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**serial presence detect (continued)**

**Table 3. Serial Presence Detect Data for the TM2TR72EPH**

| BYTE NO. | DESCRIPTION OF FUNCTION                                                        | TM2TR72EPH-8                                                                         |      | TM2TR72EPH-8A                                                                         |      |
|----------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|------|---------------------------------------------------------------------------------------|------|
|          |                                                                                | ITEM                                                                                 | DATA | ITEM                                                                                  | DATA |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                                                                            | 80h  | 128 bytes                                                                             | 80h  |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                                                                            | 08h  | 256 bytes                                                                             | 08h  |
| 2        | Fundamental memory type (FPM, EDO, SDRAM, . . .)                               | SDRAM                                                                                | 04h  | SDRAM                                                                                 | 04h  |
| 3        | Number of row addresses on this assembly                                       | 11                                                                                   | 0Bh  | 11                                                                                    | 0Bh  |
| 4        | Number of column addresses on this assembly                                    | 9                                                                                    | 09h  | 9                                                                                     | 09h  |
| 5        | Number of module rows on this assembly                                         | 1 bank                                                                               | 01h  | 1 bank                                                                                | 01h  |
| 6        | Data width of this assembly                                                    | 72 bits                                                                              | 48h  | 72 bits                                                                               | 48h  |
| 7        | Data width continuation                                                        |                                                                                      | 00h  |                                                                                       | 00h  |
| 8        | Voltage interface standard of this assembly                                    | LVTTTL                                                                               | 01h  | LVTTTL                                                                                | 01h  |
| 9        | SDRAM cycle time at maximum supported CAS latency (CL), CL = X                 | $t_{CK} = 8 \text{ ns}$                                                              | 80h  | $t_{CK} = 8 \text{ ns}$                                                               | 80h  |
| 10       | SDRAM access from clock at CL = X                                              | $t_{AC} = 6 \text{ ns}$                                                              | 60h  | $t_{AC} = 6 \text{ ns}$                                                               | 60h  |
| 11       | DIMM configuration type (non-parity, parity, error correcting code [ECC])      | ECC                                                                                  | 02h  | ECC                                                                                   | 02h  |
| 12       | Refresh rate/type                                                              | 15.6 $\mu\text{s}$ /self-refresh                                                     | 80h  | 15.6 $\mu\text{s}$ /self-refresh                                                      | 80h  |
| 13       | SDRAM width, primary DRAM                                                      | x8                                                                                   | 08h  | x8                                                                                    | 08h  |
| 14       | Error-checking SDRAM data width                                                | x8                                                                                   | 08h  | x8                                                                                    | 08h  |
| 15       | Minimum clock delay, back-to-back random column addresses                      | 1 CK cycle                                                                           | 01h  | 1 CK cycle                                                                            | 01h  |
| 16       | Burst lengths supported                                                        | 1, 2, 4, 8                                                                           | 0Fh  | 1, 2, 4, 8                                                                            | 0Fh  |
| 17       | Number of banks on each SDRAM device                                           | 2 banks                                                                              | 02h  | 2 banks                                                                               | 02h  |
| 18       | CAS latencies supported                                                        | 2, 3                                                                                 | 06h  | 2, 3                                                                                  | 06h  |
| 19       | CS latency                                                                     | 0                                                                                    | 01h  | 0                                                                                     | 01h  |
| 20       | Write latency                                                                  | 0                                                                                    | 01h  | 0                                                                                     | 01h  |
| 21       | SDRAM module attributes                                                        | Non-buffered/<br>Non-registered                                                      | 00h  | Non-buffered/<br>Non-registered                                                       | 00h  |
| 22       | SDRAM device attributes: general                                               | $V_{DD}$ tolerance = (+10%)<br>Burst read/write,<br>precharge all,<br>auto precharge | 0Eh  | $V_{DD}$ tolerance = (+10%),<br>Burst read/write,<br>precharge all,<br>auto precharge | 0Eh  |
| 23       | Minimum clock cycle time at CL = X – 1                                         | $t_{CK} = 10 \text{ ns}$                                                             | A0h  | $t_{CK} = 15 \text{ ns}$                                                              | F0h  |
| 24       | Maximum data-access time from clock at CL = X – 1                              | $t_{AC} = 6.0 \text{ ns}$                                                            | 60h  | $t_{AC} = 7.5 \text{ ns}$                                                             | 75h  |

**serial presence detect (continued)**

**Table 3. Serial Presence Detect Data for the TM2TR72EPH (Continued)**

| BYTE NO. | DESCRIPTION OF FUNCTION                                            | TM2TR72EPH-8             |            | TM2TR72EPH-8A            |            |
|----------|--------------------------------------------------------------------|--------------------------|------------|--------------------------|------------|
|          |                                                                    | ITEM                     | DATA       | ITEM                     | DATA       |
| 25       | Minimum clock cycle time at CL = X – 2                             | N/A                      | 00h        | N/A                      | 00h        |
| 26       | Maximum data-access time from clock at CL = X – 2                  | N/A                      | 00h        | N/A                      | 00h        |
| 27       | Minimum row-precharge time                                         | t <sub>RP</sub> = 20 ns  | 14h        | t <sub>RP</sub> = 20 ns  | 14h        |
| 28       | Minimum row-active to row-active delay                             | t <sub>RRD</sub> = 16 ns | 10h        | t <sub>RRD</sub> = 16 ns | 10h        |
| 29       | Minimum $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ delay | t <sub>RCD</sub> = 20 ns | 14h        | t <sub>RCD</sub> = 20 ns | 14h        |
| 30       | Minimum $\overline{\text{RAS}}$ pulse width                        | t <sub>RAS</sub> = 48 ns | 30h        | t <sub>RAS</sub> = 48 ns | 30h        |
| 31       | Density of each bank on module                                     | 16M Bytes                | 04h        | 16M Bytes                | 04h        |
| 32       | Command and address signal input setup time                        | t <sub>IS</sub> = 2 ns   | 20h        | t <sub>IS</sub> = 2 ns   | 20h        |
| 33       | Command and address signal input hold time                         | t <sub>IH</sub> = 1 ns   | 10h        | t <sub>IH</sub> = 1 ns   | 10h        |
| 34       | Data signal input setup time                                       | t <sub>IS</sub> = 2 ns   | 20h        | t <sub>IS</sub> = 2 ns   | 20h        |
| 35       | Data signal input hold time                                        | t <sub>IH</sub> = 1 ns   | 10h        | t <sub>IH</sub> = 1 ns   | 10h        |
| 36–61    | Superset features (may be used in the future)                      |                          |            |                          |            |
| 62       | SPD revision                                                       | Rev. 1.2                 | 12h        | Rev. 1.2                 | 12h        |
| 63       | Checksum for byte 0–62                                             | 98                       | 62h        | 199                      | C7h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP – 106E                        | 97h                      | 9700...00h | 97h                      | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>                                | TBD                      |            | TBD                      |            |
| 73       | Manufacturer's part number                                         | T                        | 54h        | T                        | 54h        |
| 74       | Manufacturer's part number                                         | M                        | 4Dh        | M                        | 4Dh        |
| 75       | Manufacturer's part number                                         | 2                        | 32h        | 2                        | 32h        |
| 76       | Manufacturer's part number                                         | T                        | 54h        | T                        | 54h        |
| 77       | Manufacturer's part number                                         | R                        | 52h        | R                        | 52h        |
| 78       | Manufacturer's part number                                         | 7                        | 37h        | 7                        | 37h        |
| 79       | Manufacturer's part number                                         | 2                        | 32h        | 2                        | 32h        |
| 80       | Manufacturer's part number                                         | E                        | 45h        | E                        | 45h        |
| 81       | Manufacturer's part number                                         | P                        | 50h        | P                        | 50h        |
| 82       | Manufacturer's part number                                         | H                        | 4Eh        | H                        | 4Eh        |
| 83       | Manufacturer's part number                                         | –                        | 2Dh        | –                        | 2Dh        |
| 84       | Manufacturer's part number                                         | 8                        | 38h        | 8                        | 38h        |
| 85       | Manufacturer's part number                                         | SPACE                    | 20h        | A                        | 41h        |
| 86–90    | Manufacturer's part number                                         | SPACE                    | 20h        | SPACE                    | 20h        |
| 91       | Die revision code <sup>†</sup>                                     | TBD                      |            | TBD                      |            |
| 92       | PCB revision code <sup>†</sup>                                     | TBD                      |            | TBD                      |            |
| 93–94    | Manufacturing date <sup>†</sup>                                    | TBD                      |            | TBD                      |            |
| 95–98    | Assembly serial number <sup>†</sup>                                | TBD                      |            | TBD                      |            |
| 99–125   | Manufacturer-specific data <sup>†</sup>                            | TBD                      |            | TBD                      |            |
| 126      | Clock frequency                                                    | 100 MHz                  | 64h        | 100 MHz                  | 64h        |
| 127      | SDRAM component and clock interconnection details                  | 199                      | C7h        | 199                      | C7h        |
| 128–166  | System-integrator-specific data <sup>‡</sup>                       | TBD                      |            | TBD                      |            |
| 167–255  | Open                                                               |                          |            |                          |            |

<sup>†</sup> TBD indicates values that are determined at manufacturing time and are module-dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

**TM2TR64EPH, TM4TR64EPH  
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**serial presence detect (continued)**

**Table 4. Serial Presence Detect Data for the TM4TR72EPH**

| BYTE NO. | DESCRIPTION OF FUNCTION                                                        | TM4TR72EPH-8                                                                         |      | TM4TR72EPH-8A                                                                         |      |
|----------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|------|---------------------------------------------------------------------------------------|------|
|          |                                                                                | ITEM                                                                                 | DATA | ITEM                                                                                  | DATA |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                                                                            | 80h  | 128 bytes                                                                             | 80h  |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                                                                            | 08h  | 256 bytes                                                                             | 08h  |
| 2        | Fundamental memory type (FPM, EDO, SDRAM, . . .)                               | SDRAM                                                                                | 04h  | SDRAM                                                                                 | 04h  |
| 3        | Number of row addresses on this assembly                                       | 11                                                                                   | 0Bh  | 11                                                                                    | 0Bh  |
| 4        | Number of column addresses on this assembly                                    | 9                                                                                    | 09h  | 9                                                                                     | 09h  |
| 5        | Number of module rows on this assembly                                         | 2 banks                                                                              | 02h  | 2 banks                                                                               | 02h  |
| 6        | Data width of this assembly                                                    | 72 bits                                                                              | 48h  | 72 bits                                                                               | 48h  |
| 7        | Data width continuation                                                        |                                                                                      | 00h  |                                                                                       | 00h  |
| 8        | Voltage interface standard of this assembly                                    | LVTTL                                                                                | 01h  | LVTTL                                                                                 | 01h  |
| 9        | SDRAM cycle time at maximum supported CAS latency (CL), CL = X                 | $t_{CK} = 8 \text{ ns}$                                                              | 80h  | $t_{CK} = 8 \text{ ns}$                                                               | 80h  |
| 10       | SDRAM access from clock at CL = X                                              | $t_{AC} = 6 \text{ ns}$                                                              | 60h  | $t_{AC} = 6 \text{ ns}$                                                               | 60h  |
| 11       | DIMM configuration type (non-parity, parity, error correcting code [ECC])      | ECC                                                                                  | 02h  | ECC                                                                                   | 02h  |
| 12       | Refresh rate/type                                                              | 15.6 $\mu\text{s}$ /self-refresh                                                     | 80h  | 15.6 $\mu\text{s}$ /self-refresh                                                      | 80h  |
| 13       | SDRAM width, primary DRAM                                                      | x8                                                                                   | 08h  | x8                                                                                    | 08h  |
| 14       | Error-checking SDRAM data width                                                | x8                                                                                   | 08h  | x8                                                                                    | 08h  |
| 15       | Minimum clock delay, back-to-back random column addresses                      | 1 CK cycle                                                                           | 01h  | 1 CK cycle                                                                            | 01h  |
| 16       | Burst lengths supported                                                        | 1, 2, 4, 8                                                                           | 0Fh  | 1, 2, 4, 8                                                                            | 0Fh  |
| 17       | Number of banks on each SDRAM device                                           | 2 banks                                                                              | 02h  | 2 banks                                                                               | 02h  |
| 18       | CAS latencies supported                                                        | 2, 3                                                                                 | 06h  | 2, 3                                                                                  | 06h  |
| 19       | CS latency                                                                     | 0                                                                                    | 01h  | 0                                                                                     | 01h  |
| 20       | Write latency                                                                  | 0                                                                                    | 01h  | 0                                                                                     | 01h  |
| 21       | SDRAM module attributes                                                        | Non-buffered/<br>Non-registered                                                      | 00h  | Non-buffered/<br>Non-registered                                                       | 00h  |
| 22       | SDRAM device attributes: general                                               | $V_{DD}$ tolerance = (+10%)<br>Burst read/write,<br>precharge all,<br>auto precharge | 0Eh  | $V_{DD}$ tolerance = (+10%),<br>Burst read/write,<br>precharge all,<br>auto precharge | 0Eh  |
| 23       | Minimum clock cycle time at CL = X – 1                                         | $t_{CK} = 10 \text{ ns}$                                                             | A0h  | $t_{CK} = 15 \text{ ns}$                                                              | F0h  |
| 24       | Maximum data-access time from clock at CL = X – 1                              | $t_{AC} = 6.0 \text{ ns}$                                                            | 60h  | $t_{AC} = 7.5 \text{ ns}$                                                             | 75h  |
| 25       | Minimum clock cycle time at CL = X – 2                                         | N/A                                                                                  | 00h  | N/A                                                                                   | 00h  |
| 26       | Maximum data-access time from clock at CL = X – 2                              | N/A                                                                                  | 00h  | N/A                                                                                   | 00h  |
| 27       | Minimum row-precharge time                                                     | $t_{RP} = 20 \text{ ns}$                                                             | 14h  | $t_{RP} = 20 \text{ ns}$                                                              | 14h  |
| 28       | Minimum row-active to row-active delay                                         | $t_{RRD} = 16 \text{ ns}$                                                            | 10h  | $t_{RRD} = 16 \text{ ns}$                                                             | 10h  |
| 29       | Minimum $\overline{\text{RAS}}$ -to-CAS delay                                  | $t_{RCD} = 20 \text{ ns}$                                                            | 14h  | $t_{RCD} = 20 \text{ ns}$                                                             | 14h  |
| 30       | Minimum $\overline{\text{RAS}}$ pulse width                                    | $t_{RAS} = 48 \text{ ns}$                                                            | 30h  | $t_{RAS} = 48 \text{ ns}$                                                             | 30h  |
| 31       | Density of each bank on module                                                 | 16M Bytes                                                                            | 04h  | 16M Bytes                                                                             | 04h  |

serial presence detect (continued)

**Table 4. Serial Presence Detect Data for the TM4TR72EPH (Continued)**

| BYTE NO. | DESCRIPTION OF FUNCTION                           | TM4TR72EPH-8            |            | TM4TR72EPH-8A           |            |
|----------|---------------------------------------------------|-------------------------|------------|-------------------------|------------|
|          |                                                   | ITEM                    | DATA       | ITEM                    | DATA       |
| 32       | Command and address signal input setup time       | $t_{IS} = 2 \text{ ns}$ | 20h        | $t_{IS} = 2 \text{ ns}$ | 20h        |
| 33       | Command and address signal input hold time        | $t_{IH} = 1 \text{ ns}$ | 10h        | $t_{IH} = 1 \text{ ns}$ | 10h        |
| 34       | Data signal input setup time                      | $t_{IS} = 2 \text{ ns}$ | 20h        | $t_{IS} = 2 \text{ ns}$ | 20h        |
| 35       | Data signal input hold time                       | $t_{IH} = 1 \text{ ns}$ | 10h        | $t_{IH} = 1 \text{ ns}$ | 10h        |
| 36–61    | Superset features (may be used in the future)     |                         |            |                         |            |
| 62       | SPD revision                                      | Rev. 1.2                | 12h        | Rev. 1.2                | 12h        |
| 63       | Checksum for byte 0–62                            | 99                      | 63h        | 200                     | C8h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP–106E         | 97h                     | 9700...00h | 97h                     | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>               | TBD                     |            | TBD                     |            |
| 73       | Manufacturer's part number                        | T                       | 54h        | T                       | 54h        |
| 74       | Manufacturer's part number                        | M                       | 4Dh        | M                       | 4Dh        |
| 75       | Manufacturer's part number                        | 4                       | 34h        | 4                       | 34h        |
| 76       | Manufacturer's part number                        | T                       | 54h        | T                       | 54h        |
| 77       | Manufacturer's part number                        | R                       | 52h        | R                       | 52h        |
| 78       | Manufacturer's part number                        | 7                       | 37h        | 7                       | 37h        |
| 79       | Manufacturer's part number                        | 2                       | 32h        | 2                       | 32h        |
| 80       | Manufacturer's part number                        | E                       | 45h        | E                       | 45h        |
| 81       | Manufacturer's part number                        | P                       | 50h        | P                       | 50h        |
| 82       | Manufacturer's part number                        | H                       | 4Eh        | H                       | 4Eh        |
| 83       | Manufacturer's part number                        | –                       | 2Dh        | –                       | 2Dh        |
| 84       | Manufacturer's part number                        | 8                       | 38h        | 8                       | 38h        |
| 85       | Manufacturer's part number                        | SPACE                   | 20h        | A                       | 41h        |
| 86–90    | Manufacturer's part number                        | SPACE                   | 20h        | SPACE                   | 20h        |
| 91       | Die revision code <sup>†</sup>                    | TBD                     |            | TBD                     |            |
| 92       | PCB revision code <sup>†</sup>                    | TBD                     |            | TBD                     |            |
| 93–94    | Manufacturing date <sup>†</sup>                   | TBD                     |            | TBD                     |            |
| 95–98    | Assembly serial number <sup>†</sup>               | TBD                     |            | TBD                     |            |
| 99–125   | Manufacturer-specific data <sup>†</sup>           | TBD                     |            | TBD                     |            |
| 126      | Clock frequency                                   | 100 MHz                 | 64h        | 100 MHz                 | 64h        |
| 127      | SDRAM component and clock interconnection details | 247                     | F7h        | 247                     | F7h        |
| 128–166  | System-integrator-specific data <sup>‡</sup>      | TBD                     |            | TBD                     |            |
| 167–255  | Open                                              |                         |            |                         |            |

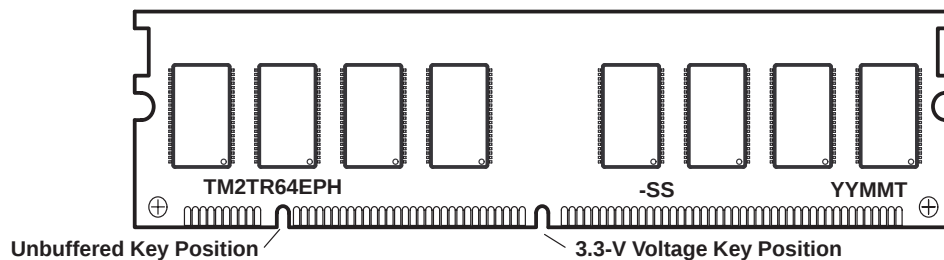
<sup>†</sup> TBD indicates values that are determined at manufacturing time and are module-dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

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**device symbolization (TM2TR64EPH illustrated)**



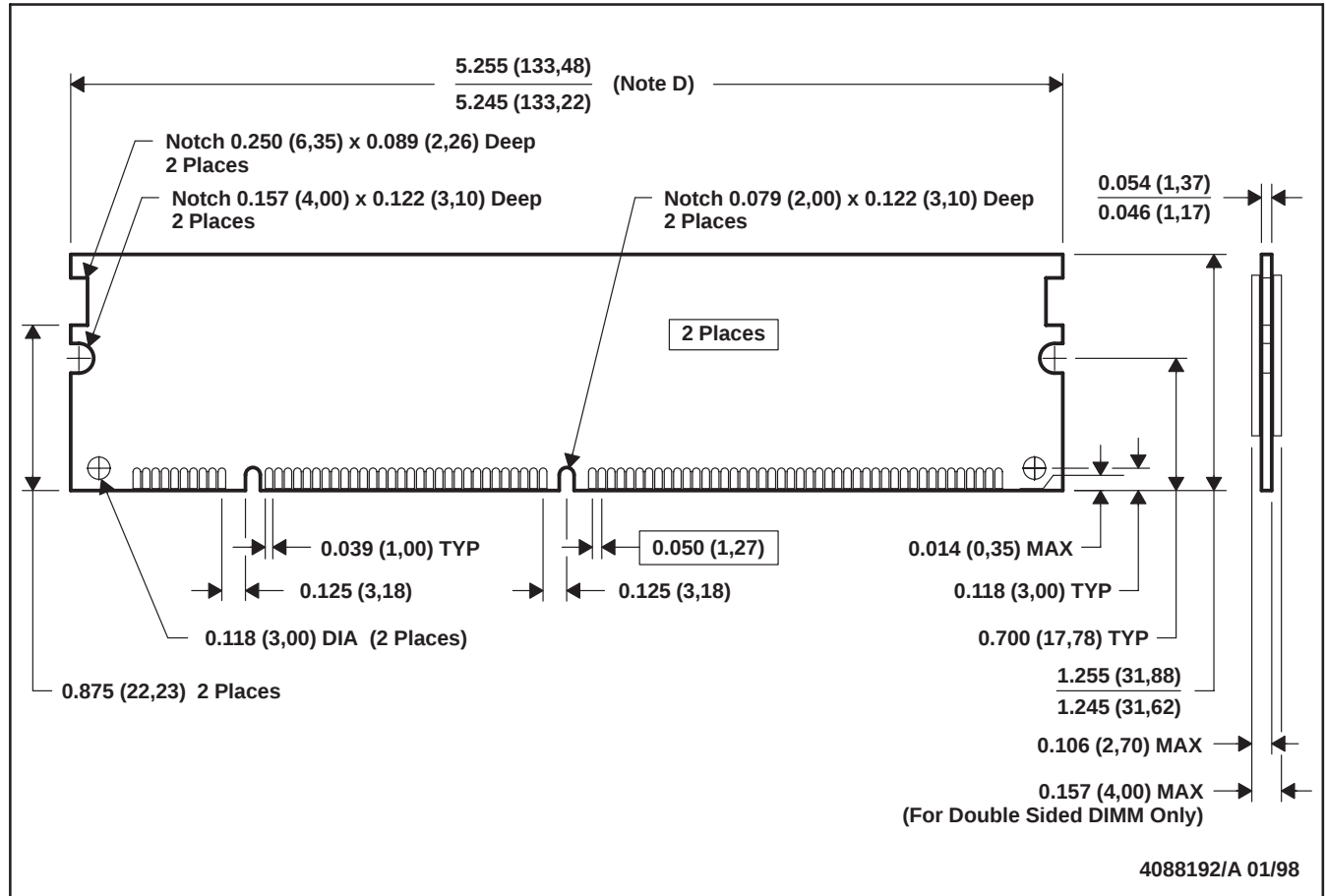
YY = Year Code  
MM = Month Code  
T = Assembly Site Code  
-SS = Speed Code

NOTE A: Location of symbolization may vary.

**MECHANICAL DATA**

**BUV (R-PDIM-N168)**

**DUAL-IN-LINE MEMORY MODULE**



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MO-161  
D. Dimension includes depanelization variations; applies between notch and tab edge.  
E. Outline may vary above notches to allow router/panelization irregularities.

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