- **Organization:**
  - **TM2CN64EFN . . . 2 097 152 x 64 Bits**
  - **TM4CN64EFN . . . 4 194 304 x 64 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **Designed for 66-MHz 4-Clock Systems**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **TM2CN64EFN — Uses Eight 16M-Bit (2M × 8-Bit) Synchronous Dynamic RAMs (SDRAMs) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM4CN64EFN — Uses Sixteen 16M-Bit (2M × 8-Bit) SDRAMs in Plastic TSOPs**
- **Byte-Read/Write Capability**
- **Performance Ranges:**

| | SYNCHRONOUS CLOCK CYCLE TIME | | ACCESS TIME CLOCK TO OUTPUT | | REFRESH INTERVAL |
|---|---|---|---|---|---|
| | $t_{CK3}$ (CL = 3)† | $t_{CK2}$ (CL = 2) | $t_{AC3}$ (CL = 3) | $t_{AC2}$ (CL = 2) | |
| 'xCN64EFN-10 | 10 ns | 15 ns | 7.5 ns | 8 ns | 64 ms |

† CL = CAS latency

- **High-Speed, Low-Noise, Low-Voltage TTL (LVTTL) Interface**
- **Read Latencies 2 and 3 Supported**
- **Support Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, and 8**
- **Two Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Electroless Gold-Finished Contacts**
- **Pipeline Architecture**
- **Serial Presence Detect (SPD) Using EEPROM**

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## description

The TM2CN64EFN is a 16M-byte, 168-pin dual-in-line memory module (DIMM). The DIMM is composed of eight TMS626812ADGE 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS626812A data sheet (literature number SMOS691).

The TM4CN64EFN is a 32M-byte, 168-pin DIMM. The DIMM is composed of sixteen TMS626812ADGE 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors.

## operation

The TM2CN64EFN operates as eight TMS626812ADGE devices that are connected as shown in the TM2CN64EFN functional block diagram. The TM4CN64EFN operates as sixteen TMS626812ADGE devices connected as shown in the TM4CN64EFN functional block diagram.

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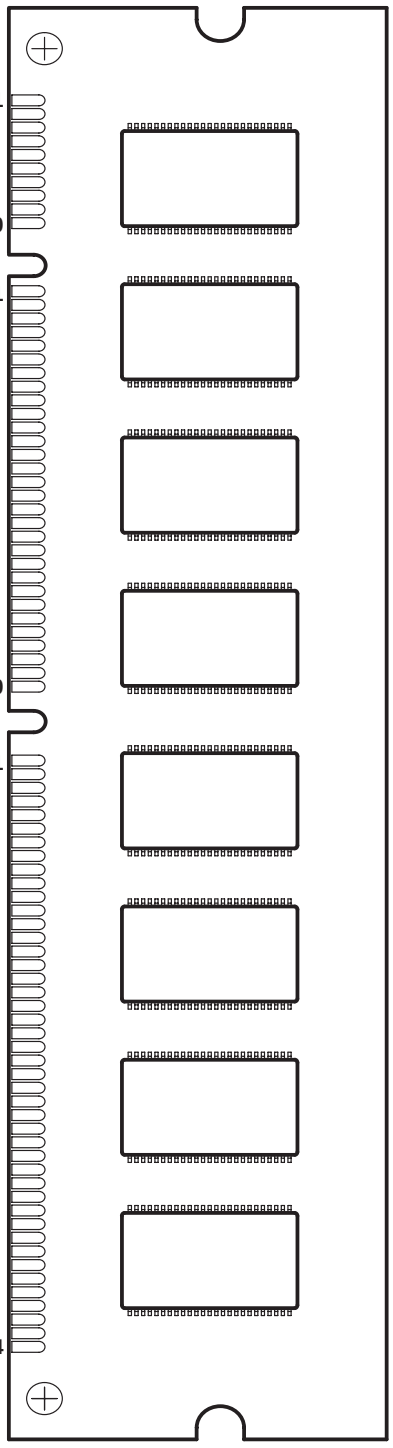
**DUAL-IN-LINE MEMORY MODULE (TOP VIEW)**




**TM2CN64EFN (SIDE VIEW)**

**TM4CN64EFN (SIDE VIEW)**

| PIN NOMENCLATURE | |
|---|---|
| A[0:10] | Row-Address Inputs |
| A[0:8] | Column-Address Inputs |
| A11/BA0 | Bank-Select Zero |
| $\overline{CAS}$ | Column-Address Strobe |
| CKE[0:1] | Clock Enable |
| CK[0:3] | System Clock |
| DQ[0:63] | Data-In/Data-Out |
| DQMB[0:7] | Data-In/Data-Out Mask Enable |
| NC | No Connect |
| $\overline{RAS}$ | Row-Address Strobe |
| $\overline{S}$[0:3] | Chip Select |
| SA[0:2] | Serial Presence Detect (SPD) Device Address Input |
| SCL | SPD Clock |
| SDA | SPD Address/Data |
| $V_{DD}$ | 3.3-V Supply |
| $V_{SS}$ | Ground |
| $\overline{WE}$ | Write Enable |
| WP | Write Protect |

## Pin Assignments

| PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME |
|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 43 | $V_{SS}$ | 85 | $V_{SS}$ | 127 | $V_{SS}$ |
| 2 | DQ0 | 44 | NC | 86 | DQ32 | 128 | CKE0 |
| 3 | DQ1 | 45 | $\overline{S2}$ | 87 | DQ33 | 129 | $\overline{S3}$ |
| 4 | DQ2 | 46 | DQMB2 | 88 | DQ34 | 130 | DQMB6 |
| 5 | DQ3 | 47 | DQMB3 | 89 | DQ35 | 131 | DQMB7 |
| 6 | $V_{DD}$ | 48 | NC | 90 | $V_{DD}$ | 132 | NC |
| 7 | DQ4 | 49 | $V_{DD}$ | 91 | DQ36 | 133 | $V_{DD}$ |
| 8 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 9 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | NC | 94 | DQ39 | 136 | NC |
| 11 | DQ8 | 53 | NC | 95 | DQ40 | 137 | NC |
| 12 | $V_{SS}$ | 54 | $V_{SS}$ | 96 | $V_{SS}$ | 138 | $V_{SS}$ |
| 13 | DQ9 | 55 | DQ16 | 97 | DQ41 | 139 | DQ48 |
| 14 | DQ10 | 56 | DQ17 | 98 | DQ42 | 140 | DQ49 |
| 15 | DQ11 | 57 | DQ18 | 99 | DQ43 | 141 | DQ50 |
| 16 | DQ12 | 58 | DQ19 | 100 | DQ44 | 142 | DQ51 |
| 17 | DQ13 | 59 | $V_{DD}$ | 101 | DQ45 | 143 | $V_{DD}$ |
| 18 | $V_{DD}$ | 60 | DQ20 | 102 | $V_{DD}$ | 144 | DQ52 |
| 19 | DQ14 | 61 | NC | 103 | DQ46 | 145 | NC |
| 20 | DQ15 | 62 | NC | 104 | DQ47 | 146 | NC |
| 21 | NC | 63 | CKE1 | 105 | NC | 147 | NC |
| 22 | NC | 64 | $V_{SS}$ | 106 | NC | 148 | $V_{SS}$ |
| 23 | $V_{SS}$ | 65 | DQ21 | 107 | $V_{SS}$ | 149 | DQ53 |
| 24 | NC | 66 | DQ22 | 108 | NC | 150 | DQ54 |
| 25 | NC | 67 | DQ23 | 109 | NC | 151 | DQ55 |
| 26 | $V_{DD}$ | 68 | $V_{SS}$ | 110 | $V_{DD}$ | 152 | $V_{SS}$ |
| 27 | $\overline{WE}$ | 69 | DQ24 | 111 | $\overline{CAS}$ | 153 | DQ56 |
| 28 | DQMB0 | 70 | DQ25 | 112 | DQMB4 | 154 | DQ57 |
| 29 | DQMB1 | 71 | DQ26 | 113 | DQMB5 | 155 | DQ58 |
| 30 | $\overline{S0}$ | 72 | DQ27 | 114 | $\overline{S1}$ | 156 | DQ59 |
| 31 | NC | 73 | $V_{DD}$ | 115 | $\overline{RAS}$ | 157 | $V_{DD}$ |
| 32 | $V_{SS}$ | 74 | DQ28 | 116 | $V_{SS}$ | 158 | DQ60 |
| 33 | A0 | 75 | DQ29 | 117 | A1 | 159 | DQ61 |
| 34 | A2 | 76 | DQ30 | 118 | A3 | 160 | DQ62 |
| 35 | A4 | 77 | DQ31 | 119 | A5 | 161 | DQ63 |
| 36 | A6 | 78 | $V_{SS}$ | 120 | A7 | 162 | $V_{SS}$ |
| 37 | A8 | 79 | CK2 | 121 | A9 | 163 | CK3 |
| 38 | A10 | 80 | NC | 122 | A11/BA0 | 164 | NC |
| 39 | NC | 81 | WP | 123 | NC | 165 | SA0 |
| 40 | $V_{DD}$ | 82 | SDA | 124 | $V_{DD}$ | 166 | SA1 |
| 41 | $V_{DD}$ | 83 | SCL | 125 | CK1 | 167 | SA2 |
| 42 | CK0 | 84 | $V_{DD}$ | 126 | NC | 168 | $V_{DD}$ |

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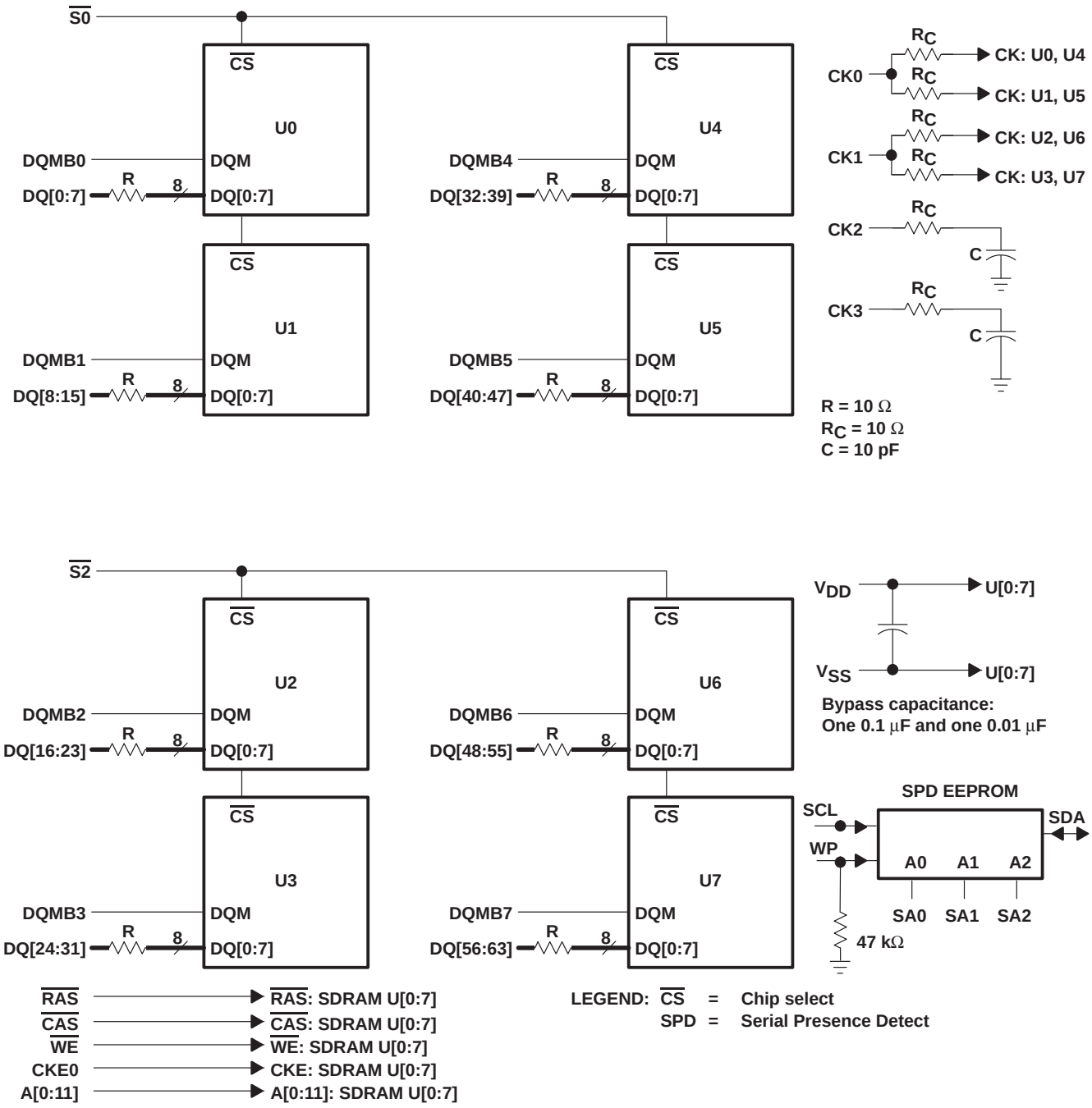
## dual-in-line memory module and components

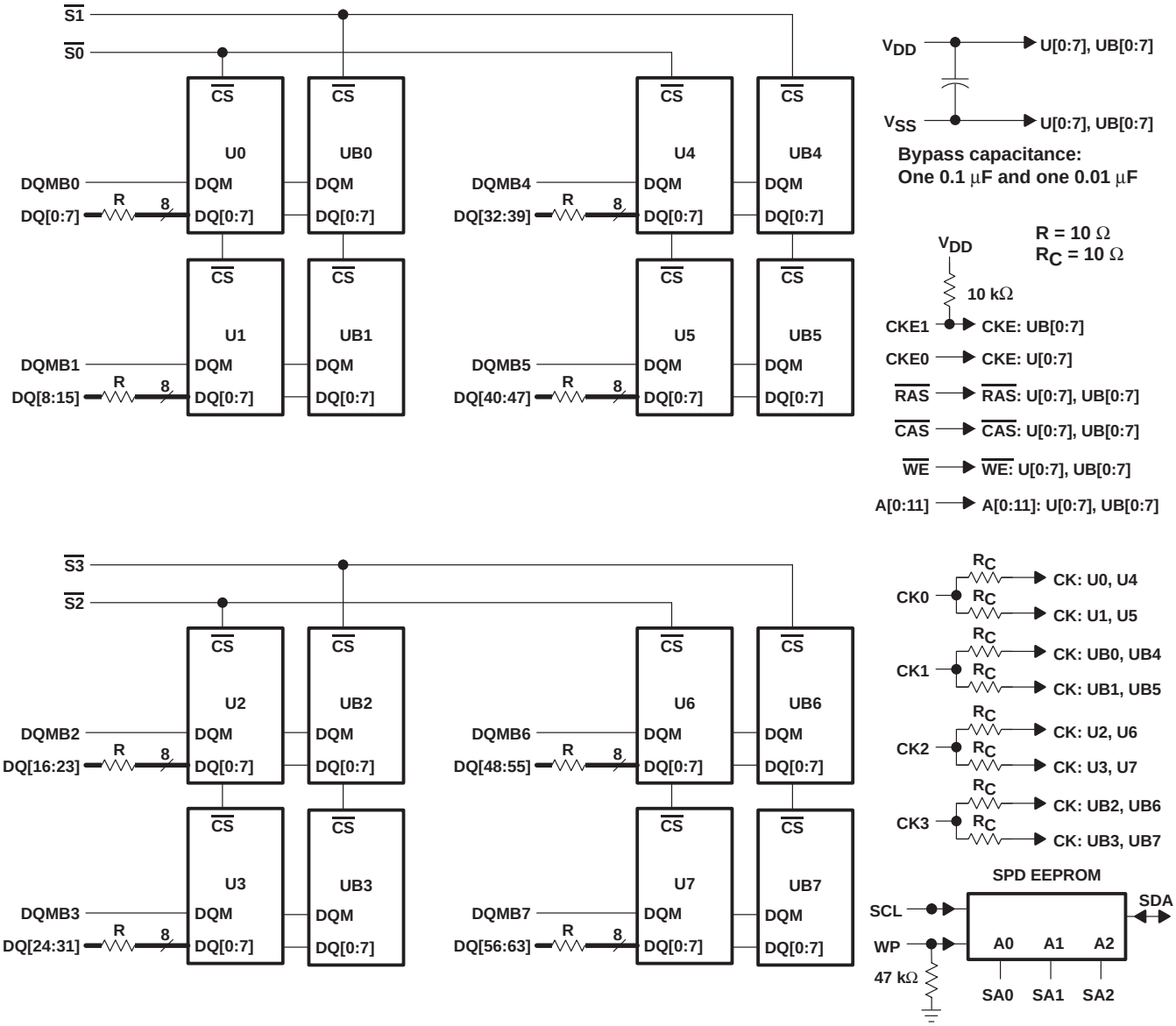
The dual-in-line memory module and components include:

- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and electroless gold-finished contacts over copper

## functional block diagram for the TM2CN64EFN



## functional block diagram for the TM4CN64EFN




PRODUCT PREVIEW

### absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD}$ . . . . . −0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . − 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM2CN64EFN . . . . . 8 W
TM4CN64EFN . . . . . 16 W
Ambient temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . − 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to $V_{SS}$.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $V_{IH}$ | High-level input voltage | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IH-SPD}$ | High-level input voltage for the SPD device | 2 | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage‡ | −0.3 | | 0.8 | V |
| $T_A$ | Ambient temperature | 0 | | 70 | °C |

‡ $V_{IL}$ MIN = −1.5 V ac (pulse width ≤ 5 ns)

### capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)§

| PARAMETER | | TMxCN64EFN | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $C_{i(CK)}$ | Input capacitance, CK input | | 4 | pF |
| $C_{i(AC)}$ | Input capacitance, address and control inputs: A0−A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | | 5 | pF |
| $C_{i(CKE)}$ | Input capacitance, CKE input | | 5 | pF |
| $C_o$ | Output capacitance | | 6.5 | pF |
| $C_{i(DQMBx)}$ | Input capacitance, DQMBx input | | 5 | pF |
| $C_{i(Sx)}$ | Input capacitance, $\overline{Sx}$ input | | 5 | pF |
| $C_{i/o(SDA)}$ | Input/output capacitance, SDA input | | 9 | pF |
| $C_{i(SPD)}$ | Input capacitance, SA0, SA1, SA2, SCL inputs | | 7 | pF |

§ Specifications in this table represent a single SDRAM device.

NOTE 2: $V_{DD}$ = 3.3 V ± 0.3 V. Bias on pins under test is 0 V.

## electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)†

| PARAMETER | | TEST CONDITIONS | | ’xCN64EFN-10 MIN | ’xCN64EFN-10 MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = − 2 mA | | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA | | | 0.4 | V |
| $I_I$ | Input current (leakage) | 0 V < $V_I$ < $V_{DD}$ + 0.3 V, All other pins = 0 V to $V_{DD}$ | | | ±10 | µA |
| $I_O$ | Output current (leakage) | 0 V < $V_O$ < $V_{DD}$ + 0.3 V, Output disabled | | | ±10 | µA |
| $I_{CC1}$ | Operating current | Burst length = 1, $t_{RC} \geq t_{RC}$ MIN, $I_{OH}/I_{OL}$ = 0 mA, one bank activated (see Note 4) | CAS latency = 2 | | 95 | mA |
| | | | CAS latency = 3 | | 105 | mA |
| $I_{CC2P}$ | Precharge standby current in power-down mode | CKE ≤ $V_{IL}$ MAX, $t_{CK}$ = 15 ns (see Note 5) | | | 2 | mA |
| $I_{CC2PS}$ | | CKE and CK ≤ $V_{IL}$ MAX, $t_{CK}$ = ∞ (see Note 6) | | | 2 | mA |
| $I_{CC2N}$ | Precharge standby current in non-power-down mode | CKE ≥ $V_{IH}$ MIN, $t_{CK}$ = 15 ns (see Note 5) | | | 25 | mA |
| $I_{CC2NS}$ | | CKE ≥ $V_{IH}$ MIN, CK ≤ $V_{IL}$ MAX, $t_{CK}$ = ∞ (see Note 6) | | | 2 | mA |
| $I_{CC3P}$ | Active standby current in power-down mode | CKE ≤ $V_{IL}$ MAX, $t_{CK}$ = 15 ns (see Note 5) | | | 3 | mA |
| $I_{CC3PS}$ | | CKE and CK ≤ $V_{IL}$ MAX, $t_{CK}$ = ∞ (see Note 6) | | | 3 | mA |
| $I_{CC3N}$ | Active standby current in non-power-down mode | CKE ≥ $V_{IH}$ MIN, $t_{CK}$ = 15 ns (see Note 5) | | | 30 | mA |
| $I_{CC3NS}$ | | CKE ≥ $V_{IH}$ MIN, CK ≤ $V_{IL}$ MAX, $t_{CK}$ = ∞ (see Note 6) | | | 10 | mA |
| $I_{CC4}$ | Burst current | Page burst, $I_{OH}/I_{OL}$ = 0 mA, All banks activated, $n_{CCD}$ = one cycle (see Note 7) | CAS latency = 2 | | 100 | mA |
| | | | CAS latency = 3 | | 130 | mA |
| $I_{CC5}$ | Auto-refresh current | $t_{RC} \leq t_{RC}$ MIN | CAS latency = 2 | | 85 | mA |
| | | | CAS latency = 3 | | 95 | mA |
| $I_{CC6}$ | Self-refresh current | CKE ≤ $V_{IL}$ MAX | | | 2 | mA |

† Specifications in this table represent a single SDRAM device.

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state twice during $t_{RC}$.
5. Control, DQ, and address inputs change state once every 30 ns.
6. Control, DQ, and address inputs do not change.
7. Control, DQ, and address inputs change state once every cycle.

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## ac timing requirements†

| | | 'xCN64EFN-10 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $t_{CK2}$ | Cycle time, CLK, CAS latency = 2 | 15 | | ns |
| $t_{CK3}$ | Cycle time, CLK, CAS latency = 3 | 10 | | ns |
| $t_{CH}$ | Pulse duration, CLK high | 3 | | ns |
| $t_{CL}$ | Pulse duration, CLK low | 3 | | ns |
| $t_{AC2}$ | Access time, CLK high to data out, CAS latency = 2 (see Note 8) | | 8 | ns |
| $t_{AC3}$ | Access time, CLK high to data out, CAS latency = 3 (see Note 8) | | 7.5 | ns |
| $t_{OH}$ | Hold time, CLK high to data out | 3 | | ns |
| $t_{LZ}$ | Delay time, CLK high to DQ in low-impedance state (see Note 9) | 2 | | ns |
| $t_{HZ}$ | Delay time, CLK high to DQ in high-impedance state (see Note 10) | | 8 | ns |
| $t_{IS}$ | Setup time, address, control, and data input | 3 | | ns |
| $t_{IH}$ | Hold time, address, control, and data input | 1 | | ns |
| $t_{CESP}$ | Power-down/self-refresh exit time | 10 | | ns |
| $t_{RAS}$ | Delay time, ACTV command to DEAC or DCAB command | 50 | 100000 | ns |
| $t_{RC}$ | Delay time, ACTV, REFR, or SLFR exit to ACTV, MRS, REFR, or SLFR command | 80 | | ns |
| $t_{RCD}$ | Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 11) | 30 | | ns |
| $t_{RP}$ | Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command | 30 | | ns |
| $t_{RRD}$ | Delay time, ACTV command in one bank to ACTV command in the other bank | 20 | | ns |
| $t_{RSA}$ | Delay time, MRS command to ACTV, MRS, REFR, or SLFR command | 20 | | ns |
| $t_{APR}$ | Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command | $t_{RP} - (CL - 1) * t_{CK}$ | | ns |
| $t_{APW}$ | Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command | $t_{RP} + t_{CK}$ | | ns |
| $t_T$ | Transition time (see Note 12) | 1 | 5 | ns |
| $t_{REF}$ | Refresh interval | | 64 | ms |
| $n_{CCD}$ | Delay time, READ or WRT command to an interrupting command | 1 | | cycle |
| $n_{CDD}$ | Delay time, $\overline{CS}$ low or high to input enabled or inhibited | 0 | 0 | cycle |
| $n_{CLE}$ | Delay time, CKE high or low to CLK enabled or disabled | 1 | 1 | cycle |
| $n_{CWL}$ | Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P | 1 | | cycle |
| $n_{DID}$ | Delay time, ENBL or MASK command to enabled or masked data in | 0 | 0 | cycle |
| $n_{DOD}$ | Delay time, ENBL or MASK command to enabled or masked data out | 2 | 2 | cycle |
| $n_{HZP2}$ | Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2 | | 2 | cycle |
| $n_{HZP3}$ | Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3 | | 3 | cycle |
| $n_{WCD}$ | Delay time, WRT command to first data in | 0 | 0 | cycle |
| $n_{WR}$ | Delay time, final data in of WRT operation to DEAC or DCAB command | 1 | | cycle |

† All references are made to the rising transition of CK unless otherwise noted.

NOTES: 8. $t_{AC}$ is referenced from the rising transition of CK that precedes to the data-out cycle. For example, the first-data out $t_{AC}$ is referenced from the rising transition of CK that is CAS latency − one cycle after the READ command. Access time is measured at output reference level 1.4 V.

9. $t_{LZ}$ is measured from the rising transition of CK that is CAS latency − one cycle after the READ command.
10. $t_{HZ}$ MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
11. For read or write operations with automatic deactivate, $t_{RCD}$ must be set to satisfy minimum $t_{RAS}$.
12. Transition time, $t_T$, is measured between $V_{IH}$ and $V_{IL}$.

## serial presence detect

The serial presence detect (SPD) is contained in a 256-byte serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see Table 1 and Table 2). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the Texas Instruments *Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

SPD contents for the TMxCN64EFN devices are listed in the following tables:

Table 1−TM2CN64EFN  Table 2−TM4CN64EFN

**Table 1. Serial Presence Detect Data for the TM2CN64EFN**

| BYTE NO. | DESCRIPTION OF FUNCTION | TM2CN64EFN-10 | |
|---|---|---|---|
| | | ITEM | DATA |
| 0 | Defines number of bytes written into serial memory during module manufacturing | 128 bytes | 80h |
| 1 | Total number of bytes of SPD memory device | 256 bytes | 08h |
| 2 | Fundamental memory type (FPM, EDO, SDRAM, . . .) | SDRAM | 04h |
| 3 | Number of row addresses on this assembly | 11 | 0Bh |
| 4 | Number of column addresses on this assembly | 9 | 09h |
| 5 | Number of module rows on this assembly | 1 bank | 01h |
| 6 | Data width of this assembly | 64 bits | 40h |
| 7 | Data width continuation | | 00h |
| 8 | Voltage interface standard of this assembly | LVTTL | 01h |
| 9 | SDRAM cycle time at maximum supported CAS latency (CL), CL = X | $t_{CK}$ = 10 ns | A0h |
| 10 | SDRAM access from clock at CL = X | $t_{AC}$ = 7.5 ns | 75h |
| 11 | DIMM configuration type (non-parity, parity, error correcting code [ECC]) | Non-Parity | 00h |
| 12 | Refresh rate/type | 15.6 µs/ self-refresh | 80h |
| 13 | SDRAM width, primary DRAM | x8 | 08h |
| 14 | Error-checking SDRAM data width | N/A | 00h |
| 15 | Minimum clock delay, back-to-back random column addresses | 1 CK cycle | 01h |
| 16 | Burst lengths supported | 1, 2, 4, 8 | 0Fh |
| 17 | Number of banks on each SDRAM device | 2 banks | 02h |
| 18 | CAS latencies supported | 2, 3 | 06h |
| 19 | CS latency | 0 | 01h |
| 20 | Write latency | 0 | 01h |
| 21 | SDRAM module attributes | Non-buffered/ Non-registered | 00h |
| 22 | SDRAM device attributes: general | $V_{DD}$ tolerance = (+10%), Burst read/write, precharge all, auto precharge | 0Eh |
| 23 | Minimum clock cycle time at CL = X − 1 | $t_{CK}$ = 15 ns | F0h |
| 24 | Maximum data-access time from clock at CL = X − 1 | $t_{AC}$ = 8 ns | 80h |

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## serial presence detect (continued)

**Table 1. Serial Presence Detect Data for the TM2CN64EFN (Continued)**

| BYTE NO. | DESCRIPTION OF FUNCTION | TM2CN64EFN-10 | |
|---|---|---|---|
| | | ITEM | DATA |
| 25 | Minimum clock cycle time at CL = X − 2 | N/A | 00h |
| 26 | Maximum data-access time from clock at CL = X − 2 | N/A | 00h |
| 27 | Minimum row-precharge time | $t_{RP}$ = 30 ns | 1Eh |
| 28 | Minimum row-active to row-active delay | $t_{RRD}$ = 20 ns | 14h |
| 29 | Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay | $t_{RCD}$ = 30 ns | 1Eh |
| 30 | Minimum $\overline{RAS}$ pulse width | $t_{RAS}$ = 50 ns | 32h |
| 31 | Density of each bank on module | 16M Bytes | 04h |
| 32 | Command and address signal input setup time | $t_{IS}$ = 3 ns | 30h |
| 33 | Command and address signal input hold time | $t_{IH}$ = 1 ns | 10h |
| 34 | Data signal input setup time | $t_{IS}$ = 3 ns | 30h |
| 35 | Data signal input hold time | $t_{IH}$ = 1 ns | 10h |
| 36−61 | Superset features (may be used in the future) | | |
| 62 | SPD revision | Rev. 1.2 | 12h |
| 63 | Checksum for byte 0−62 | 47 | 2Fh |
| 64−71 | Manufacturer's JEDEC ID code per JEP−106E | 97h | 9700...00h |
| 72 | Manufacturing location† | TBD | |
| 73 | Manufacturer's part number | T | 54h |
| 74 | Manufacturer's part number | M | 4Dh |
| 75 | Manufacturer's part number | 2 | 32h |
| 76 | Manufacturer's part number | C | 43h |
| 77 | Manufacturer's part number | N | 4Eh |
| 78 | Manufacturer's part number | 6 | 36h |
| 79 | Manufacturer's part number | 4 | 34h |
| 80 | Manufacturer's part number | E | 45h |
| 81 | Manufacturer's part number | F | 46h |
| 82 | Manufacturer's part number | N | 4Eh |
| 83 | Manufacturer's part number | − | 2Dh |
| 84 | Manufacturer's part number | 1 | 31h |
| 85 | Manufacturer's part number | 0 | 30h |
| 86−90 | Manufacturer's part number | SPACE | 20h |
| 91 | Die revision code† | TBD | |
| 92 | PCB revision code† | TBD | |
| 93−94 | Manufacturing date† | TBD | |
| 95−98 | Assembly serial number† | TBD | |
| 99−125 | Manufacturer-specific data† | TBD | |
| 126 | Clock frequency | 66 MHz | 66h |
| 127 | SDRAM component and clock interconnection details | 199 | C7h |
| 128−166 | System-integrator-specific data‡ | TBD | |
| 167−255 | Open | | |

† TBD indicates values are determined at manufacturing time and are module-dependent.
‡ These TBD values are determined and programmed by the customer (optional).

## serial presence detect (continued)

**Table 2. Serial Presence Detect Data for the TM4CN64EFN**

| BYTE NO. | DESCRIPTION OF FUNCTION | TM4CN64EFN-10 | |
|---|---|---|---|
| | | ITEM | DATA |
| 0 | Defines number of bytes written into serial memory during module manufacturing | 128 bytes | 80h |
| 1 | Total number of bytes of SPD memory device | 256 bytes | 08h |
| 2 | Fundamental memory type (FPM, EDO, SDRAM, . . .) | SDRAM | 04h |
| 3 | Number of row addresses on this assembly | 11 | 0Bh |
| 4 | Number of column addresses on this assembly | 9 | 09h |
| 5 | Number of module rows on this assembly | 2 banks | 02h |
| 6 | Data width of this assembly | 64 bits | 40h |
| 7 | Data width continuation | | 00h |
| 8 | Voltage interface standard of this assembly | LVTTL | 01h |
| 9 | SDRAM cycle time at maximum supported CAS latency (CL), CL = X | $t_{CK}$ = 10 ns | A0h |
| 10 | SDRAM access from clock at CL = X | $t_{AC}$ = 7.5 ns | 75h |
| 11 | DIMM configuration type (non-parity, parity, error correcting code [ECC]) | Non-Parity | 00h |
| 12 | Refresh rate/type | 15.6 µs/ self-refresh | 80h |
| 13 | SDRAM width, primary DRAM | x8 | 08h |
| 14 | Error-checking SDRAM data width | N/A | 00h |
| 15 | Minimum clock delay, back-to-back random column addresses | 1 CK cycle | 01h |
| 16 | Burst lengths supported | 1, 2, 4, 8 | 0Fh |
| 17 | Number of banks on each SDRAM device | 2 banks | 02h |
| 18 | CAS latencies supported | 2, 3 | 06h |
| 19 | CS latency | 0 | 01h |
| 20 | Write latency | 0 | 01h |
| 21 | SDRAM module attributes | Non-buffered/ Non-registered | 00h |
| 22 | SDRAM device attributes: general | $V_{DD}$ tolerance = (+10%), Burst read/write, precharge all, auto precharge | 0Eh |
| 23 | Minimum clock cycle time at CL = X − 1 | $t_{CK}$ = 15 ns | F0h |
| 24 | Maximum data-access time from clock at CL = X − 1 | $t_{AC}$ = 8 ns | 80h |
| 25 | Minimum clock cycle time at CL = X − 2 | N/A | 00h |
| 26 | Maximum data-access time from clock at CL = X − 2 | N/A | 00h |

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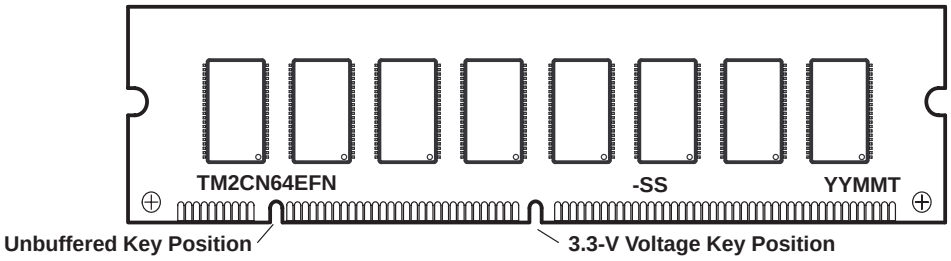
## serial presence detect (continued)

**Table 2. Serial Presence Detect Data for the TM4CN64EFN (Continued)**

| BYTE NO. | DESCRIPTION OF FUNCTION | TM4CN64EFN-10 | |
|---|---|---|---|
| | | ITEM | DATA |
| 27 | Minimum row-precharge time | $t_{RP}$ = 30 ns | 1Eh |
| 28 | Minimum row-active to row-active delay | $t_{RRD}$ = 20 ns | 14h |
| 29 | Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay | $t_{RCD}$ = 30 ns | 1Eh |
| 30 | Minimum $\overline{RAS}$ pulse width | $t_{RAS}$ = 50 ns | 32h |
| 31 | Density of each bank on module | 16M Bytes | 04h |
| 32 | Command and address signal input setup time | $t_{IS}$ = 3 ns | 30h |
| 33 | Command and address signal input hold time | $t_{IH}$ = 1 ns | 10h |
| 34 | Data signal input setup time | $t_{IS}$ = 3 ns | 30h |
| 35 | Data signal input hold time | $t_{IH}$ = 1 ns | 10h |
| 36−61 | Superset features (may be used in the future) | | |
| 62 | SPD revision | Rev. 1.2 | 12h |
| 63 | Checksum for byte 0−62 | 48 | 30h |
| 64−71 | Manufacturer's JEDEC ID code per JEP−106E | 97h | 9700...00h |
| 72 | Manufacturing location† | TBD | |
| 73 | Manufacturer's part number | T | 54h |
| 74 | Manufacturer's part number | M | 4Dh |
| 75 | Manufacturer's part number | 4 | 34h |
| 76 | Manufacturer's part number | C | 43h |
| 77 | Manufacturer's part number | N | 4Eh |
| 78 | Manufacturer's part number | 6 | 36h |
| 79 | Manufacturer's part number | 4 | 34h |
| 80 | Manufacturer's part number | E | 45h |
| 81 | Manufacturer's part number | F | 46h |
| 82 | Manufacturer's part number | N | 4Eh |
| 83 | Manufacturer's part number | − | 2Dh |
| 84 | Manufacturer's part number | 1 | 31h |
| 85 | Manufacturer's part number | 0 | 30h |
| 86−90 | Manufacturer's part number | SPACE | 20h |
| 91 | Die revision code† | TBD | |
| 92 | PCB revision code† | TBD | |
| 93−94 | Manufacturing date† | TBD | |
| 95−98 | Assembly serial number† | TBD | |
| 99−125 | Manufacturer-specific data† | TBD | |
| 126 | Clock frequency | 66 MHz | 66h |
| 127 | SDRAM component and clock interconnection details | 247 | F7h |
| 128−166 | System-integrator-specific data‡ | TBD | |
| 167−255 | Open | | |

† TBD indicates values are determined at manufacturing time and are module-dependent.
‡ These TBD values are determined and programmed by the customer (optional).

## device symbolization (TM2CN64EFN)



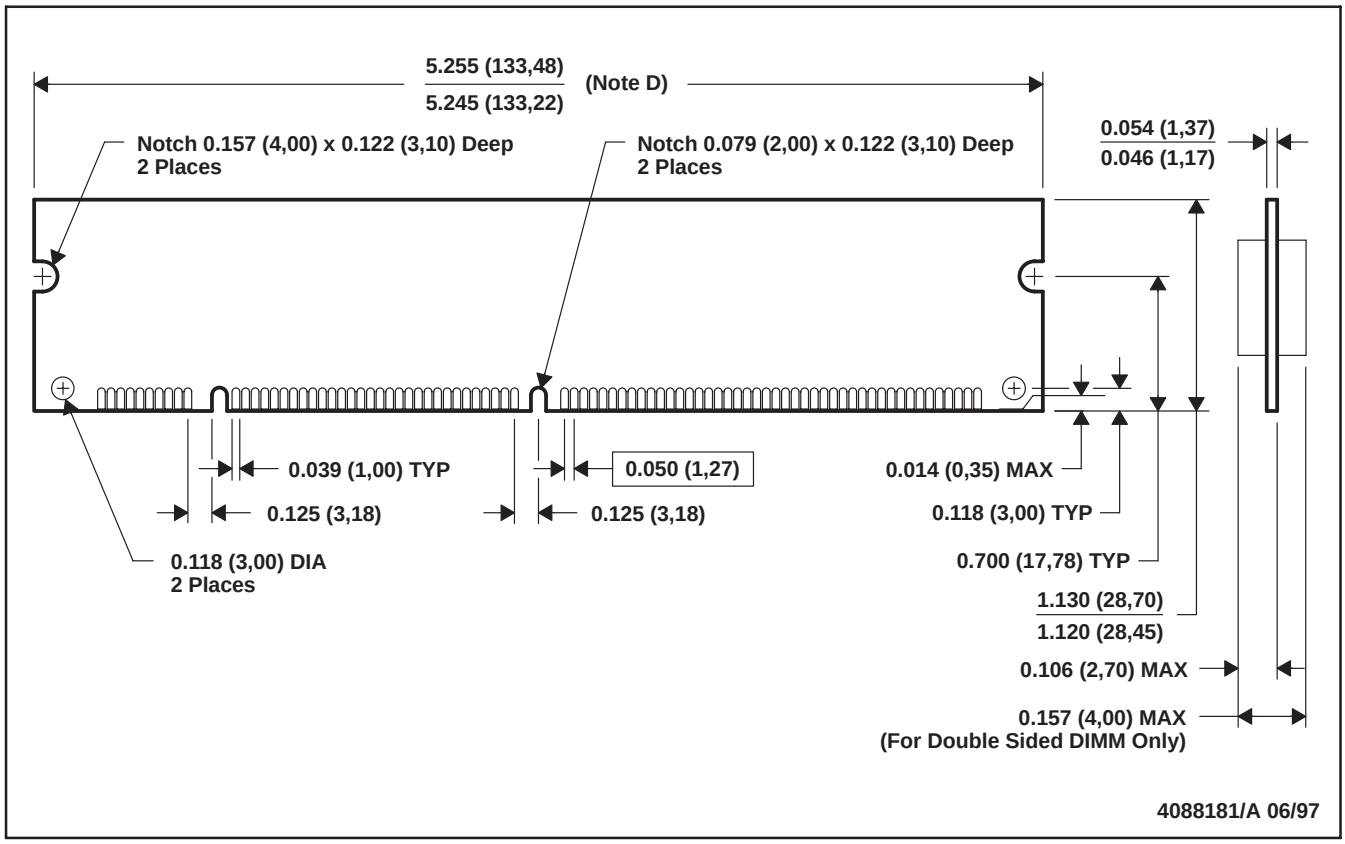

**YY = Year Code**
**MM = Month Code**
**T = Assembly Site Code**
**-SS = Speed Code**

NOTE A: Location of symbolization may vary.

PRODUCT PREVIEW

## MECHANICAL DATA

**BS (R-PDIM-N168)** **DUAL IN-LINE MEMORY MODULE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes De−panelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

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