MODEL NO. : TM045YYSP02

ISSUED DATE: 2013-01-29

VERSION : Ver 1.0

■Preliminary Specification
□Final Product Specification

Customer :

Approved by	Notes

SHANGHAI AVIC Confirmed :

Prepared by	Checked by	Approved by
JIN CHUAN 2013-01-29	CHEN CANHUI 2013-01-29	HE HAIJUN 2013-01-29

This technical specification is subjected to change without notice

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2013-01-29	Preliminary Specification Release	JIN CHUAN

1 General Specifications

Item	Specification	Unit
Substrate Thickness	0.25	mm
Panel Outline Dimension	58.34(H)X105.74(V)X0.5(D)	mm
Active Screen Size	4.5	Inch
Active Area	55.44(W)X98.64(H)	mm
Resolution	480xRGBx854	pixel
Pixel Size	0.1155(H) x0.1155(V)	um
Pixel Arrangement	Stripe	/
Pixel Driving Element	a-Si	/
Viewing Direction	all	o'clock
Gray Scale Inversion Direction	/	o'clock
Suggested driver IC	Himax: HX8379-A/HX8379-B Orise: OTM8009A/OTM8018B ILI: ILI9806	/

Note 1: Viewing direction for best image quality is different from TFT definition; there is a 180 degree shift.

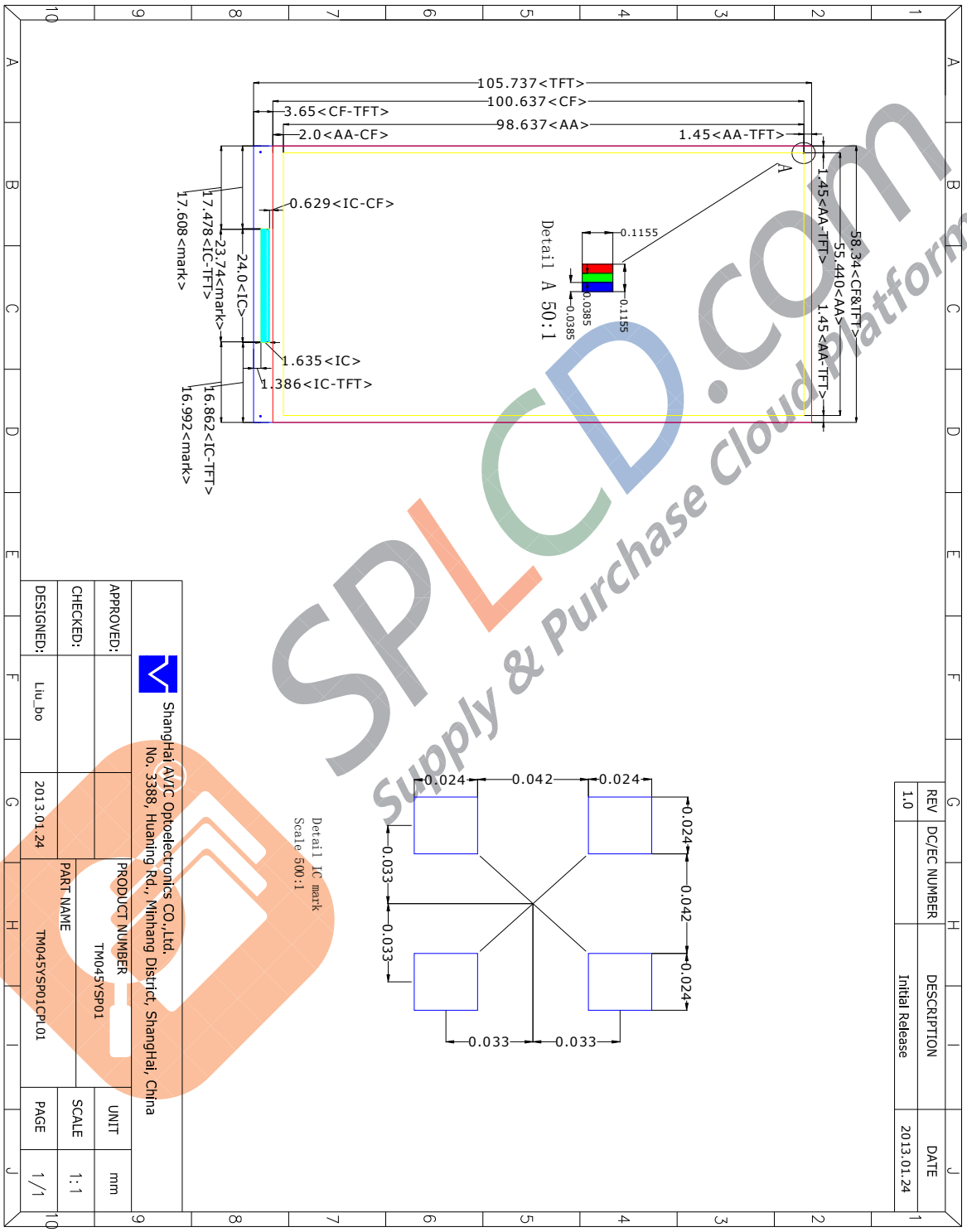
Note 2: Requirements on Environmental Protection: RoHS

Note 3: Substrate represents TFT or CF side thickness.

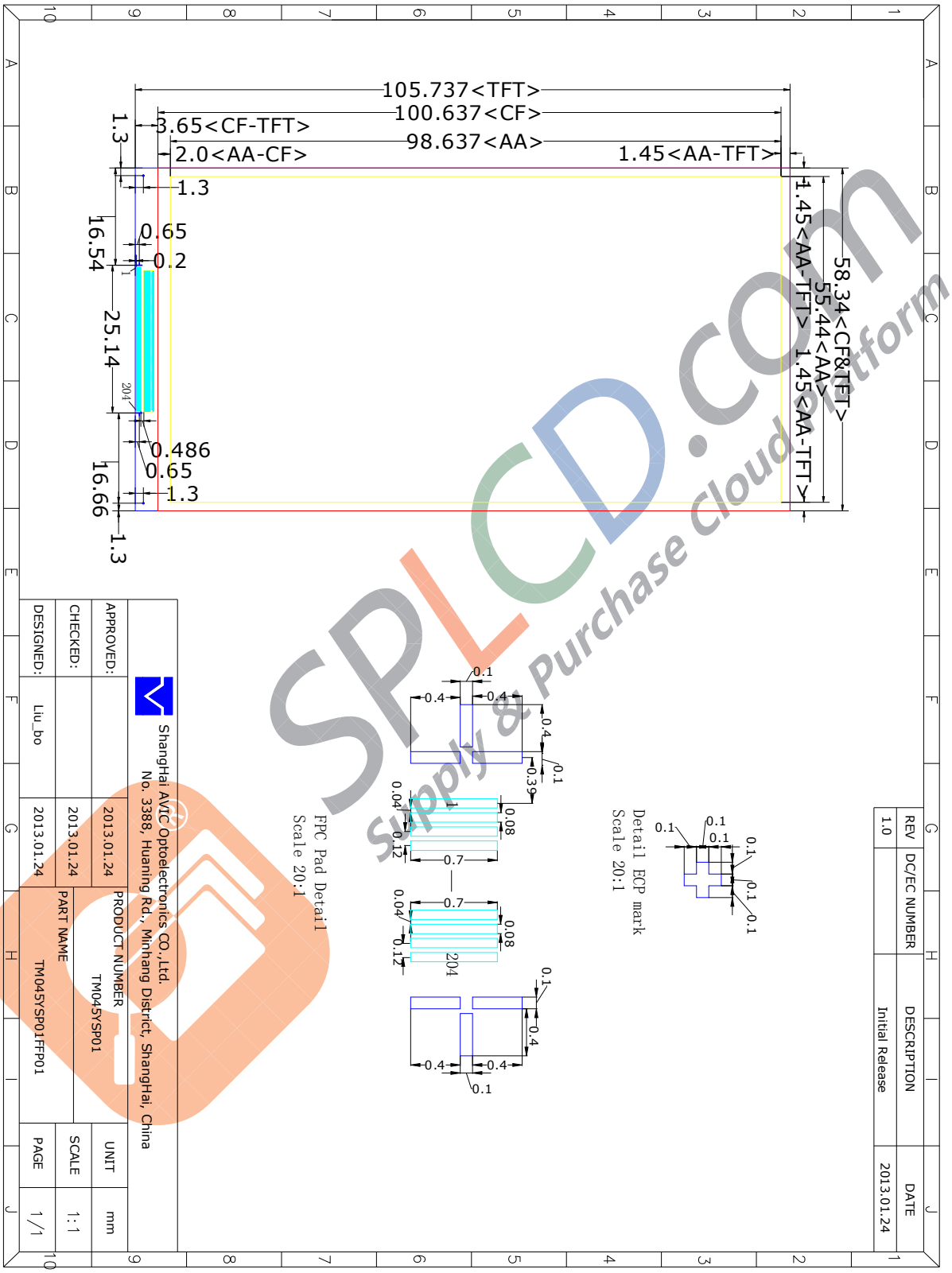
Note 4: LCD weight tolerance: +/- 5%

2 Dimension

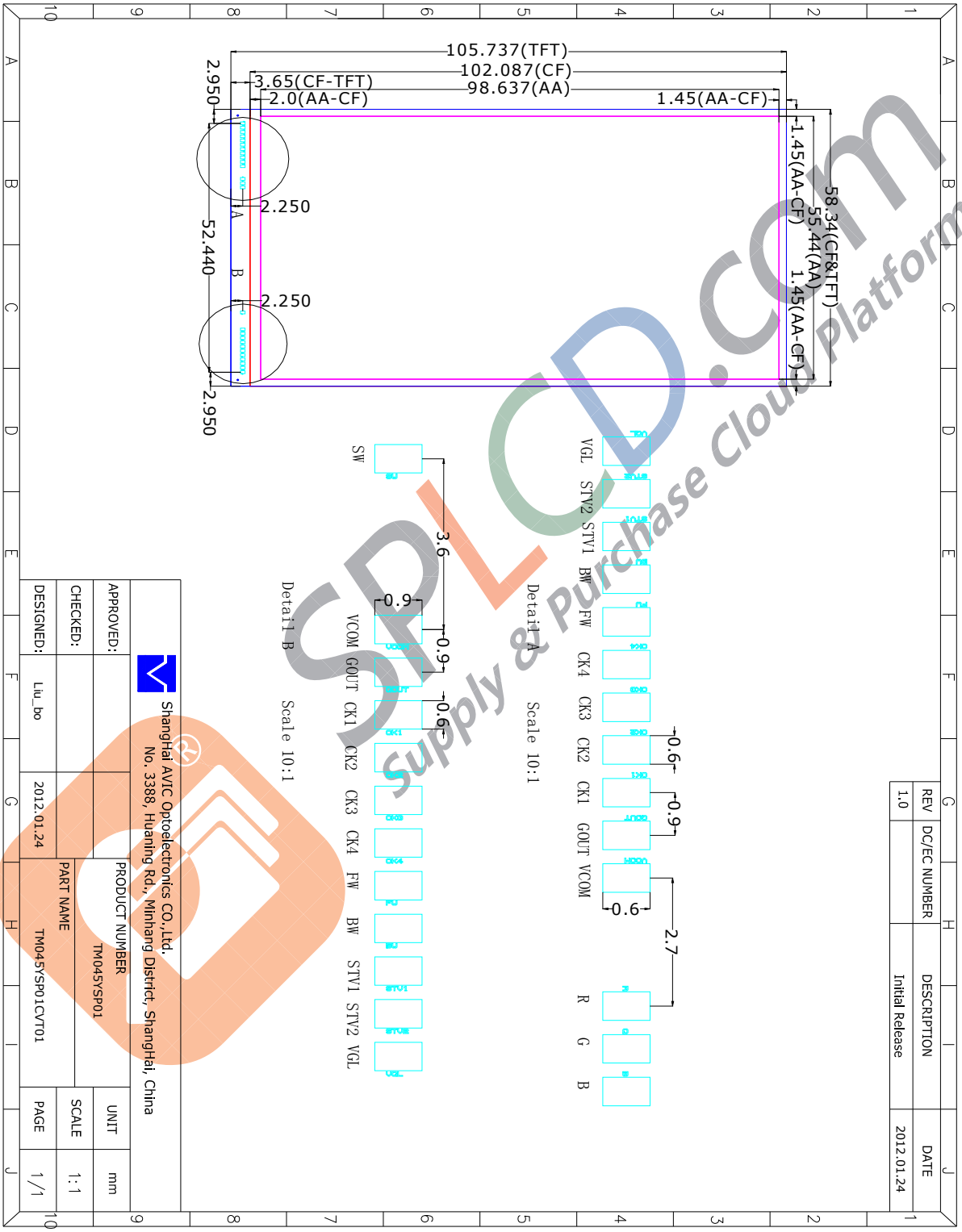
2.1 Outline Dimension

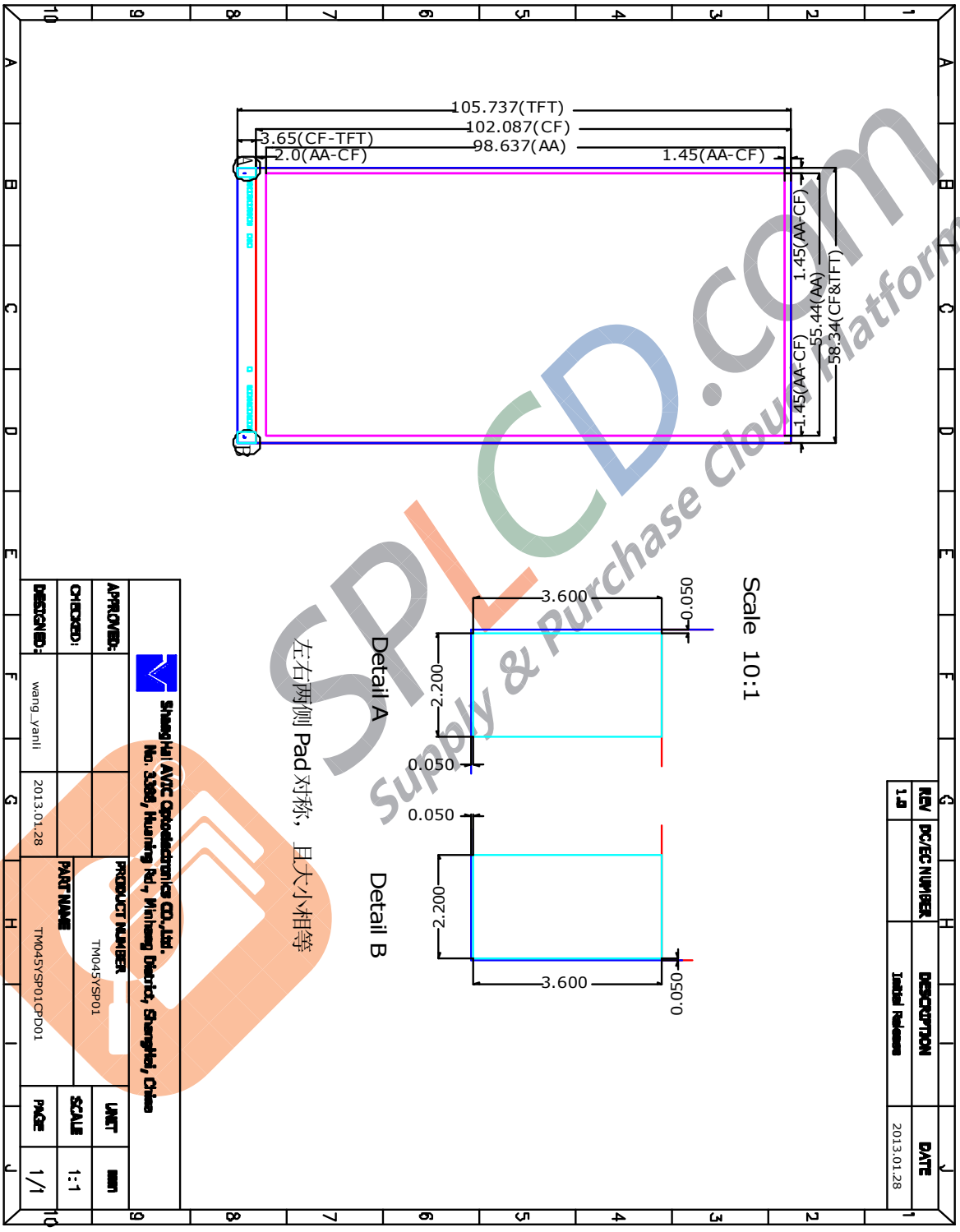


2.2 FPC Detail



2.3 CELL Visual Test Pad





3 FPC PIN Assignment

3.1 Pin Definition

Pin No.	OTM8009A	Note
1	DUMMY	Not used. Let it open.
2	GND	Ground
3	VCOM	Regulator output for common voltage of panel. Connect a capacitor for stabilization.
4	VCOM	
5	VCOM	
6	VCOM	
7	CONTACT2B	Test pin,for test bonding quality, IC internal will connect CONTACT2A with CONTACT2B
8	CONTACT2A	
9	VGL	Substrate voltage for driver IC.Please connect VGL to VGLX.
10	VGL	
11	VGLO	Low voltage level for gate control signals and gate circuit of panel.
12	VGLO	
13	VGL_REG	Output voltage generated from VGLX. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
14	C51N	Capacitor connection pins for the step-up circuit which generate VGLX. Connect capacitor as requirement.
15	C51N	
16	C51P	
17	C51P	
18	VGH	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
19	VGH	
20	C41N	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
21	C41N	
22	C41P	
23	C41P	
24	DVSS	Digital GND
25	DVDD	Regulator output for logic system power (1.55V typical),Connect a capacitor for stabilization.
26	C32N	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
27	C32N	
28	C32P	
29	C32P	
30	C31N	
31	C31N	
32	C31P	
33	C31P	
34	VSSB	DC/DC GND
35	VSSB	
36	AVSS	Source OP GND
37	VCL	Output voltage from step-up circuit 3,

38	VCL	generated from VDDB.Connect a capacitor for stabilization.
39	VDDB	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
40	VDDB	
41	C24N	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement. When not in used, please open these pins.
42	C24N	
43	C24P	
44	C24P	
45	C23N	
46	C23N	
47	C23P	
48	C23P	
49	C22N	
50	C22N	
51	C22P	
52	C22P	
53	C21N	
54	C21N	
55	C21P	
56	C21P	
57	AVEE	Output voltage from step-up circuit 2, generated from VDDB.Connect a capacitor for stabilization.
58	AVEE	
59	AVSS	Source OP GND
60	AVSS	
61	AVDD	Output voltage from step-up circuit 1, generated from VDDB.Connect a capacitor for stabilization.
62	AVDD	
63	C14N	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
64	C14N	
65	C14P	
66	C14P	
67	C13N	
68	C13N	
69	C13P	
70	C13P	
71	C12N	
72	C12N	
73	C12P	
74	C12P	
75	C11N	
76	C11N	
77	C11P	
78	C11P	
79	VSSB	DC/DC GND
80	VSSB	
81	VDDB	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the
82	VDDB	

		same input voltage level
83	CSN	Current sensing input for PFM2 DC/DC converter (generate AVEE).When not in use, please connect to VSSB.
84	EXTN	PFM2 control output for DC/DC converter to generate AVEE.Connect to gate of external PMOS device. When not in use, please open this pin.
85	CSP	Current sensing input for PFM1 DC/DC converter (generate AVDD).When not in use, please connect to VSSB.
86	EXTP	PFM1 control output for DC/DC converter to generate AVDD. Connect to gate of external NMOS device. When not in use, please open this pin.
87	VREFCP	Reference voltage for internal voltage generating circuit.Connect capacitor for stabilization.
88	VSSR	Regulator GND
89	VSSR	
90	TE_R	The same output signal as TE (TE_L) pin.TE_L and TE_R can not be connected together, choose one side for application.
91	VDDR	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
92	VDDAM	Power supply for MIPI/MDDI analog regulator system
93	VDDAM	
94	MVDDA	Regulator output for internal MIPI/MDDI analog system (1.5V typical)Connect a capacitor for stabilization.
95	MVDDL	Regulator output for internal MIPI low power system (1.2V typical)Connect a capacitor for stabilization.
96	VSSAM	MIPI GND
97	HSSI_D0_N	These pins are DSI-D0+/- differential data signals.
98	HSSI_D0_N	
99	HSSI_D0_P	
100	HSSI_D0_P	
101	VSSAM	MIPI GND
102	HSSI_CLK_N	These pins are DSI-CLK+/- differential clock signals.
103	HSSI_CLK_N	
104	HSSI_CLK_P	
105	HSSI_CLK_P	

106	VSSAM	MIPI GND
107	HSSI_D1_N	These pins are DSI-D1+/- differential data signals.
108	HSSI_D1_N	
109	HSSI_D1_P	
110	HSSI_D1_P	
111	VSSAM	MIPI GND
112	DVDD	Regulator output for logic system power (1.55V typical).Connect a capacitor for stabilization.
113	DVSS	Digital GND
114	VDDA	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
115	AVEE	Output voltage from step-up circuit 2, generated from VDDB.Connect a capacitor for stabilization.
116	AVEE	
117	AVSS	Source OP GND
118	AVDD	Output voltage from step-up circuit 1, generated from VDDB.Connect a capacitor for stabilization.
119	AVDD	
120	VSSI	I/O GND
121	VDDI	Power supply for interface system except MIPI/MDDI interface
122	ERR	CRC and ECC error output pin for MIPI interface.
123	LEDON	It is a LED driver control signal.
124	LEDPWM	It is a PWM type control signal for brightness of the LED backlight.
125	VS	Vertical sync. Signal in RGB I/F.connect to VSSI this pin.
126	HS	Horizontal sync. Signal in RGB I/F.connect to VSSI this pin.
127	PCLK	Pixel clock signal in RGB I/F.connect to VSSI this pin.
128	DE	Data enable signal in RGB I/F mode 1.connect to VSSI this pin.
129	D0	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For 8080-series MPU I/F: 8-bit interface: D[7:0] are used, D[23:8] should be connected to VSSI 16-bit interface: D[15:0] are used, D[23:16] should be connected to VSSI 18-bit interface: D[17:0] are used, D[23:18] should be connected to VSSI 24-bit interface: D[23:0] are used
130	D1	
131	D2	
132	D3	
133	D4	
134	D5	
135	D6	
136	D7	
137	D8	
138	D9	
139	D10	
140	D11	
141	D12	

142	D13	
143	D14	
144	D15	
145	D16	
146	D17	
147	D18	
148	D19	
149	D20	
150	D21	
151	D22	
152	D23	
153	VDDI	Power supply for interface system except MIPI/MDDI interface
154	VSSI	I/O GND
155	RESX	This signal will reset the device
156	CSX	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F.connect to VDDI this pin.
157	RDX	Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface.connect to VDDI this pin.
158	WRX	This pin is not used for MIPI I/F, please connect to VDDI this pin.
159	DCX	Display data / command selection in 80-series MPU I/F.
160	SDI	Serial input signal in SPI I/F.
161	SDO	Please open this pin.
162	TE_L	Tearing effect output pin.
163	EXB1T	Input pin to select the external AVDD DC/DC voltage.
164	GPO2	General purpose output pins.
165	IM0	Interface type selection.
166	IM1	
167	IM2	
168	IM3	
169	I2C_SA0	Select the I2C interface address from MPU. If not used, please connect to VSSI.
170	RGBBP	Please connect to VSSI.
171	PSWAP	Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only.
172	DSWAP	
173	LANSEL	Input pin to select 1 data lane or 2 data lanes in MIPI interface.
174	AVSS	Source OP GND
175	VCL	Output voltage from step-up circuit 3, generated from VDDB.Connect a capacitor for stabilization.
176	VCL	
177	VDDB	Power supply for DC/DC converter

178	VDDB	VDDB, VDDA and VDDR should be the same input voltage level
179	DVDD	Regulator output for logic system power (1.55V typical)Connect a capacitor for stabilization.
180	DVSS	Digital GND
181	VGMP	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
182	VGMN	Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.
183	VGSN	Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.
184	VDD_DET	Connect to VDDB/VDDA/VDDR for detection.
185	VSSR	Regulator GND
186	VDDR	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
187	VDDA	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
188	VSSA	Analog GND
189	VREF_PWR	Regulator output for power voltage. Connect a capacitor for stabilization.
190	VCL	Output voltage from step-up circuit 3, generated from VDDB.Connect a capacitor for stabilization.
191	VCL	
192	VGL_REG	Substrate voltage for driver IC. Please connect VGL to VGLX.
193	VGLO	Low voltage level for gate control signals and gate circuit of panel.
194	VGLX	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
195	MTP_PWR	MTP programming power supply pin (7.5 to 8.0V and 7.75V typical)
196	MTP_PWR	
197	VCOM	Regulator output for common voltage of panel. Connect a capacitor for stabilization.
198	VCOM	
199	VCOM	
200	VCOM	
201	FOG_1	
202	FOG_2	
203	GND	Ground
204	DUMMY	Not used. Let it open.

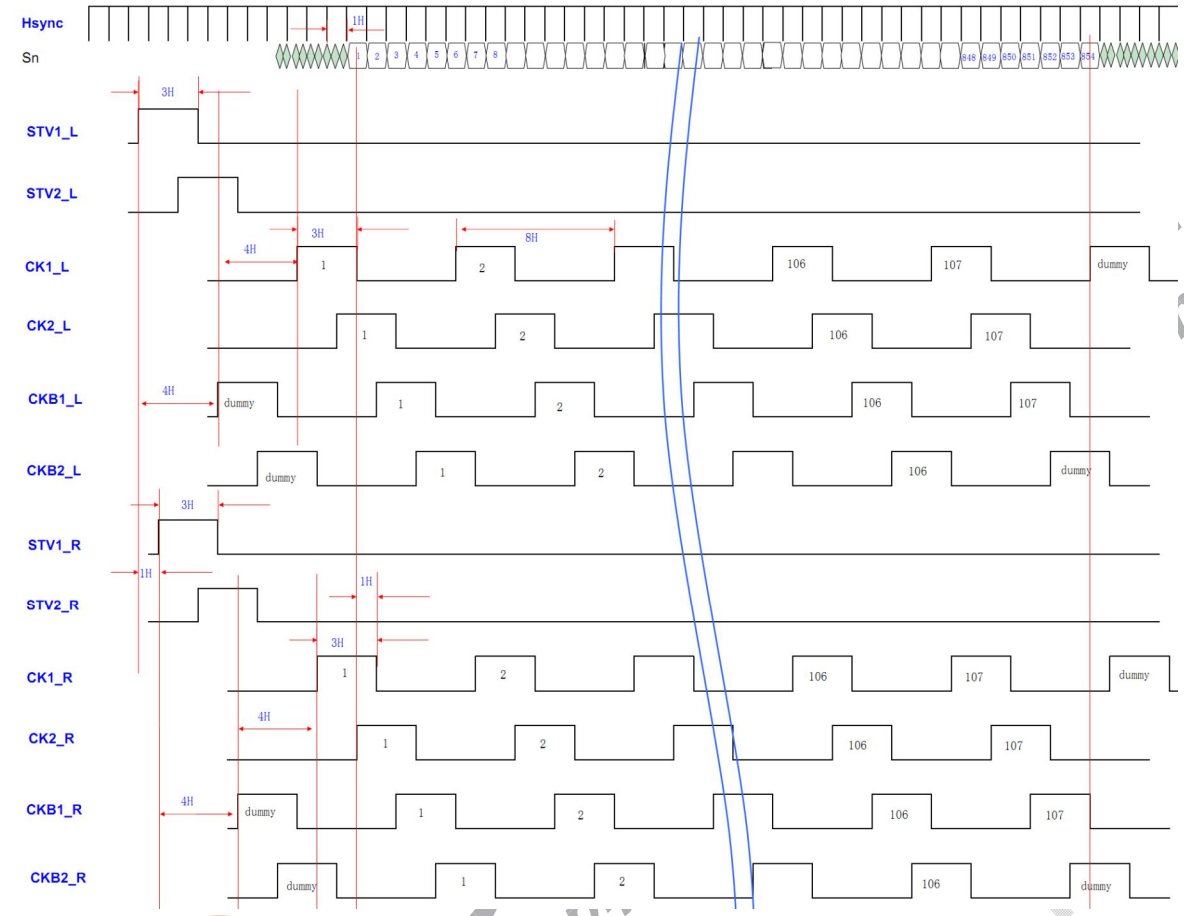
3.2 GIP(gate in panel) pin mapping and input timing

Pin mapping

STV1_L	---->	GOUT24
STV2_L	---->	GOUT23
CK1_L	---->	GOUT25
CK2_L	---->	GOUT26
CKB1_L	---->	GOUT27
CKB2_L	---->	GOUT28
FW_L	---->	GOUT32
BW_L	---->	GOUT31
STV1_R	---->	GOUT9
STV2_R	---->	GOUT10
CK1_R	---->	GOUT8
CK2_R	---->	GOUT7
CKB1_R	---->	GOUT6
CKB2_R	---->	GOUT5
FW_R	---->	GOUT1
BW_R	--->	GOUT2

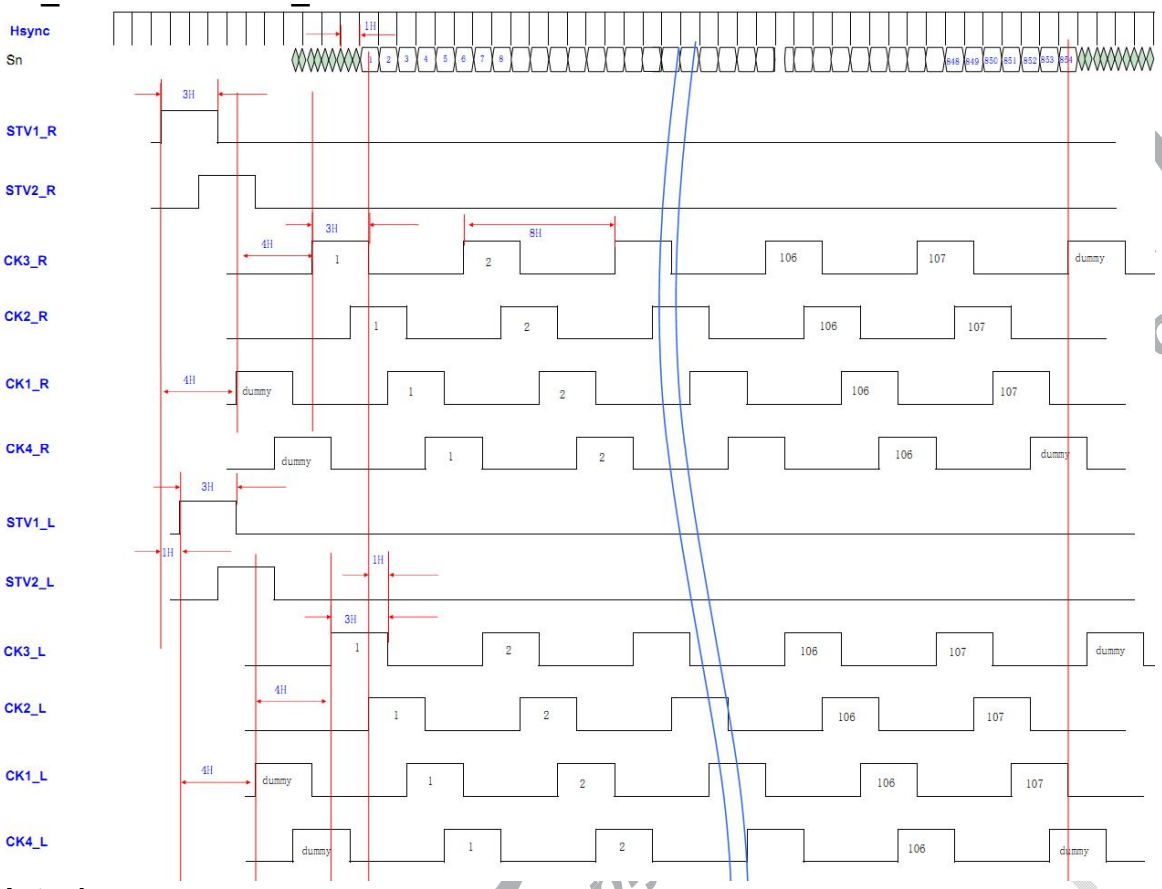
3.3 Forward scan timing

FW_L / R = 'H' BW_L / R = 'L'



3.4 Backward scan timing

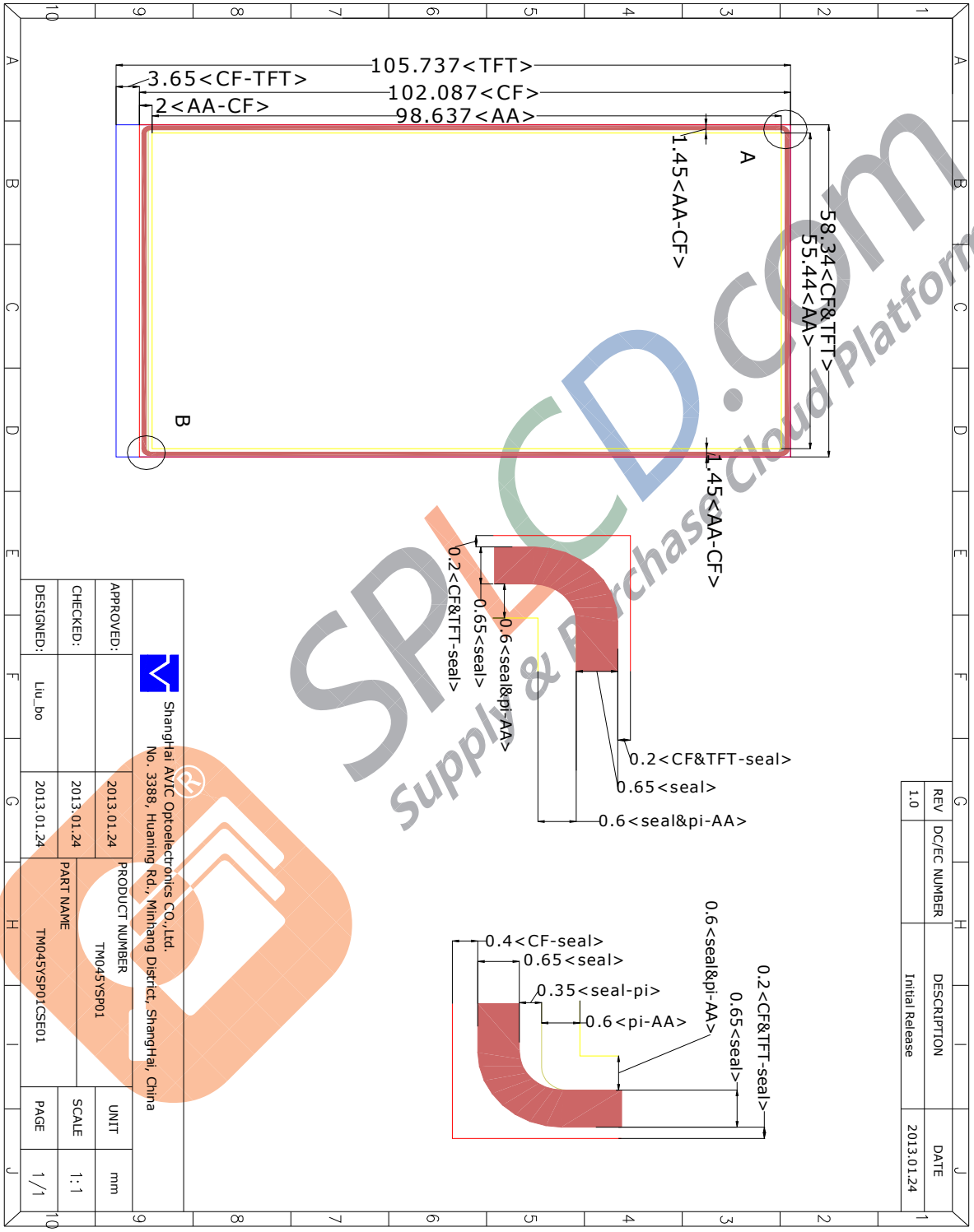
FW_L / R = 'L' BW_L / R = 'H'



Note 1：NT35510 can not be backward scan.

4 Cell Process Rule

4.1 Seal Pattern



5 Electrical Specification

5.1 Electrical Characteristics

Symbol	Status	Specification			Unit
		Min	Typ	Max	
CK/CKB/STV/RESET	H	14.5	+15	15.5	V
	L	-10.5	-10	-9.5	V
FW/BW	H	14.5	+15	15.5	V
	L	-10.5	-10	-9.5	V
VGL	--	-10.5	-10	-9.5	V
VCOM	--	-2	-1.63	0	V

Note:

(1) Vcom must be adjusted to optimize display quality: cross talk, contrast ratio and etc.

(2) VGH is TFT gate on voltage

(3) VGL is TFT gate off voltage

The storage capacitance structure of this product is Cst(Storage on Common).

The low voltage level of VGL signal must be fluctuated with same phase as Vcom, in case of Storage on Gate structure.

(4) Environmental condition : 25℃

6 Optical Specification

6.1 Optical Specification

Light Source: C-light (With EWV Polarizer) Ta=25℃

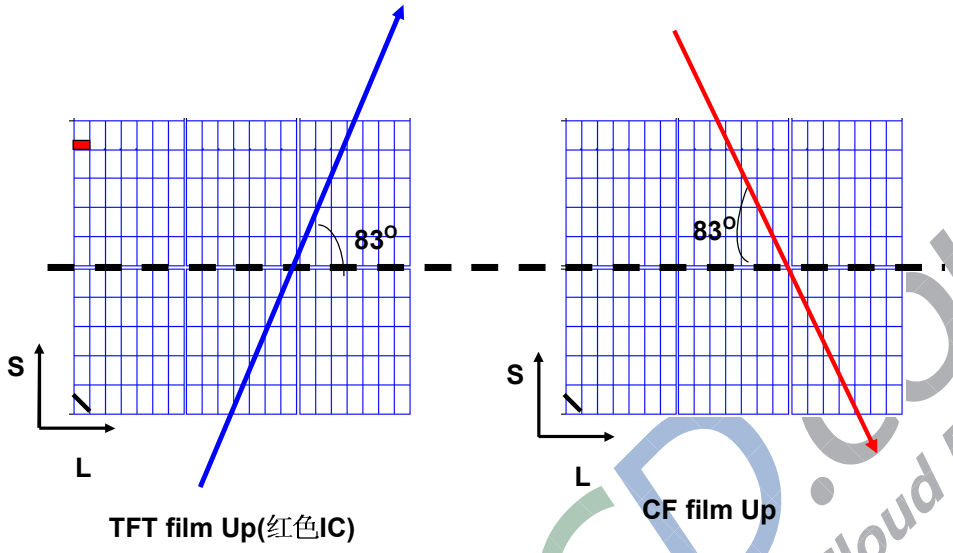
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	-	80	-	Degree	Note 2
		θB		-	80	-		
		θL		-	80	-		
		θR		-	80	-		
Contrast Ratio		CR	θ=0°	600	800	-	-	Note1 Note3
Response Time		T_{ON}	25℃	-	25	35	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	C-Light	-	0.309±0.03	-		Note5 Note1
		y		-	0.354±0.03	-		
	Red	x		-	0.661±0.03	-		
		y		-	0.326±0.03	-		
	Green	x		-	0.259±0.03	-		
		y		-	0.588±0.03	-		
	Blue	x		-	0.139±0.03	-		
		y		-	0.108±0.03	-		
NTSC		-	-	65	70	-	%	Note 5
Transmittance		T	-	4.14	4.40	-	%	Note 1

Test Conditions:

1. The ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

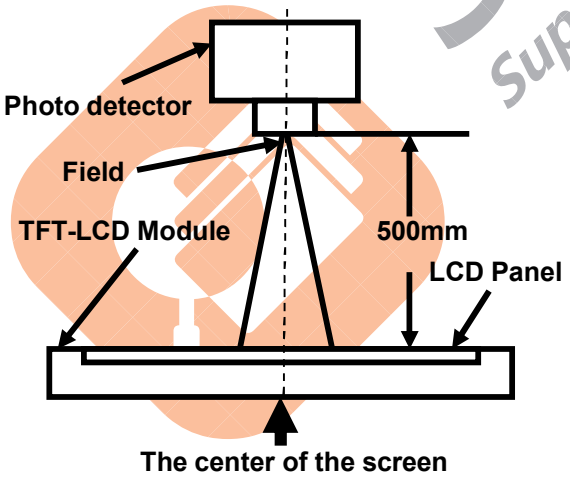
The Transmittance and NTSC are the emulated values base on the panel with 0-TAC polarizer and C-Light, and when using LED back light they will be to decrease about 0.3%.

6.2 Rubbing Direction



Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Chromaticity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system, viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).

Viewing angle is measured With EWV Polarizer.

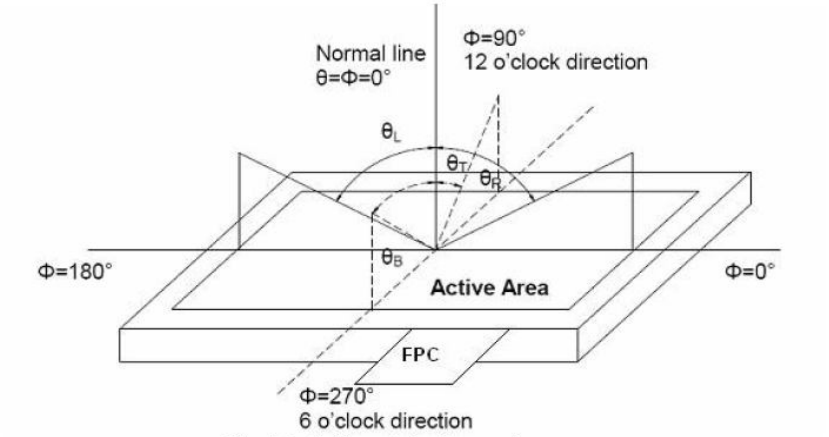


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

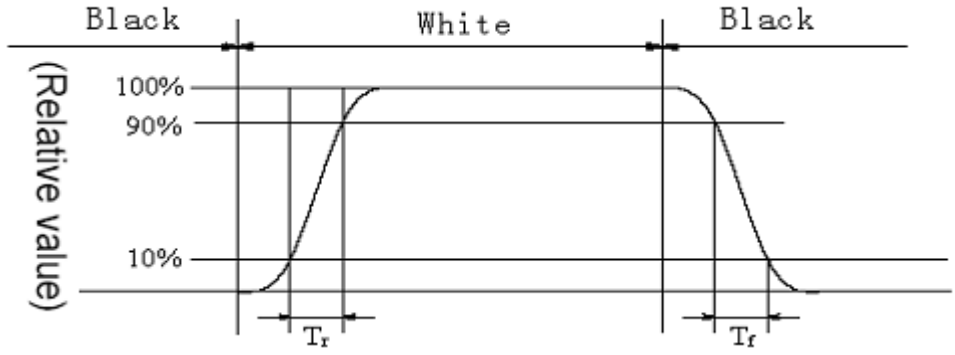
"White state ": The state is that the LCD should driven by Vwhite.

"Black state": The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

7 Environmental / Reliability Tests

No	Test Item	Condition	Remark
1	High Temperature Operation	Ts=+70℃, 240hrs	IEC60068-2-1:2007,GB2423.2-2008
2	Low Temperature Operation	Ta=-20℃,240hrs	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta=+80℃, 240hrs	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	Ta=-30℃, 240hrs	IEC60068-2-1:2007 GB2423.1-2008
5	High Temperature & High Humidity Storage	Ta=+60℃, 90% RH 240 hours	Note2 IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (Non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 20 Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total)(Package condition)	IEC60068-2-6:1982 GB/T2423.10—1995
8	Shock (Non-operation)	60G 6ms, ± X,± Y,± Z 3times, for each direction	IEC60068-2-27:1987 GB/T2423.5—1995
9	Package Drop Test	Height:60 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32:1990 GB/T2423.8—1995

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of samples.

Note3: In the standard condition,there is not display function NG issue occurred.All the cosmetic specification is judged before the reliability stress.

8 Packing Form

-TBD

9. Precautions for Use of LCD

9.1. Handling Precautions

9.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

9.1.5. Do not attempt to disassemble the LCD.

9.1.6. If the logic circuit power is off, do not apply the input signals.

9.1.7. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

9.1.7.1. Be sure to ground the body when handling the LCD.

9.1.7.2. Tools required for assembly, such as soldering irons, must be properly ground.

9.1.7.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

9.2. Storage precautions

9.2.1. When storing the LCD, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2. The LCD should be stored under the storage temperature range. If the LCD will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

9.2.3. The LCD should be stored in the room without acid, alkali and harmful gas.

9.3. Transportation Precautions:

The LCD should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.