TLV61225 Single-Cell High-Efficient Step-Up Converter in 6-Pin SC-70 Package

1 Features

- Up to 94% Efficiency at Typical Operating Conditions
- 5-µA Quiescent Current
- Operating Input Voltage from 0.7 V to 3.3 V
- Pass-Through Function During Shutdown
- Output Current of More Than 40-mA From a 1.2-V Input
- Typical Switch Current Rating 400 mA
- Output Overvoltage Protection
- Overtemperature Protection
- Fixed 3.3-V Output Voltage
- Small 6-Pin SC-70 Package

2 Applications

- Battery-Powered Applications
  - 1- to 2- Cell NiMH or Alkaline
  - 1-Cell Li-Primary
- Consumer and Portable Medical Products
- Personal Care Products

3 Description

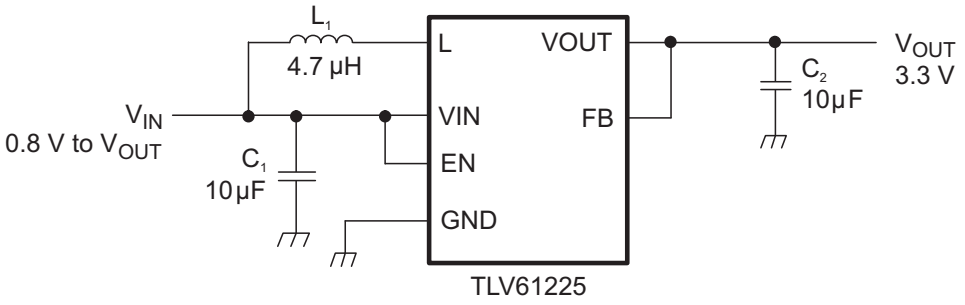
The TLV61225 device provides a power-supply solution for products powered by either a single-cell or 2-cell alkaline or NiMH, or 1-cell Li-primary battery. Possible output currents depend on the input-to-output voltage ratio. The boost converter is based on a hysteretic controller topology using synchronous rectification to obtain maximum efficiency at minimal quiescent currents. The output voltage of this device is set internally to a fixed output voltage of 3.3 V. The converter can be switched off by a featured enable pin. While being switched off, battery drain is minimized. The device is offered in a 6-pin SC-70 package (DCK) measuring 2 mm × 2 mm to enable small circuit layout size.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV61225	SOT (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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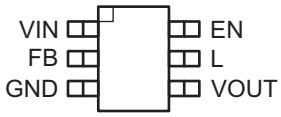
4 Revision History

Changes from Original (August 2010) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DCK Package
6-Pin SOT
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	6	I	Enable input (1: enabled, 0: disabled). Must be actively tied high or low.
FB	2	I	Output voltage sense input. Must be connected to V_{OUT}.
GND	3	—	Control / logic and power ground
L	5	I	Connection for Inductor
VIN	1	I	Boost converter input voltage
VOUT	4	O	Boost converter output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, L, VOUT, EN, FB	–0.3	7.5	V
Temperature	Operating junction temperature, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	
		Machine model (MM)	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply voltage at VIN	0.7	3.3	V
T_A	Operating free air temperature	–40	85	°C
T_J	Operating virtual junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLV61225 DCK (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE							
V_{IN}	Input voltage range			0.7		3.3	V
V_{IN}	Maximum minimum input voltage for start-up		$R_{Load} \geq 150\ \Omega$, $T_A = 25°C$		0.7		V
V_{OUT}	TLV61225 output voltage		$V_{IN} < V_{OUT}$	3.13	3.3	3.43	V
I_{LH}	Inductor current ripple				200		mA
I_{SW}	switch current limit		V_{OUT} = 3.3 V, V_{IN} = 1.2 V	160	400		mA
R_{DSon_HSD}	Rectifying switch ON-resistance		V_{OUT} = 3.3 V		1000		mΩ
R_{DSon_LSD}	Main switch ON-resistance		V_{OUT} = 3.3 V		600		mΩ
	Line regulation		$V_{IN} < V_{OUT}$		0.5%		
	Load regulation		$V_{IN} < V_{OUT}$		0.5%		
I_Q	Quiescent current	V_{IN}	I_O = 0 mA, $V_{EN} = V_{IN}$ = 1.2 V, V_{OUT} = 3.3 V		0.5	1	µA
		V_{OUT}			5	10	µA
I_{SD}	Shutdown current	V_{IN}	V_{EN} = 0 V, V_{IN} = 1.2 V, $V_{OUT} \geq V_{IN}$		0.2	1	µA
I_{LKG_VOUT}	Leakage current into VOUT		V_{EN} = 0 V, V_{IN} = 1.2 V, V_{OUT} = 3.3 V		1		µA
I_{LKG_L}	Leakage current into L		V_{EN} = 0 V, V_{IN} = 1.2 V, V_L = 1.2 V, $V_{OUT} \geq V_{IN}$		0.01	0.7	µA
I_{EN}	EN input current		Clamped on GND or V_{IN} (V_{IN} < 1.5 V)		0.005	0.1	µA
CONTROL STAGE							
V_{IL}	Maximum EN input low voltage		$V_{IN} \leq 1.5$ V	0.2 × V_{IN}			V
V_{IH}	Minimum EN input high voltage		$V_{IN} \leq 1.5$ V			0.8 × V_{IN}	V
V_{IL}	Maximum EN input low voltage		$V_{IN} > 1.5$ V		0.4		V
V_{IH}	Minimum EN input high voltage		$V_{IN} > 1.5$ V		1.2		V
V_{UVLO}	Undervoltage lockout threshold for turnoff		V_{IN} decreasing		500		mV
	Undervoltage lockout hysteresis				50		mV
	Overvoltage protection threshold			5.5		7.5	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

6.6 Dissipation Ratings

PACKAGE	POWER RATING $T_A \leq 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
DCK	444 mW	4.44 mW/°C

6.7 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Minimum of Maximum Output Current	vs Input Voltage	Figure 1
Efficiency	vs Output Current, V_{IN} = [1.2 V; 2.4 V; 3 V]	Figure 2
	vs Input Voltage, I_{OUT} = [100 uA; 1 mA; 10 mA; 50 mA]	Figure 3
Input Current	vs Input Voltage at No Output Load, Device Enabled	Figure 4
Output Voltage	vs Output Current, V_{IN} = [1.2 V; 2.4 V]	Figure 5
	vs Input Voltage, Device Disabled, R_{LOAD} = [1 kΩ; 10 kΩ]	Figure 6

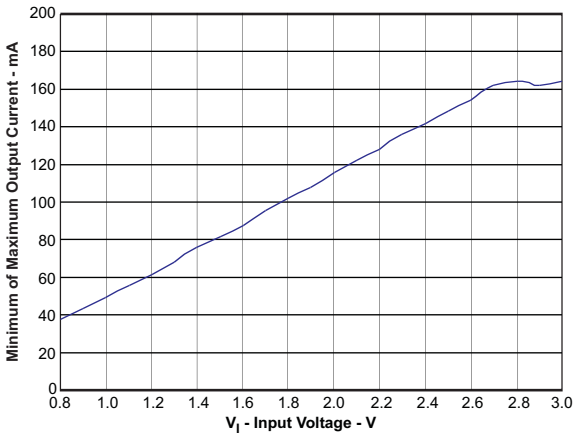


Figure 1. Minimum of Maximum Output Current vs Input Voltage

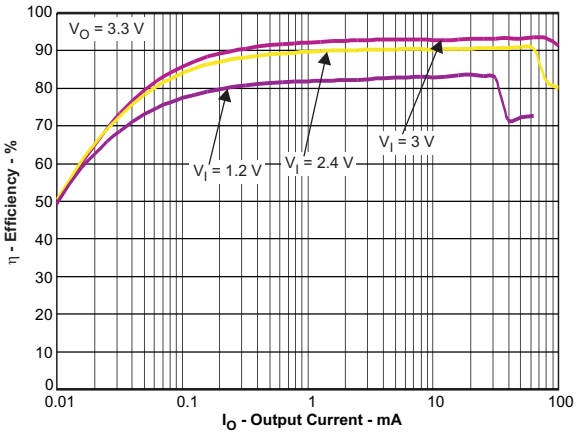


Figure 2. Efficiency vs Output Current

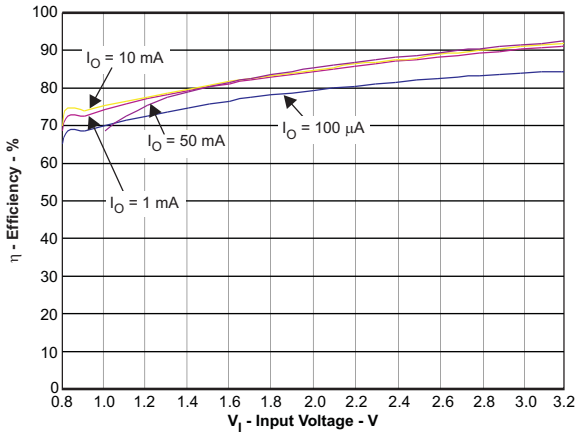


Figure 3. Efficiency vs Input Voltage

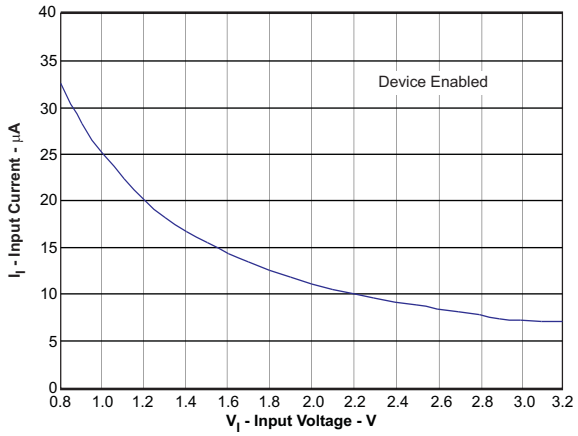


Figure 4. No Load Application Input Current vs Input Voltage

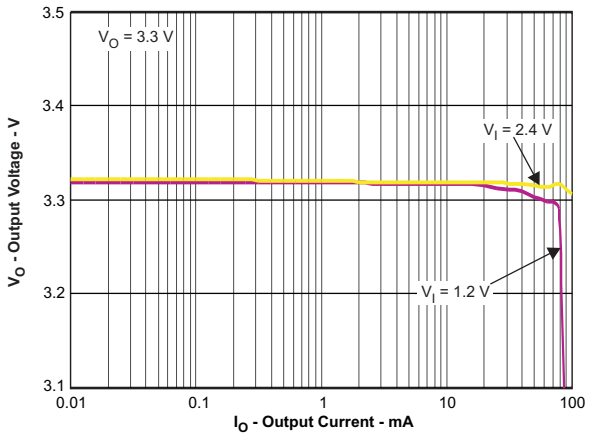


Figure 5. Output Voltage vs Output Current

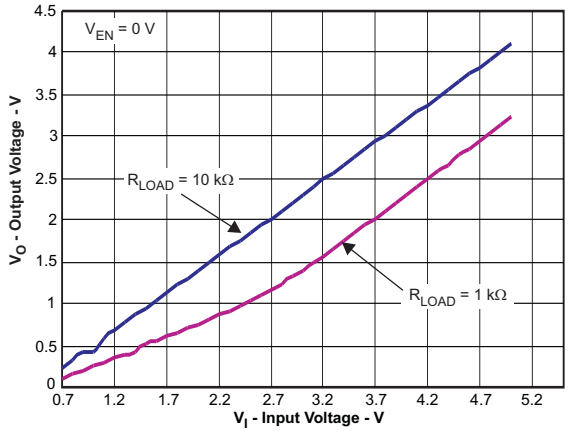


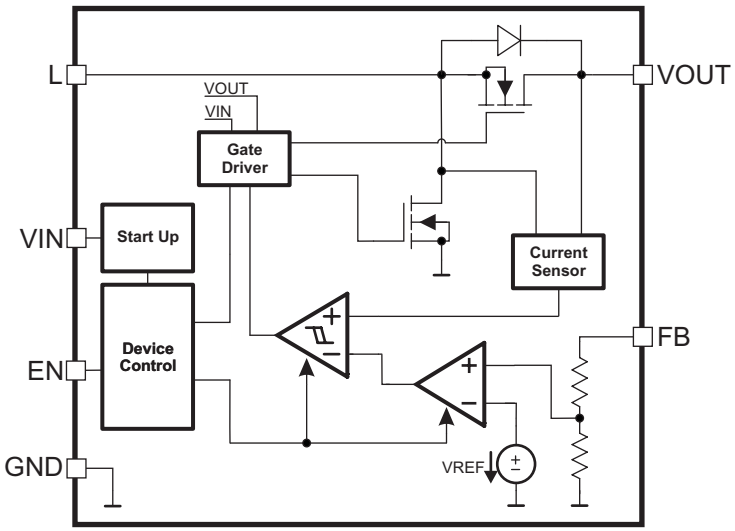
Figure 6. Output Voltage vs Input Voltage, Device Disabled

7 Detailed Description

7.1 Overview

The TLV61225 device is a high-performance, high-efficient family of switching boost converters. To achieve high efficiency the power stage is implemented as a synchronous boost topology. Two actively controlled low R_{DSon} power MOSFETs are used to achieve power switching.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Controller Circuit

The device is controlled by a hysteretic current-mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 200 mA and adjusting the offset of this inductor current depending on the output load. If the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current becomes discontinuous to keep the efficiency high at low load conditions.

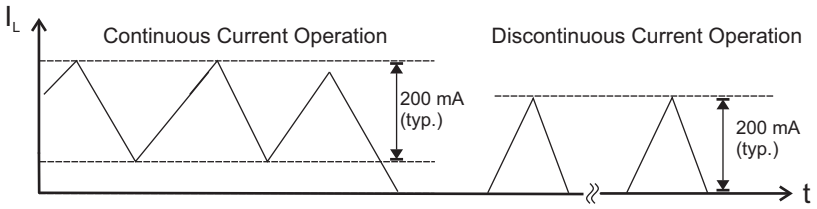


Figure 7. Hysteretic Current Operation

The output voltage V_{OUT} is monitored through the internal feedback network, which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly.

Feature Description (continued)

7.3.2 Start-Up

After the EN pin is tied high, the device starts to operate. If the input voltage is not high enough to supply the control circuit properly, a start-up oscillator starts to operate the switches. During this phase the switching frequency is controlled by the oscillator and the maximum switch current is limited. As soon as the device has built up the output voltage to about 1.8 V (high enough for supplying the control circuit) the device switches to its normal hysteretic current mode operation. The start-up time depends on input voltage, load current and output capacitance.

7.3.3 Operation at Output Overload

If the inductor current is in normal boost operation, the current reaches the internal switch current limit threshold. When the threshold is reached, the main switch is turned off to stop further increase of the input current.

The output voltage decreases because with limited input current is no longer possible to provide sufficient power to the output to maintain the programmed output voltage.

If the output voltage drops below the input voltage, the back-gate diode of the rectifying switch gets forward-biased and current starts flowing through it. This diode cannot be turned off, so the current finally is only limited by the remaining DC resistances. As soon as the output load decreases to a value the converter can supply, the converter resumes normal operation providing the set output voltage.

7.3.4 Undervoltage Lockout

An implemented undervoltage lockout function (UVLO) stops the operation of the converter if the input voltage drops below the typical UVLO threshold. This function is implemented to prevent malfunctioning of the converter and protect batteries against deep discharge.

7.3.5 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore, overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the TLV61225 output voltage is also monitored internally. If the output voltage of the device reaches the internally programmed threshold, the voltage amplifier regulates the output voltage to this value.

7.3.6 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC junction temperature. If the temperature exceeds the programmed threshold (see *Electrical Characteristics*), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. To prevent unstable operation close to the region of overtemperature threshold, a built-in hysteresis is implemented.

7.4 Device Functional Modes

7.4.1 Device Enable and Shutdown Modes

The device is enabled when the EN pin is set high and shut down when the EN pin is low. During shutdown, the converter stops switching and all internal control circuitry is turned off. In this case, the input voltage is connected to the output through the back-gate diode of the rectifying MOSFET. This means that voltage will always exist at the output, which can be as high as the input voltage or lower depending on the load.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV61225 is intended for systems which are powered by a single-cell battery to up to two Alkaline, NiCd, or NiMH cells with a typical terminal voltage from 0.7 V to 3.3 V and can output 3.3-V voltage. Additionally, any other voltage source with a typical output voltage from 0.7 V to 3.3 V can be used with the TLV61225.

8.2 Typical Application

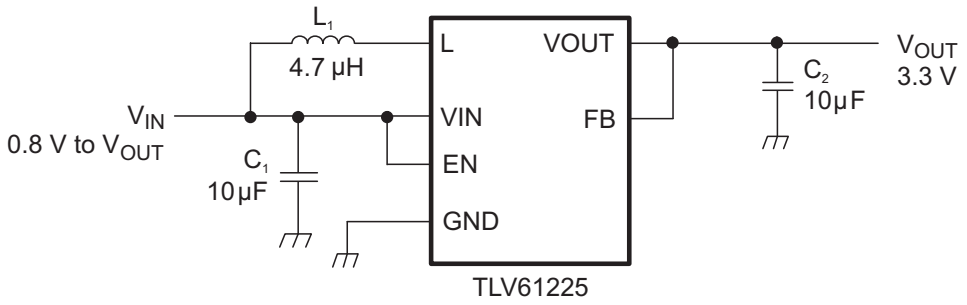


Figure 8. Typical Application Schematic

8.2.1 Design Requirements

In this example, TLV61225 is used to design a 3.3-V power supply with up to 15-mA output current capability. The TLV61225 can be powered by a single-cell battery to up to two Alkaline, NiCd or NiMH cells with a typical terminal voltage from 0.7 V to 3.5 V. In this example, the input voltage range is from 0.8 V to 1.5 V for single-cell Alkaline battery input design.

Table 2. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_1	GRM188R60J106ME84D	Murata	10 µF, 6.3 V
C_2	GRM188R60J106ME84D	Murata	10 µF, 6.3 V
L_1	EPL3015-472MLB	Coilcraft	4.7 µH

8.2.2 Detailed Design Procedure

8.2.2.1 Programming the Output Voltage

At fixed voltage versions, the output voltage is programmed by an internal resistor divider. The FB pin is used to sense the output voltage. To configure the devices properly, the FB pin must be connected directly to VOUT.

8.2.2.2 Inductor Selection

To make sure that the TLV61225 devices can operate, a suitable inductor must be connected between pin VIN and pin L. Inductor values of 4.7 µH show good performance over the whole input and output voltage range.

Due to the fixed inductor current ripple control the switching frequency is defined by the inductor value. For a given switching frequency, input and output voltage the required inductance can be estimated using Equation 1.

$$L = \frac{1}{f \times 200\ mA} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \quad (1)$$

Using inductor values greater than 4.7 µH can improve efficiency because higher values cause lower switching frequency and less switching losses. TI does not recommend using inductor values below 2.2 µH.

To ensure reliable operation of the TLV61225 under all load conditions, TI recommends using inductors with a current rating of 400 mA or higher. This will cover normal operation including current peaks during line and load transients.

Table 3 lists the inductor series from different suppliers have been used with the TLV61225 converter:

Table 3. List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	EPL3015
	EPL2010
Murata	LQH3NP
Tajo Yuden	NR3015
Wurth Elektronik	WE-TPC Typ S

8.2.2.3 Capacitor Selection

8.2.2.3.1 *Input Capacitor*

TI recommends using at least a 10-µF input capacitor to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. TI also recommends placing a ceramic capacitor placed as close as possible to the VIN and GND pins of the IC.

8.2.2.3.2 *Output Capacitor*

For the output capacitor C_2 ,TI recommends using small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. There are no minimum output capacitor ESR requirements for maintaining control loop stability. If the application requires the use of large capacitors which cannot be placed close to the IC, TI recommends using a small ceramic capacitor with an capacitance value in the range of 2.2µF in parallel to the large capacitor. Place this small capacitor as close as possible to the VOUT and GND pins of the IC.

A minimum capacitance value of 4.7 µF should be used, TI recommends using 10 µF. To calculate the required output capacitance in case an inductor with a value higher than 4.7 µH has been selected Equation 2 can be used.

$$C_2 \geq \frac{L}{2} \times \frac{\mu F}{\mu H} \quad (2)$$

8.2.3 Application Curves

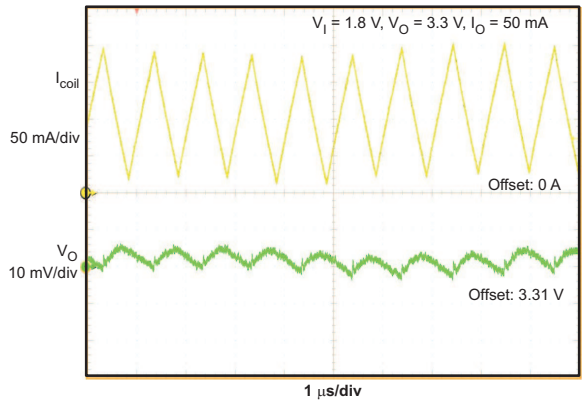


Figure 9. Output Voltage Ripple

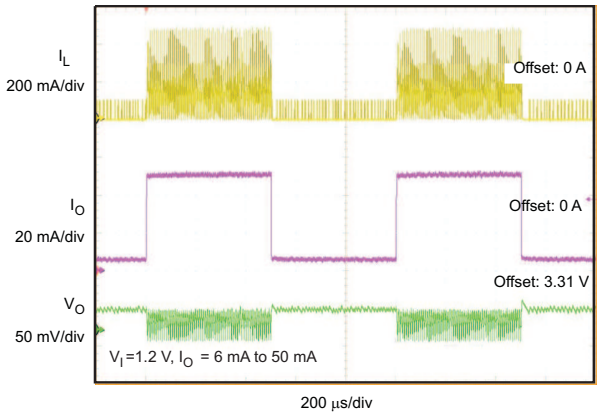


Figure 10. Load Transient Response

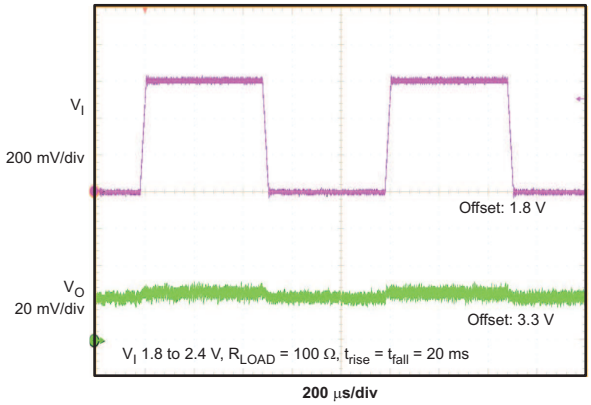


Figure 11. Line Transient Response

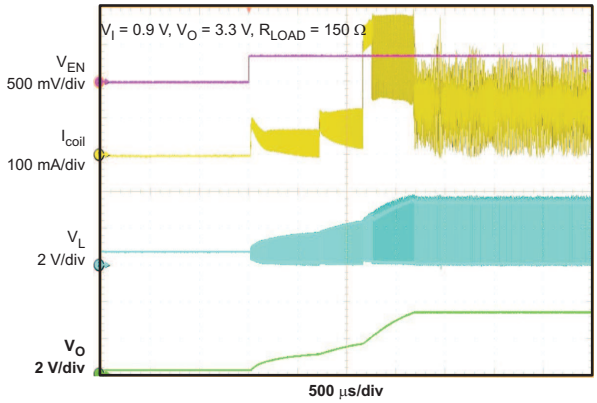


Figure 12. Output Voltage vs Output Current and Input Voltage

9 Power Supply Recommendations

The power supply can be 1-cell or 2-cell alkaline, NiCd or NiMH batteries.

The input supply should be well regulated with the rating of TLV61225. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

To lay out the ground, TI recommended using short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. Assure that the ground traces are connected close to the device GND pin.

10.2 Layout Example

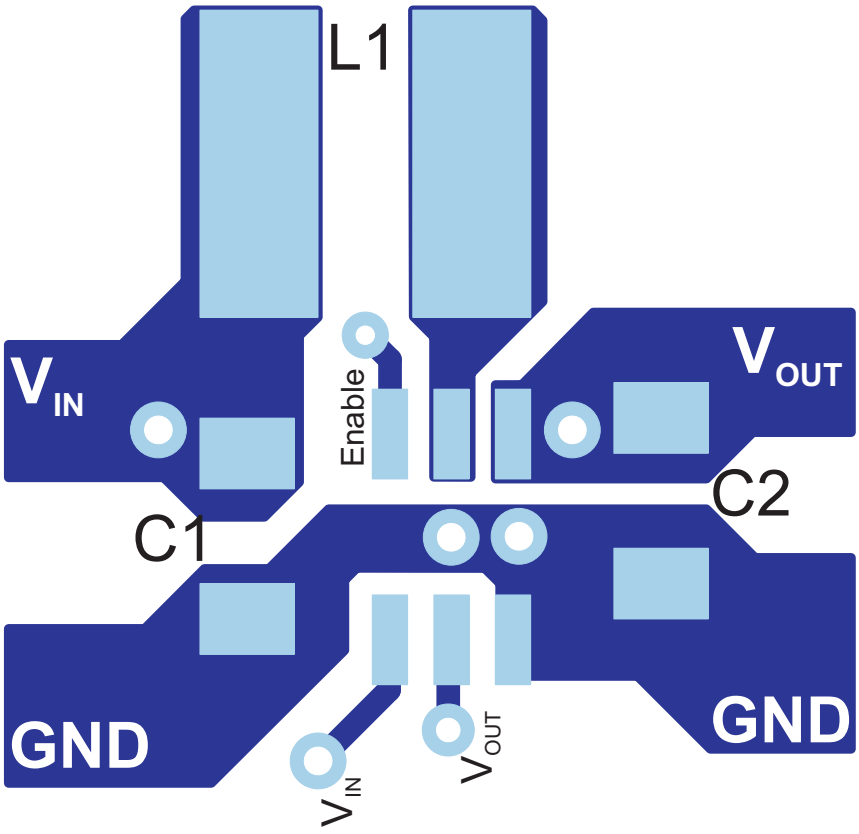


Figure 13. PCB Layout Suggestion

10.3 Thermal Consideration

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table, check the *Thermal Characteristics Application Note* (SZZA017) and the *Semiconductor and IC Package Thermal Metrics Application Note* (SPRA953).

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Thermal Characteristics Application Note*, SZZA017

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV61225DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	QUL	Samples
TLV61225DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	QUL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

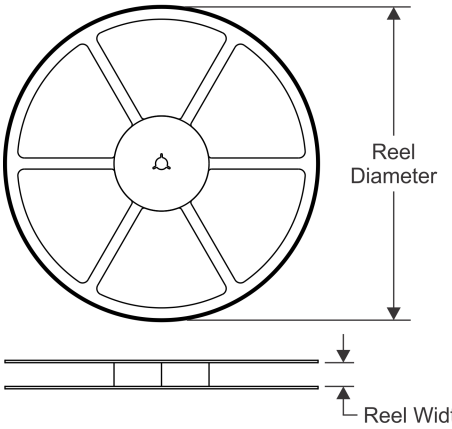
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

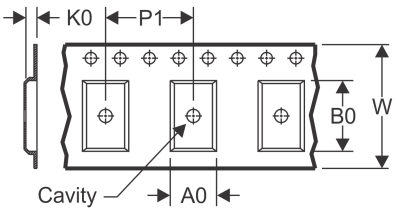
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

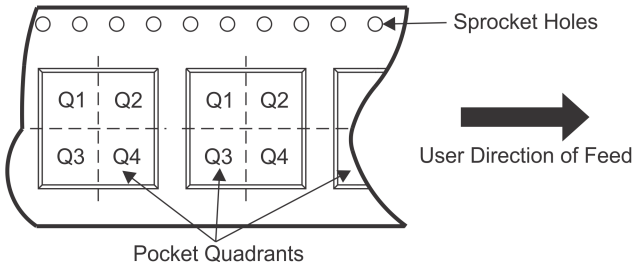


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

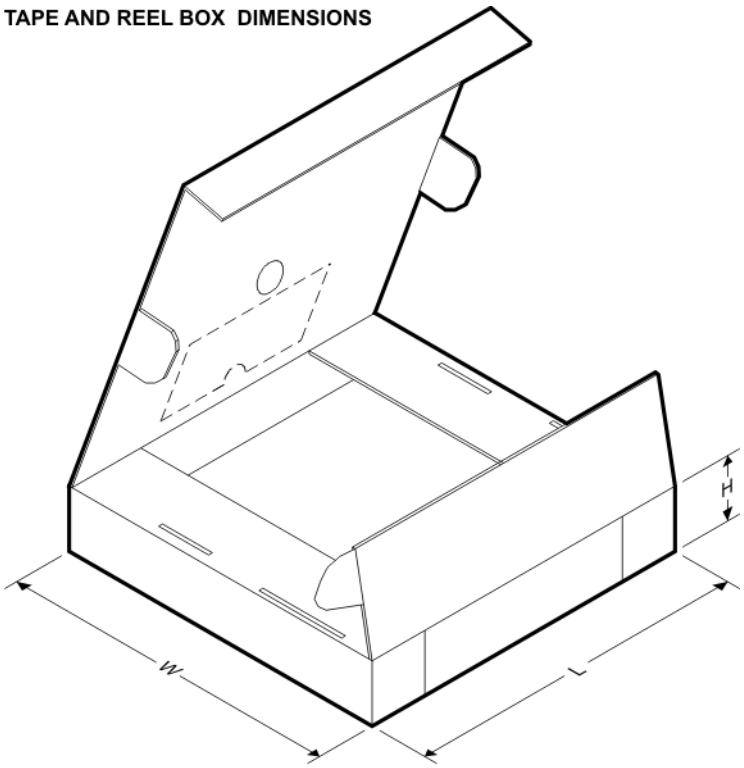
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV61225DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV61225DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

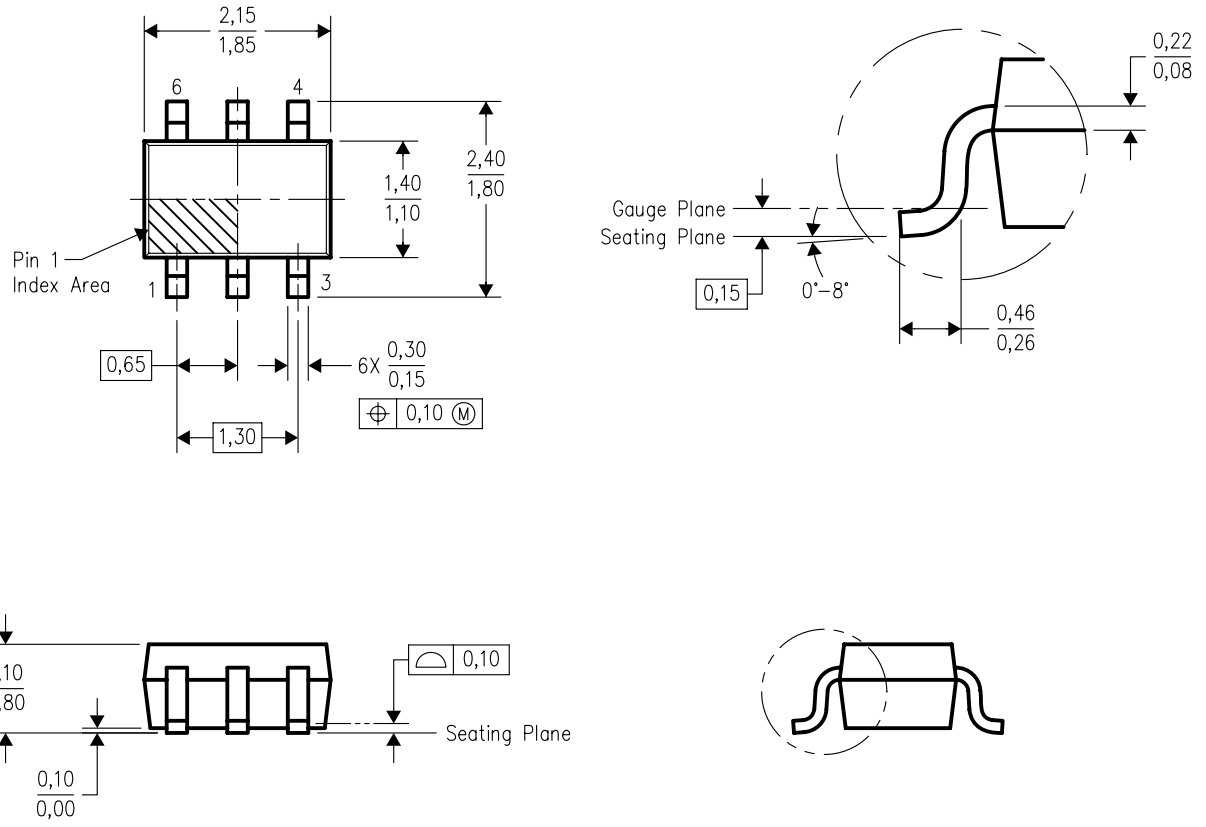
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV61225DCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV61225DCKT	SC70	DCK	6	250	203.0	203.0	35.0

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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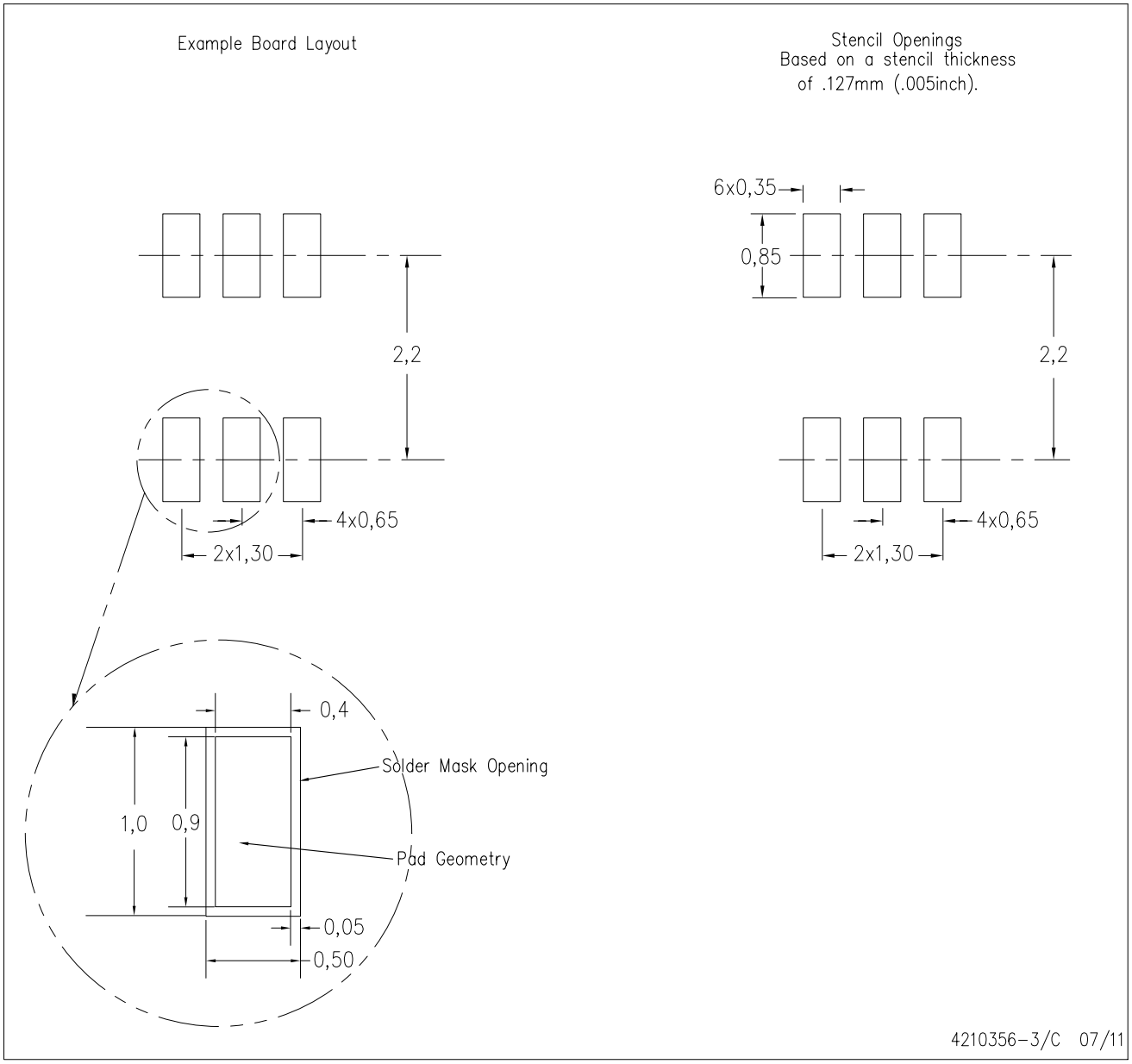
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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