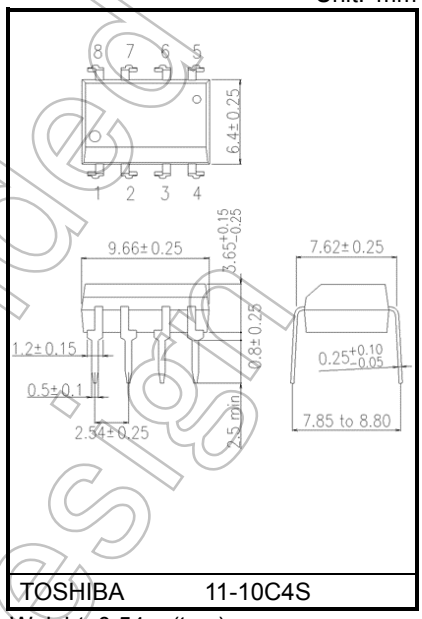
TOSHIBA Photocoupler IRED & Photo IC

TLP558

Isolated Bus Driver
High Speed Line Receiver
Microprocessor System Interfaces
MOS FET Gate Driver
Transistor Inverter

Unit: mm

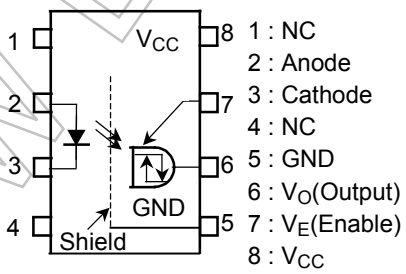


Weight: 0.54 g (typ.)

The TOSHIBA TLP558 consists of an infrared emitting diode and integrated high gain, high speed photodetector.
This unit is 8-lead DIP package.
The detector has a three state output stage that provides source drive and sink drive, and built-in schmitt trigger. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V / μs.
TLP558 is inverter logic type. For buffer logic type, TLP555 is in line-up.

- Input current: I_F=1.6 mA (max)
- Power supply voltage: V_{CC}=4.5 to 20 V
- Switching speed: t_{pHL}, t_{pLH}=400ns (max)
- Common mode transient immunity: ±1000V/μs (min)
- Guaranteed performance over temperature: -25 to 85°C
- Isolation voltage: 2500V_{rms} (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

Pin Configuration (top view)



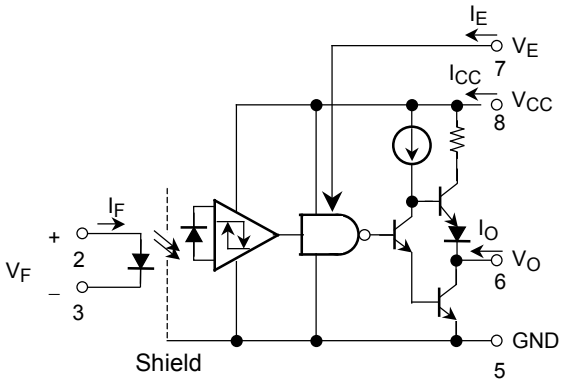
1 : NC
2 : Anode
3 : Cathode
4 : NC
5 : GND
6 : V_O(Output)
7 : V_E(Enable)
8 : V_{CC}

Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	Z
L	L	Z

A 0.1μF bypass capacitor must be connected between pins 8 and 5.

Schematic



Start of commercial production
1987-05

Absolute Maximum Ratings

Characersitic			Symbol	Rating	Unit
LED	Forward current		I_F	10	mA
	Peak transient forward current	(Note 1)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Diode power dissipation		P_D	45	mW
Detector	Output current		I_O	40 / -25	mA
	Peak output current	(Note 2)	I_{OP}	80 / -50	mA
	Output voltage		V_O	-0.5 to 20	V
	Supply voltage		V_{CC}	-0.5 to 20	V
	Three state enabel voltage		V_E	-0.5 to 20	V
	Output power dissipation		P_O	100	mW
	Output power dissipation derating (Ta > 70 °C)		ΔPO/ΔTa	-1.8	mW/°C
	Total package power dissipation		P_T	200	mW
	Total package power dissipation derating (Ta > 70 °C)		ΔPT/ΔTa	-3.6	mW/°C
Operating temperature range			T_{opr}	-40 to 85	°C
Storage temperature range			T_{stg}	-55 to 125	°C
Lead solder temperature(10 s)		(Note 3)	T_{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %, Ta=25°C)		(Note 4)	BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width ≤ 1 μs, 300 pps.

Note 2: Pulse width ≤ 5μ s, duty ratio ≤ 0.025.

Note 3: 1.6 mm below seating plane.

Note 4: Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, on	$I_{F(ON)}$	2 (Note 1)	—	5	mA
Input voltage, off	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage	V_{CC}	4.5	—	20	V
Enable voltage high	V_{EH}	2.0	—	20	V
Enable voltage low	V_{EL}	0	—	0.8	V
Fan out(TTL load)	N	—	—	4	—
Operating temperature	T_{opr}	-25	—	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: 2 mA condition permits at least 20 % CTR degradation guardband.
Initial switching threshold is 1.6 mA or less.

Electrical Characteristics (unless otherwise specified, Ta = -25 to 85°C, V_{CC} = 4.5 to 20V)

Characteristic	Symbol	Test Condition		Min	Typ.	Max	Unit
Input forward voltage	V_F	I_F = 5 mA, Ta = 25 °C		—	1.55	1.7	V
Temperature coefficient of forward voltage	$\Delta V_F / \Delta Ta$	I_F = 5 mA		—	-2.0	—	mV / °C
Input reverse current	I_R	V_R = 5 V, Ta = 25 °C		—	—	10	μA
Input capacitance	C_T	V_F = 0 V, f = 1 MHz, Ta = 25 °C		—	45	—	pF
Output leakage current (V_O > V_{CC})	I_{OHH}	V_F = 0 V, V_{CC} = 4.5 V	V_O = V_E = 5.5 V	—	—	100	μA
			V_O = V_E = 20 V	—	0.01	500	
Logic low output voltage	V_{OL}	I_{OL} = 6.4 mA, I_F = 1.6 mA, V_E = 2 V		—	0.4	0.5	V
Logic high output voltage	V_{OH}	I_{OH} = -2.6 mA, V_F = 0.8 V, V_E = 2 V		2.4	3.3	—	V
Logic low enable current	I_{EL}	V_E = 0.4 V		—	-0.13	-0.32	mA
Logic high enable current	I_{EH}	V_E = 2.7 V		—	—	20	μA
		V_E = 5.5 V		—	—	100	
		V_E = 20 V		—	0.01	250	
Logic low enable voltage	V_{EL}	—		—	—	0.8	V
Logic high enable voltage	V_{EH}	—		2.0	—	—	V
Logic low supply current	I_{CCL}	I_F = 5 mA	V_{CC} = V_E = 5.5 V	—	4.0	6.0	mA
			V_{CC} = V_E = 20 V	—	4.6	7.5	
Logic high supply current	I_{CCH}	V_F = 0 V	V_{CC} = V_E = 5.5 V	—	4.2	6.0	mA
			V_{CC} = V_E = 20 V	—	4.7	7.5	
High impedance state output current	I_{OZL}	V_F = 0 V, V_E = 0.8 V	V_O = 0.4 V	—	—	-20	μA
	I_{OZH}	I_F = 5 mA, V_E = 0.8 V	V_O = 2.4 V	—	—	20	
			V_O = 5.5 V	—	—	100	
			V_O = 20 V	—	1	500	
Logic low short circuit output current (Note 1)	I_{OSL}	I_F = 5 mA, V_E = 2 V	V_O = V_{CC} = 5.5 V	25	55	—	mA
			V_O = V_{CC} = 20 V	40	80	—	
Logic high short circuit output current (Note 1)	I_{OSH}	V_F = 0 V, V_O = GND, V_E = 2 V	V_{CC} = 5.5 V	-10	-25	—	mA
			V_{CC} = 20 V	-25	-60	—	
Input current logic low output	I_{FL}	V_E = 2 V, I_O = 6.4 mA, V_O < 0.4 V		—	0.4	1.6	mA
Input voltage logic high output	V_{FH}	V_E = 2 V, I_O = -2.6 mA, V_O > 2.4 V		0.8	—	—	V
Input current hysteresis	I_{HYS}	V_{CC} = V_E = 5 V		—	0.05	—	mA
Resistance (input-output)	R_S	V_S = 500 V, R.H. ≤60 %, Ta = 25 °C (Note 2)		5×10^{10}	10^{14}	—	Ω
Capacitance(input-output)	C_S	V_S = 0 V, f = 1 MHz, Ta = 25 °C (Note 2)		—	1.0	—	pF

Note: All typical values are at Ta = 25 °C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Note 1: Duration of output short circuit time should not exceed 10 ms.

Note 2: Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (unless otherwise specified, V_{CC} = 4.5 to 20V, Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to logic high output (Note 1)	t_{pLH}	1	I_F = 3→ 0 mA	—	250	400	ns
Propagation delay time to logic low output (Note 1)	t_{pHL}		I_F = 0→ 3 mA	—	270	400	ns
Output rise time (10-90%)	t_r		I_F = 3→ 0 mA, V_{CC} = 5 V	—	35	75	ns
Output fall time (90-10%)	t_f		I_F = 0→ 3 mA, V_{CC} = 5 V	—	20	75	ns
Common mode transient immunity at logic high output (Note 2)	C_{MH}	3	I_F = 0 mA, V_{CM} = 50 V $V_{O\ (Min)}$ = 2 V	1000	—	—	V / μs
Common mode transient immunity at logic low output (Note 2)	C_{ML}		I_F = 1.6 mA, V_{CM} = 50 V $V_{O\ (Max)}$ = 0.8 V	-1000	—	—	V / μs

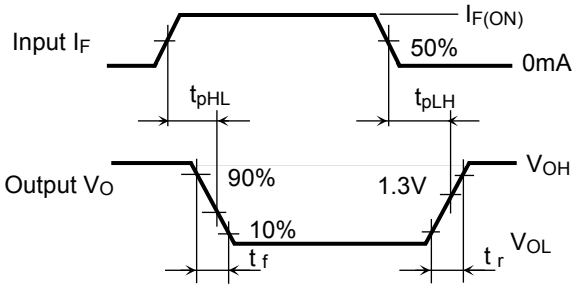
Note: All typical values are at Ta = 25 °C, V_{CC} = 5 V

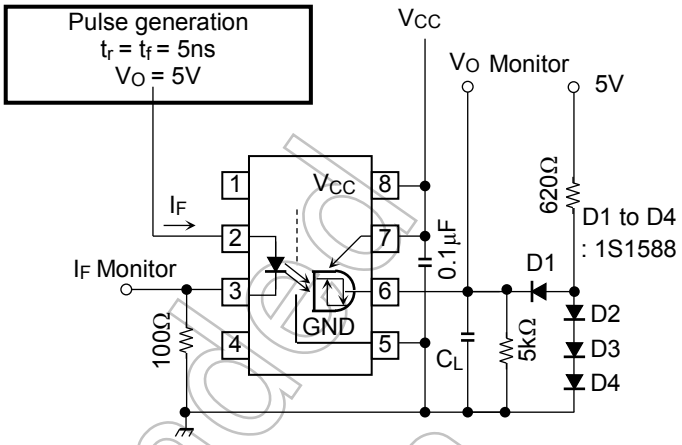
Note: A ceramic capacitor (0.1 μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

Note 1: The t_{pLH} propagation delay is measured from the 50 % point on the trailing edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{pHL} propagation delay is measured from the 50 % point on the leading edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.

Note 2: C_{ML} is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V).
C_{MH} is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic state (V_O > 2.0 V).

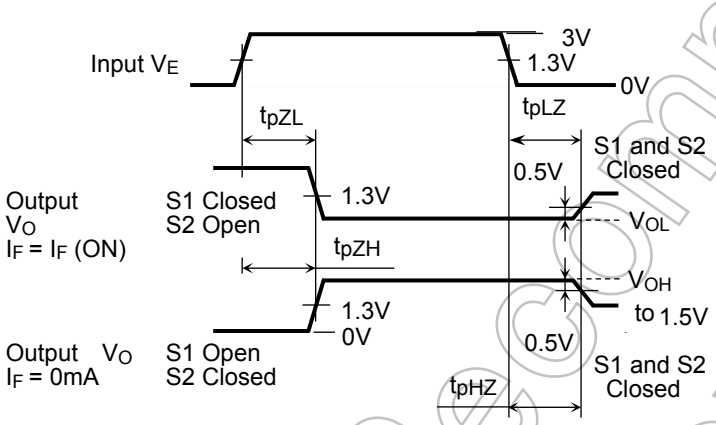
Test Circuit 1: t_{pLH}, t_{pHL}, t_r and t_f

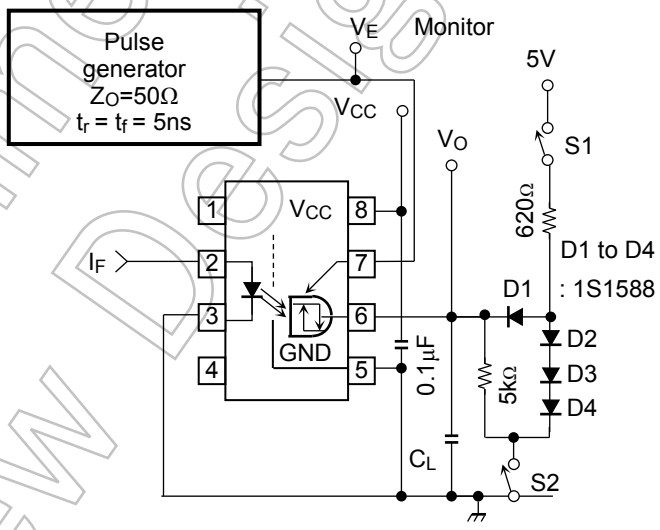




C_L is approximately 15pF which includes probe and stray wiring capacitance.

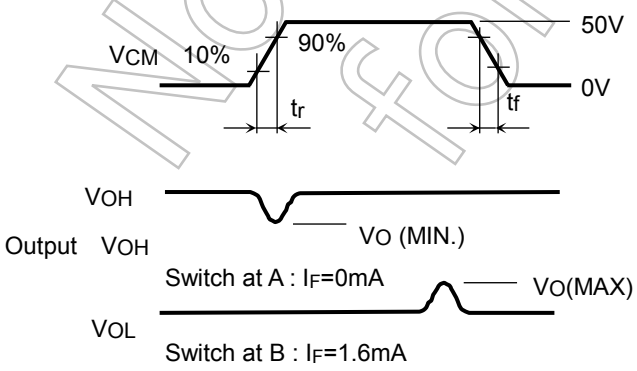
Test Circuit 2: t_{pHZ}, t_{pZH}, t_{pLZ} and t_{pZL}



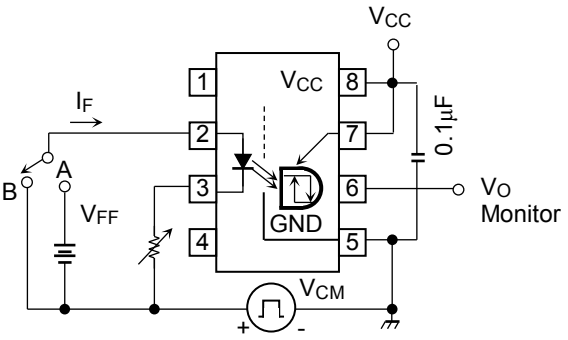


C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 3: Common Mode Transient Immunity



$$CM_H = \frac{45(V)}{tf(\mu s)}\ ,\ CM_L = \frac{45(V)}{tf(\mu s)}$$



Pulse generator
Z_O =50Ω

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