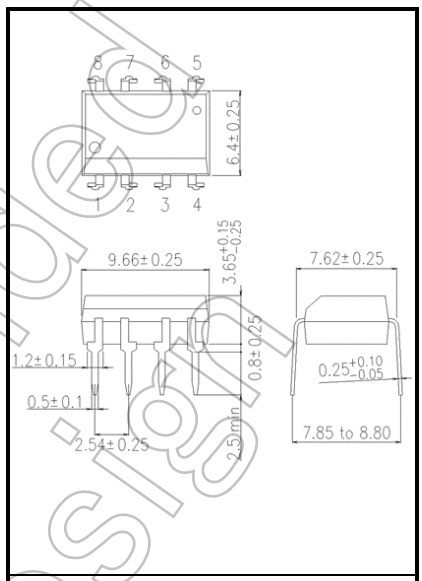
Photocouplers IRED & Photo ICTLP555

TLP555

○ Isolated Bus Driver
○ High Speed Line Receiver
○ Microprocessor System Interfaces
○ MOS FET Gate Driver
○ Transistor Inverter

Unit : mm



JEDEC	—
JEITA	—
TOSHIBA	11−10C4S

Weight: 0.54 g (typ.)

The TOSHIBA TLP555 consists of an infrared emitting diode and integrated high gain, high speed photodetector.
This unit is 8−lead DIP package.

The detector has a three state output stage that eliminates the need for pull−up resistor, and built−in Schmitt trigger. The detector has a Schmitt trigger circuit and 3 State output circuit, so both-directions of source and sink drive can be performed.

The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V / μs.

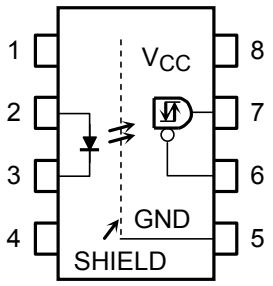
TLP555 is a buffer logic type. When an inverter logic type is required, there is TLP558.

- Input current : I_F = 1.6 mA (max.)
- Power supply voltage : V_{CC} = 4.5 to 20 V
- Switching speed : t_{pHL}、t_{pLH} = 400 ns (max.)
- Common mode transient immunity : ±1000V / μs (Min.)
- Guaranteed performance over temperature : −25 to 85°C
- Isolation voltage : 2500 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
  File No.E67349

Truth Table (positive logic)

Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

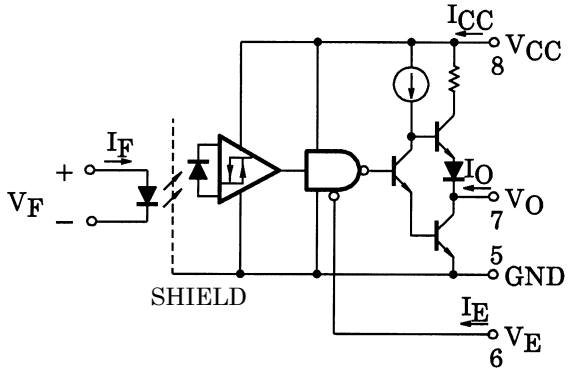
Pin Configuration (top view)



1: N.C.
2: Anode
3: Cathode
4: N.C.
5: GND
6: V_E (enable)
7: V_O (output)
8: V_{CC}

Start of commercial production
1986-07

Schematic



Note : 0.1-μF bypass capacitor must be connected between pin 8 and pin 5.

Absolute Maximum Ratings (Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
LED	Input forward current	I_F	10	mA
	Peak transient input forward current (Note 1)	I_{FPT}	1	A
	Input reverse voltage	V_R	5	V
	Input power dissipation(Ta= to 85°C)	P_D	45	mW
Detector	Output current	I_O	40 / −25	mA
	Peak output current (Note 2)	I_{OP}	80 / −50	mA
	Output voltage	V_O	−0.5 to 20	V
	Supply voltage	V_{CC}	−0.5 to 20	V
	Three state enable voltage	V_E	−0.5 to 20	V
	Output power dissipation (Note 3)	P_O	100	mW
Common	Total package power dissipation (Note 4)	P_T	200	mW
	Operating temperature range	T_{opr}	−40 to 85	°C
	Storage temperature range	T_{stg}	−55 to 125	°C
	Lead solder temperature (10 s) **	T_{sol}	260	°C
	Isolation voltage (AC 60 s, R.H. ≤ 60 %) (Note 5)	BV_S	2500	Vrms

Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) ≤ 1 μs, 300 pps

Note 2: PW ≤ 5 μs, Duty ≤ 0.025%

Note 3: Derate 1.8 mW / °C above 70 °C ambient temperature.

Note 4: Derate 3.6 mW / °C above 70 °C ambient temperature.

Note 5: Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5,6,7 and 8 shorted together

** : More than 2 mm from the root of a lead.

Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max	Unit
Input on-state current	$I_{F\ (ON)}$	2*	—	5	mA
Input off-state voltage	$V_{F\ (OFF)}$	0	—	0.8	V
Supply voltage	V_{CC}	4.5	—	20	V
Enable voltage high	V_{EH}	2.0	—	20	V
Enable voltage low	V_{EL}	0	—	0.8	V
Fan out (TTL load)	N	—	—	4	—
Operating temperature	T_{opr}	−25	—	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

*:2 mA is a value at the time of taking into consideration 20 % of IFH degradation.

An input hreshold is an initial value and is below 1.6 mA.

Electrical Characteristics

(Unless otherwise specified, Ta = −25 to 85°C、V_{CC} = 4.5 to 20 V)

Characteristics	Symbol	Test Condition		Min.	Typ.(*)	Max	Unit
Input forward voltage	V_F	I_F = 5 mA, Ta = 25 °C		—	1.55	1.7	V
Input forward voltage temperature coefficient	$\Delta V_F / \Delta Ta$	I_F = 5 mA		—	−2.0	—	mV /°C
Input reverse curren	I_R	V_R = 5 V, Ta = 25 °C		—	—	10	μA
Input capacitance	C_T	V_F = 0 V, f = 1 MHz, Ta = 25 °C		—	45	—	pF
Output leakage current ($V_O > V_{CC}$)	I_{OHH}	I_F = 5 mA, V_{CC} = 4.5 V, V_E = GND	V_O = 5.5 V	—	—	100	μA
			V_O = 20 V	—	2	500	
Logic low output voltage	V_{OL}	I_{OL} = 6.4 mA, V_F = 0.8 V, V_E = 0.8 V		—	0.4	0.5	V
Logic high output voltage	V_{OH}	I_{OH} = −2.6 mA, I_F = 1.6 mA, V_E = 0.8 V		2.4	3.3	—	V
Logic low enable current	I_{EL}	V_E = 0.4 V		—	−0.13	−0.32	mA
Logic high enable current	I_{EH}	V_E = 2.7 V		—	—	20	μA
		V_E = 5.5 V		—	—	100	
		V_E = 20 V		—	0.01	250	
Logic low enable voltage	V_{EL}	—		—	—	0.8	V
Logic high enable voltage	V_{EH}	—		2.0	—	—	V
Logic low supply current	I_{CCL}	V_F = 0 V, V_E = GND	V_{CC} = 5.5 V	—	5	6.0	mA
			V_{CC} = 20 V	—	5.6	7.5	
Logic high supply current	I_{CCH}	I_F = 5 mA, V_E = GND	V_{CC} =5.5 V	—	2.5	4.5	mA
			V_{CC} = 20 V	—	2.8	6.0	
High impedance state output current	I_{OZL}	I_F = 5 mA, V_E = 2 V	V_O = 0.4 V	—	1	−20	μA
	I_{OZH}	V_F = 0 V, V_E = 2 V	V_O = 2.4 V	—	—	20	
			V_O = 5.5 V	—	—	100	
			V_O = 20 V	—	0.01	500	
Logic low short circuit output current (Note 6)	I_{OSL}	V_F = 0 V, V_E = 0.8 V	V_O = V_{CC} = 5.5 V	25	55	—	mA
			V_O = V_{CC} = 20 V	40	80	—	
Logic high short circuit output current (Note 6)	I_{OSH}	I_F = 5 mA, V_O = GND, V_E = 0.8V	V_{CC} =5.5 V	−10	−25	—	mA
			V_{CC} = 20 V	−25	−60	—	
Threshold input current (L/H)	I_{FH}	V_E = 0.8 V, I_O = −2.6 mA, V_O > 2.4 V		—	0.4	1.6	mA
Threshold input voltage (H/L)	V_{FL}	V_E = 0.8 V, I_O = 6.4 mA, V_O < 0.4 V		0.8	—	—	V
Input current hysteresis	I_{HYS}	V_{CC} = 5 V, V_E = GND		—	0.05	—	mA
Isolation resistance	R_S	V_S = 500 V, R.H.≤60 % , Ta = 25 °C (Note 5)		5×10^{10}	10^{14}	—	Ω
Total capacitance (input to output)	C_S	V_S = 0 V, f = 1 MHz, Ta = 25 °C (Note 5)		—	1.0	—	pF

* : All typ. values are at Ta = 25 °C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Note 6 : Duration of output short circuit time should not exceed 10 ms.

Switching Characteristics (unless otherwise specified, Ta = 25°C、V_{CC} = 4.5 to 20 V)

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ. (*)	Max.	Unit
Propagation delay time to logic high output level (L →H) (Note 7)	t_{pLH}	1	I_F = 0→3 mA	—	235	400	ns
Propagation delay time to logic low output level (H →L) (Note 7)	t_{pHL}		I_F = 3→0 mA	—	250	400	ns
Output rise time (10–90%)	t_r		I_F = 0→3 mA, V_{CC} = 5 V	—	35	75	ns
Output fall time (90–10%)	t_f		I_F = 3→0 mA, V_{CC} = 5 V	—	20	75	ns
Common mode transient immunity at logic high output (Note 8)	CM_H	3	I_F = 1.6 mA, V_{CM} = 50 V $V_{O\ (min)}$ = 2 V	−1000	—	—	V / μs
Common mode transient immunity at logic low output (Note 8)	CM_L		I_F = 0 mA, V_{CM} = 50 V $V_{O\ (max)}$ = 0.8 V	1000	—	—	V / μs

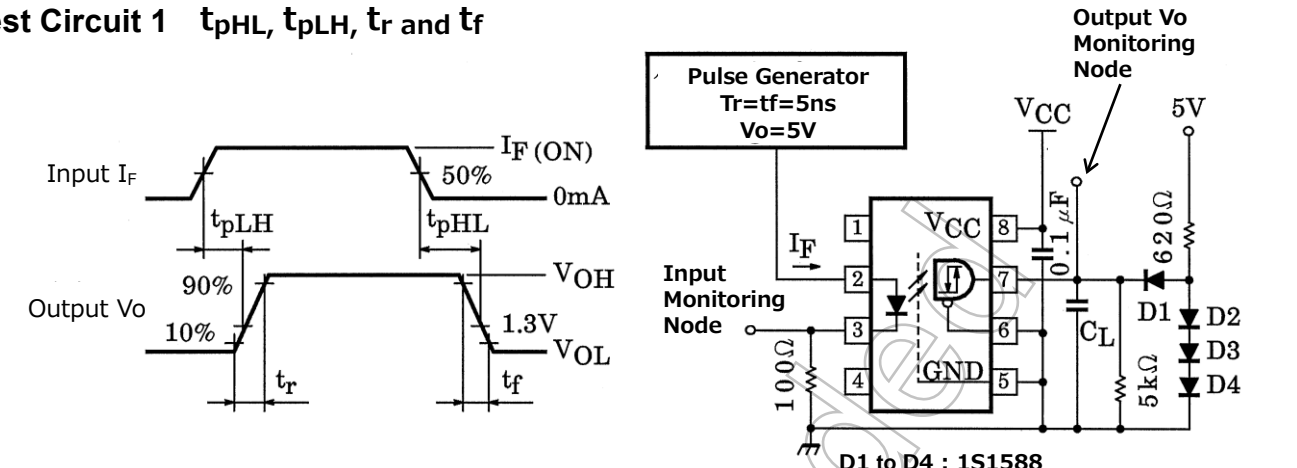
*: All typ. values are at Ta = 25 °C, V_{CC} = 5 V unless otherwise specified.

Note 7: The t_{pLH} propagation delay is measured from the 50 % point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse.
The t_{pHL} propagation delay is measured from the 50 % point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.

Note 8: CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O \leq 0.8$ V).
CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O \geq 2.0$ V).

Note 9: Output photo IC should build in the amplifier of high sensitivity very much, and should attach bypass capacitor 0.1 uF with a sufficient high frequency characteristic to the place within 1 cm from a pin between the pin 8 (VCC) and the pin 5 (GND) as an object for oscillation prevention.
When there is nothing, normal operation of speed, or ON/OFF may not be carried out.

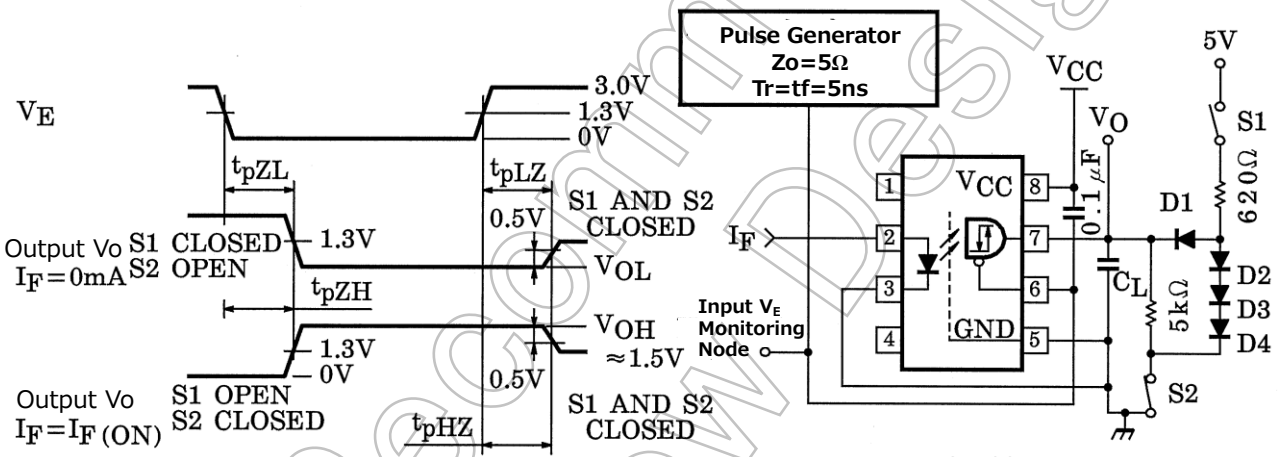
Test Circuit 1 t_{pHL}, t_{pLH}, t_r and t_f



D1 to D4 : 1S1588

C_L is approximately 15pF which includes probe and stray wiring capacitance.

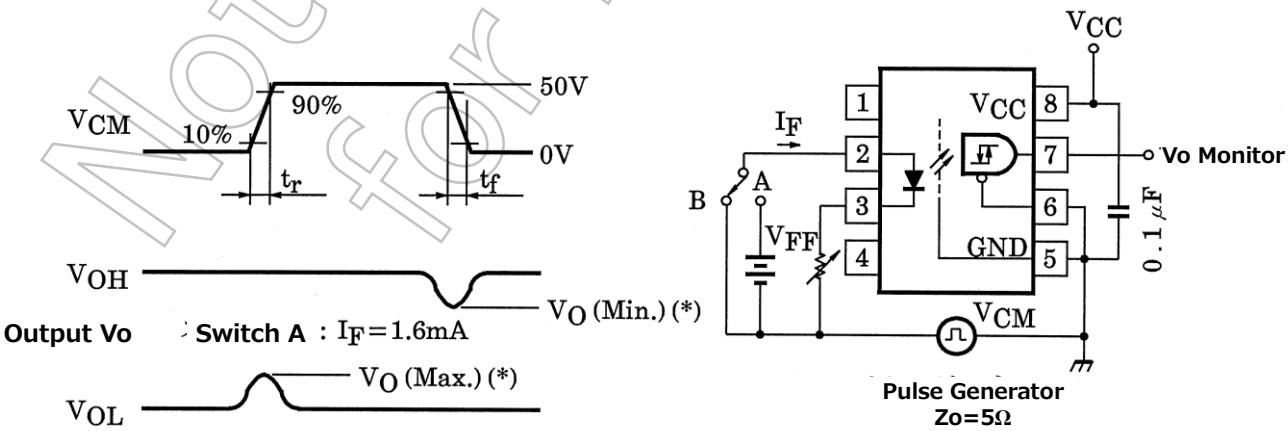
Test Circuit 2 t_{pHZ}, t_{pZH}, t_{pLZ}, and t_{pZL}



D1 to D4 : 1S1588

C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 3 Common Mode Transient Immunity



$$CM_H = \frac{40\ (V)}{t_f\ (\mu s)},\quad CM_L = \frac{40\ (V)}{t_r\ (\mu s)}$$

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