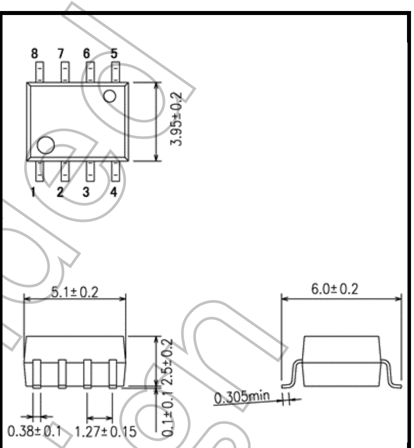
TOSHIBA PHOTOCOUPLER IRED & PHOTO-IC

TLP2118

PDP (Plasma Display Panel)
FA (Factory Automation)
Interfaces of measuring and control instruments

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	11-5K1S

Weight: 0.11 g (Typ.)

The Toshiba TLP2118 consists of an infrared emitting diodes and integrated high-gain, high-speed photodetectors.
The TLP2118 is housed in the SO8 package.
Since the TLP2118 contains two photocouplers, it saves board space.
The photodetector has an open-collector output stage.
The photodetector has an internal Faraday shield that provides a guaranteed common-mode transient immunity of ±15 kV/μs.

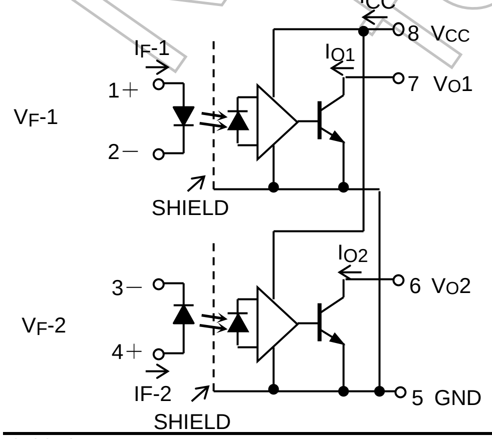
- Inverter logic type (Open collector output)
- Package: SO8
- Guaranteed performance over -40 to 100°C
- Power supply voltage: 4.5 to 5.5 V
- Input threshold current: I_{FH} = 5.0 mA (max)
- Propagation delay time t_{pHL}/t_{pLH}: 75 ns (max)
- Common-mode transient immunity: ±15 kV/μs (min)
- Isolation voltage: 2500 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
  File No.E67349
- VDE-approved : EN 60747-5-5 (Note 1)

Note 1: When a VDE approved type is needed, please designate the **Option(V4)**.

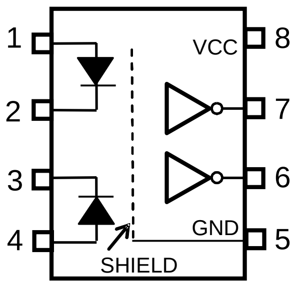
Truth Table

Input	LED1(2)	Output 1(2)
H	ON	L
L	OFF	H

Schematic



Pin Configuration (Top View)



1: ANODE 1
2: CATHODE 1
3: CATHODE 2
4: ANODE 2
5: GND
6: V_O2 (Output 2)
7: V_O1 (Output 1)
8: V_{CC}

Start of commercial production
2009-07

Absolute Maximum Ratings (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Note 1)	I_F	20	mA
	Forward Current Derating (Ta ≥ 95°C)	ΔI_F /°C	-0.67	mA/°C
	Reverse Voltage (Note 1)	V_R	5	V
	Peak Transient Forward Current (Note 1)(Note 2)	I_{FPT}	40	mA
	Peak Transient Forward Current Derating (Ta ≥ 95°C)	ΔI_{FPT} /°C	-1.0	mA/°C
	Diode power dissipation	P_D	40	mW
	Diode power dissipation derating (Ta ≥ 95°C)	ΔP_D /°C	-1.3	mW/°C
DETECTOR	Output Current (Ta ≤ 100°C) (Note 1)	I_O	25	mA
	Output Voltage (Note 1)	V_O	6	V
	Supply Voltage	V_{CC}	6	V
	Output Power Dissipation (Note 1)	P_O	40	mW
Operating Temperature Range		T_{opr}	-40 to 100	°C
Storage Temperature Range		T_{stg}	-55 to 125	°C
Lead Soldering Temperature (10 s)		T_{sol}	260	°C
Isolation Voltage (AC, 60 s, R.H.≤ 60 %) (Note 3)		BV_S	2500	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Each channel.

Note 2: Pulse width ≤ 1 ms, duty = 50 %.

Note 3: This device is regarded as a two terminal device: pins 1, 2, 3 and 4 are shorted together, as are pins 5, 6, 7 and 8.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current , High Level	I_{FH}	7.5	-	18	mA
Input Voltage , Low Level	V_{FL}	0	-	0.8	V
Supply Voltage*	V_{CC}	4.5	-	5.5	V
Operating Temperature	T_{opr}	-40	-	100	°C

* This item denotes operating range, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics
(Unless otherwise specified, Ta=-40 to 100°C, V_{CC}=4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT
Input Forward Voltage	V_F	-	I_F = 10 mA, Ta = 25 °C	1.4	1.57	1.8	V
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta Ta$	-	I_F = 10 mA	-	-2.0	-	mV/°C
Input Reverse Current	I_R	-	V_R = 5V, Ta = 25 °C	-	-	10	µA
Input Capacitance	C_T	-	V = 0 V, f = 1 MHz, Ta = 25 °C	-	60	-	pF
Logic High Output Current	I_{OH}	1	V_F = 0.8 V, V_O = 5.5 V	-	-	250	µA
			Ta=25 °C	-	0.5	10	
Logic Low Output Voltage	V_{OL}	2	I_F = 10 mA, I_O = 13 mA (Sinking)	-	0.2	0.6	V
Logic Low Supply Current	I_{CCL}	3	I_{F1} = I_{F2} = 10 mA	-	3	10	mA
Logic High Supply Current	I_{CCH}	4	I_F = 0 mA	-	3	10	mA
"H Level Output to L Level Output" Input Current	I_{FH}	-	I_O = 13 mA (Sinking), V_O < 0.6 V	-	1.0	5.0	mA

*All typical values are at Ta = 25°C, V_{CC} = 5V unless otherwise specified

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C_S	V_S = 0 V, f = 1 MHz (Note 3)	—	0.8	—	pF
Isolation resistance	R_S	R.H. ≤ 60 %, V_S = 500 V (Note 3)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 60 s (Note 3)	2500	—	—	V_{rms}

Switching Characteristics (Unless otherwise specified, Ta=-40 to 100 ˚C、V_{CC}=4.5 to 5.5 V)(Each Channel)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION		MIN	TYP.	MAX	UNIT
Propagation Delay Time to Logic Low output	t_{pHL}	5	I_F = 0→7.5 mA	R_L = 350 Ω C_L = 15 pF (Note 4)	-	30	75	ns
Propagation Delay Time to Logic High output	t_{pLH}		I_F = 7.5→0 mA		-	30	75	ns
Switching Time Dispersion between ON and OFF	$\|t_{pHL}-t_{pLH}\|$		I_F = 0↔7.5 mA	R_L = 350 Ω C_L = 15 pF (Note 4)	-	-	35	ns
Propagation Delay Skew (Note 5)	t_{psk}				-50	-	50	ns
Fall Time (90 – 10 %)	t_f		I_F = 0→7.5 mA	R_L = 350 Ω C_L = 15 pF (Note 4)	-	30	-	ns
Rise Time (10 – 90 %)	t_r		I_F = 7.5→0 mA		-	30	-	ns
Common Mode transient Immunity at High Level Output	CM_H	6	V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{CC} = 5 V , Ta = 25 °C		15	-	-	kV/μs
Common Mode transient Immunity at Low Level Output	CM_L		V_{CM} =1 000 V_{p-p}, I_F = 10 mA, VCC = 5 V , Ta = 25 °C		-15	-	-	kV/μs

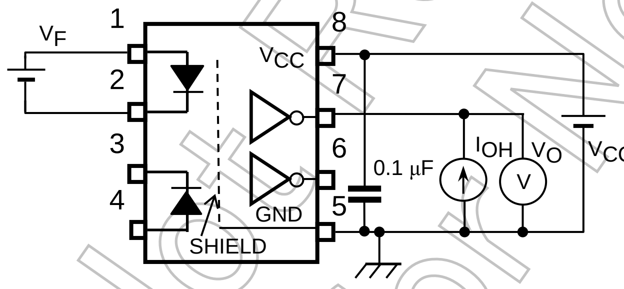
*All typical values are at Ta = 25 °C

Note: A ceramic capacitor (0.1 μF) should be connected from pin 8 (V_{CC}) to pin 5 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

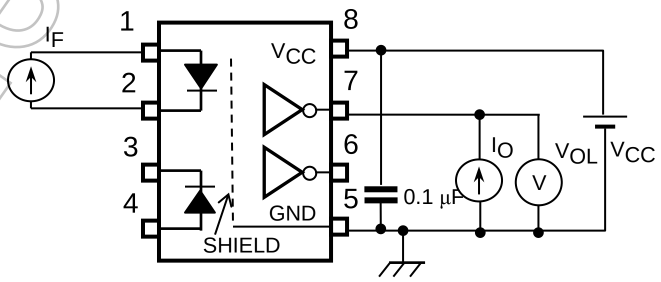
Note 4: f = 5 MHz, duty = 50 %, input current t_r = t_f = 5 ns, C_L is approximately 15 pF which includes probe and Jig/stray wiring capacitance.

Note 5: Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. tpHL or tpLH) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

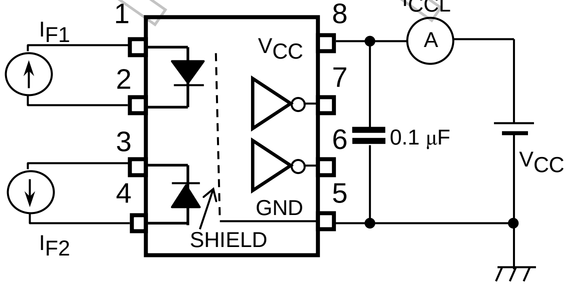
TEST CIRCUIT 1: I_{OH} Test Circuit



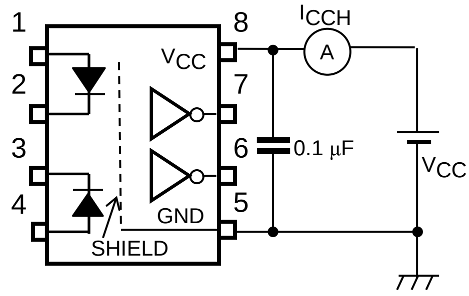
TEST CIRCUIT 2: V_{OL} Test Circuit



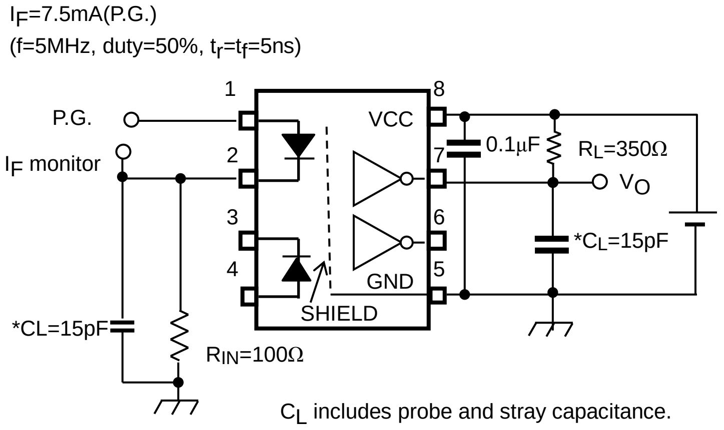
TEST CIRCUIT 3: I_{CCL} Test Circuit

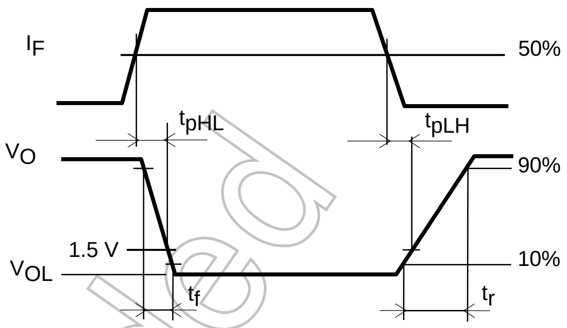


TEST CIRCUIT 4: I_{CCH} Test Circuit



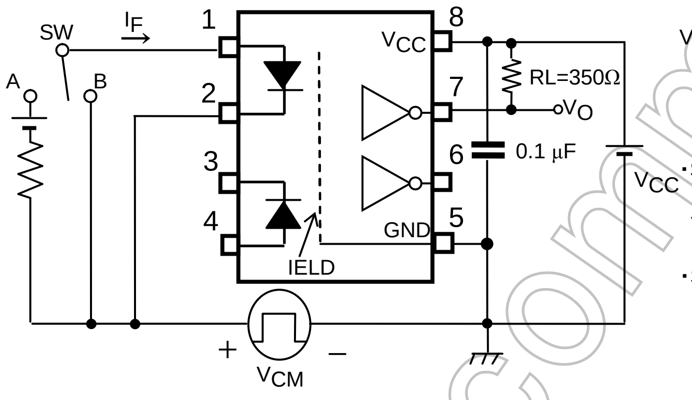
TEST CIRCUIT 5: Switching Time Test Circuit

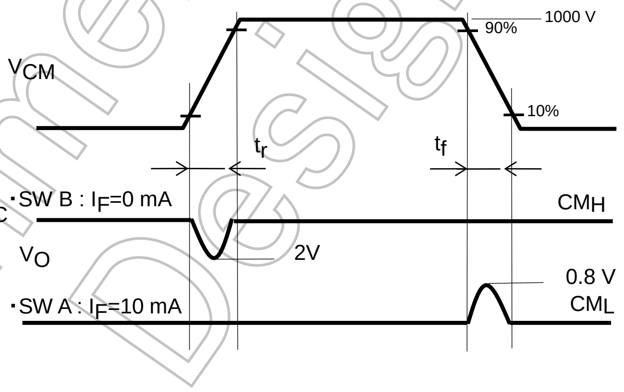




C_L includes probe and stray capacitance.
P.G.: Pulse generator

TEST CIRCUIT 6: Common-Mode Transient Immunity Test Circuit





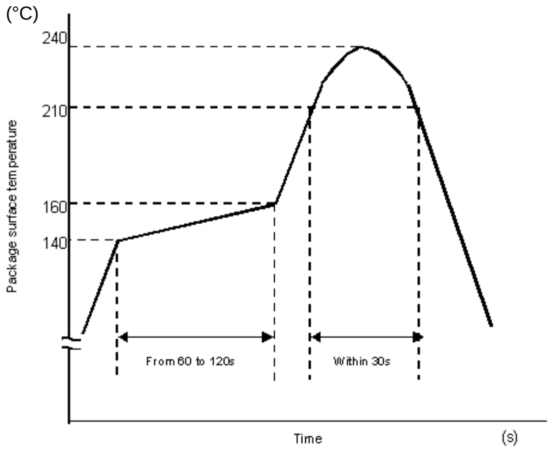
$$CM_H = -\frac{800(V)}{t_r(\mu s)} \quad CM_L = \frac{800(V)}{t_f(\mu s)}$$

PRECAUTIONS OF SURFACE MOUNTING TYPE PHOTOCOUPLER SOLDERING & GENERAL STORAGE

(1) Precautions for Soldering

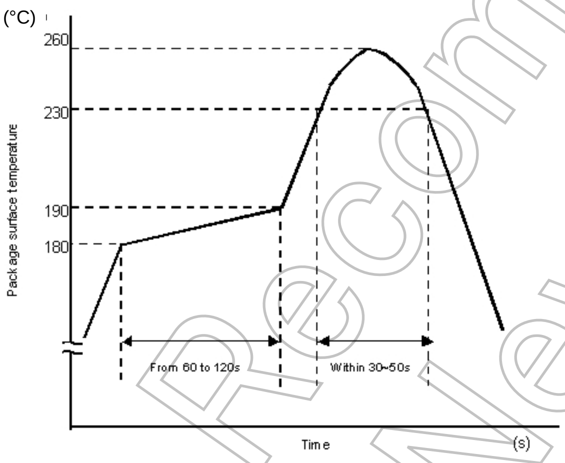
1) When Using Soldering Reflow

- An example of a temperature profile when Sn-Pb eutectic solder is used:



This profile is based on the device’s maximum heat resistance guaranteed value.
Set the preheat temperature/heating temperature to the optimum temperature corresponding to the solder paste type used by the customer within the described profile.

- An example of a temperature profile when lead(Pb)-free solder is used:



This profile is based on the device’s maximum heat resistance guaranteed value.
Set the preheat temperature/heating temperature to the optimum temperature corresponding to the solder paste type used by the customer within the described profile.

- Reflow soldering must be performed once or twice.
- The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

2) When using soldering Flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)

- Apply preheating of 150 °C for 60 to 120 seconds.
- Mounting condition of 260 °C and within 10 seconds is recommended.
- Flow soldering must be performed once.

3) When using soldering Iron (Applicable to both eutectic solder and Lead(Pb)-Free solder)

- Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C.
- Heating by soldering iron must be only once per one lead.

(2) Precautions for General Storage

1) Do not store devices at any place where they will be exposed to moisture or direct sunlight.

2) When transportation or storage of devices, follow the cautions indicated on the carton box.

3) The storage area temperature should be kept within a temperature range of 5 °C to 35 °C,
and relative humidity should be maintained at between 45% and 75%.

4) Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.

5) Use storage areas where there is minimal temperature fluctuation. Because rapid temperature changes can cause condensation to occur on stored devices, resulting in lead oxidation or corrosion, as a result, the solderability of the leads will be degraded.

6) When repacking devices, use anti-static containers.

7) Do not apply any external force or load directly to devices while they are in storage.

8) If devices have been stored for more than two years, even though the above conditions have been followed, it is recommended that solderability of them should be tested before they are used.

Specification for Embossed–Tape Packing (TP) for SO8 Coupler

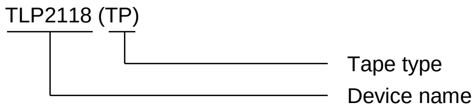
1. Applicable Package

Package	Product Type
SO8	Photocoupler

2. Product Naming System

Type of package used for shipment is denoted by a symbol suffix after a product number. The method of classification is as below.

(Example)



3. Tape Dimensions

3.1 Orientation of Device in Relation to Direction of Tape Movement

Device orientation in the recesses is as shown in Figure 1.

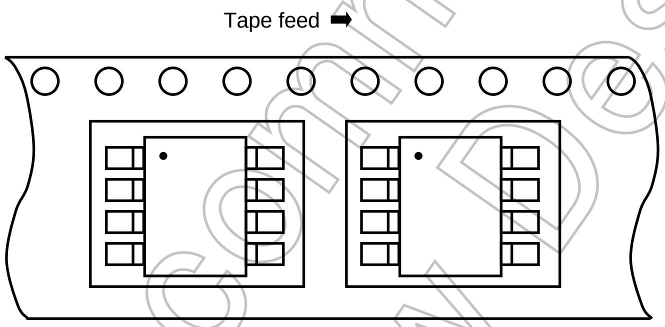


Figure 1 Device Orientation

3.2 Tape Packing Quantity: 2500 devices per reel

3.3 Empty Device Recesses Are as Shown in Table 1.

Table 1 Empty Device Recesses

	Standard	Remarks
Occurrences of 2 or more successive empty device recesses	0 device	Within any given 40-mm section of tape, not including leader and trailer
Single empty device recesses	6 devices (max) per reel	Not including leader and trailer

3.4 Start and End of Tape

The start of the tape has 50 or more empty holes. The end of tape has 50 or more empty holes and two empty turns only for a cover tape.

3.5 Tape Specification

(1) Tape material: Plastic (protection against electrostatics)

(2) Dimensions: The tape dimensions are as shown in Figure 2 and table 2.

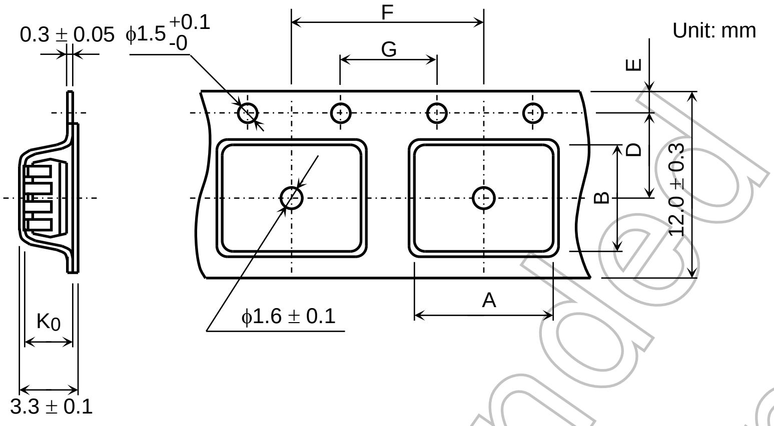


Figure 2 Tape Forms

Table 2 Tape Dimensions

Unit: mm
Unless otherwise specified: ±0.1

Symbol	Dimension	Remark
A	6.5	—
B	5.6	—
D	5.5	Center line of indented square hole and sprocket hole
E	1.75	Distance between tape edge and hole center
F	8.0	Cumulative error $^{+0.1}_{-0.3}$ (max) per 10 feed holes
G	4.0	Cumulative error $^{+0.1}_{-0.3}$ (max) per 10 feed holes
K_0	3.1	Internal space

3.6 Reel

(1) Material: Plastic

(2) Dimensions: The reel dimensions are as shown in Figure 3 and Table 3.

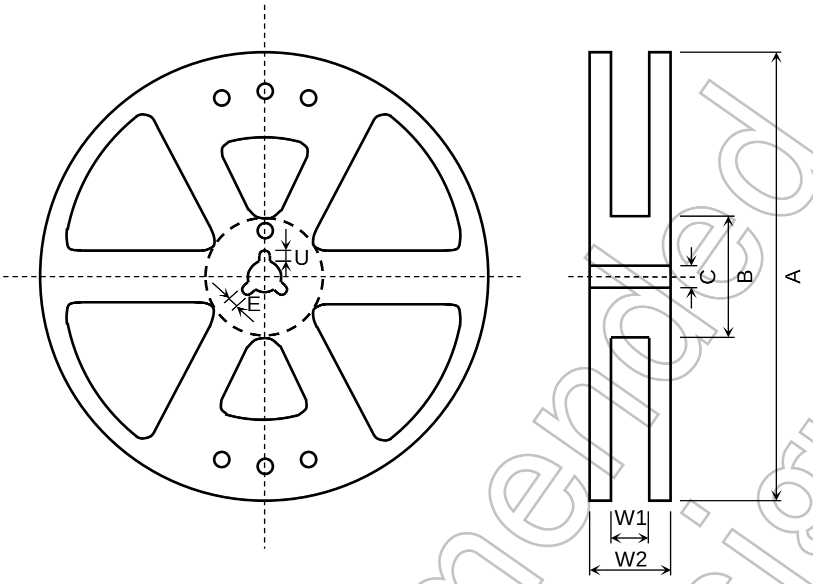


Figure 3 Reel Form

Table 3 Reel Dimensions

Unit: mm

Symbol	Dimension
A	Φ330 ±2
B	Φ80 ±1
C	Φ13 ±0.5
E	2.0 ±0.5
U	4.0 ±0.5
W1	13.5 ±0.5
W2	17.5 ±1.0

4. Packing

Packed in a shipping carton.

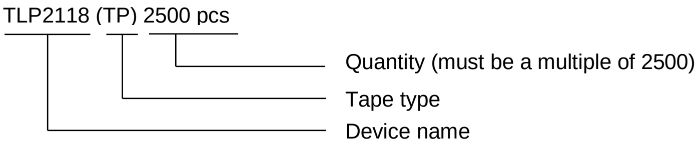
5. Label Indication

The carton bears a label indicating the product number, the symbol representing classification of standard, the quantity, the lot number and the Toshiba company name.

6. Ordering Method

When placing an order, please specify the product number, the tape type and the quantity as shown in the following example.

(Example)



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