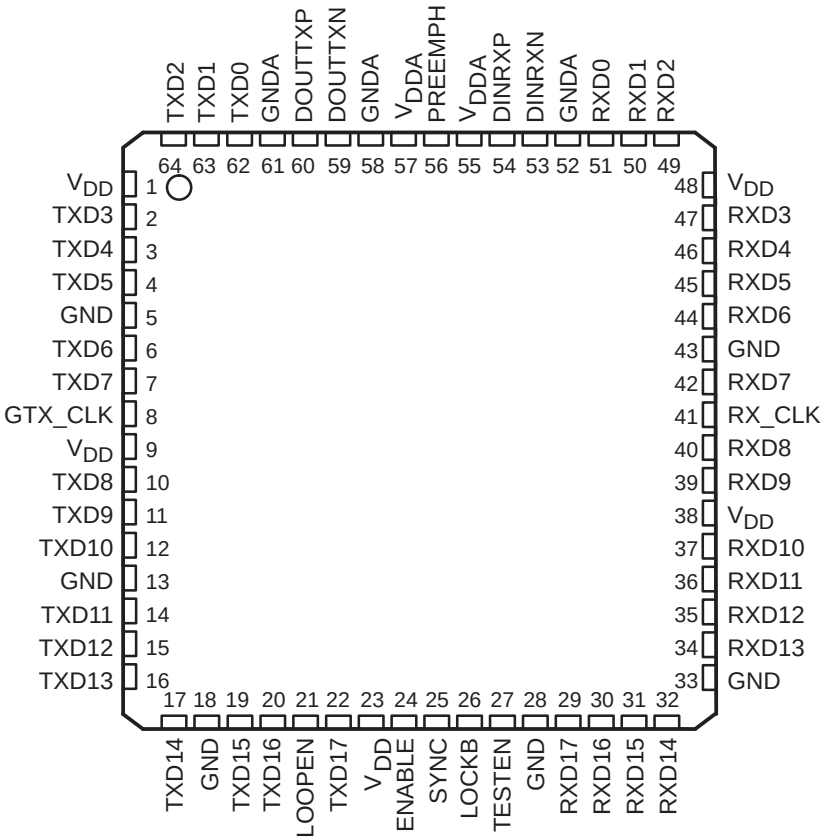
- **Hot Plug Protection**
- **1 to 2.5 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **High-Performance 64-Pin HTQFP Thermally Enhanced Package (PowerPAD™)**
- **2.5-V Power Supply for Low Power Operation**
- **Selectable Signal Preemphasis Serial Output**
- **Interfaces to Backplane, Copper Cables, or Optical Converters**
- **Lock Indication and Sync Mode for Fast Initialization**
- **18-Bit Parallel Busses for Flexible Interface Applications**
- **On-chip PLL Provides Clock Synthesis From Low-Speed Reference**
- **Receiver Differential Input Thresholds 200 mV Min**
- **Rated for Industrial Temperature Range**
- **Power: 424 mW at 2.5 Gbps**
- **Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link**
- **Passive Receive Equalizer**



## description

The TLK2521 is a member of the WizardLink family of multi-gigabit transceivers, intended for use in high-speed bidirectional point-to-point data transmission systems. The TLK2521 supports an effective serial interface speed of 1 Gbps to 2.5 Gbps, providing up to 2.25 Gbps of data bandwidth.

The primary application of the TLK2521 is to provide high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The TLK2521 can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector pins, and transmit/receive pins. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. The data is then reconstructed into its original parallel format. It offers significant power and cost savings over current solutions, as well as scalability for higher data rate in the future.

The TLK2521 performs the data parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface device. The serial transceiver interface operates at a maximum speed of 2.5 Gbps. The transmitter latches 18-bit parallel data at a rate based on the supplied reference clock (GTX_CLK). The 18-bit parallel data is internally encoded into 20 bits by framing the 18-bit data with a start and a stop bit. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (GTX_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data synchronizing the resulting 20-bit wide parallel data to the extracted reference clock (RX_CLK). It then extracts the 18 bits of data from the 20-bit wide data resulting in 18 bits of parallel data at the receive data pins (RXD0−17). This results in an effective data payload of 900 Mbps to 2.25 Gbps (18 bits data x GTX_CLK frequency).

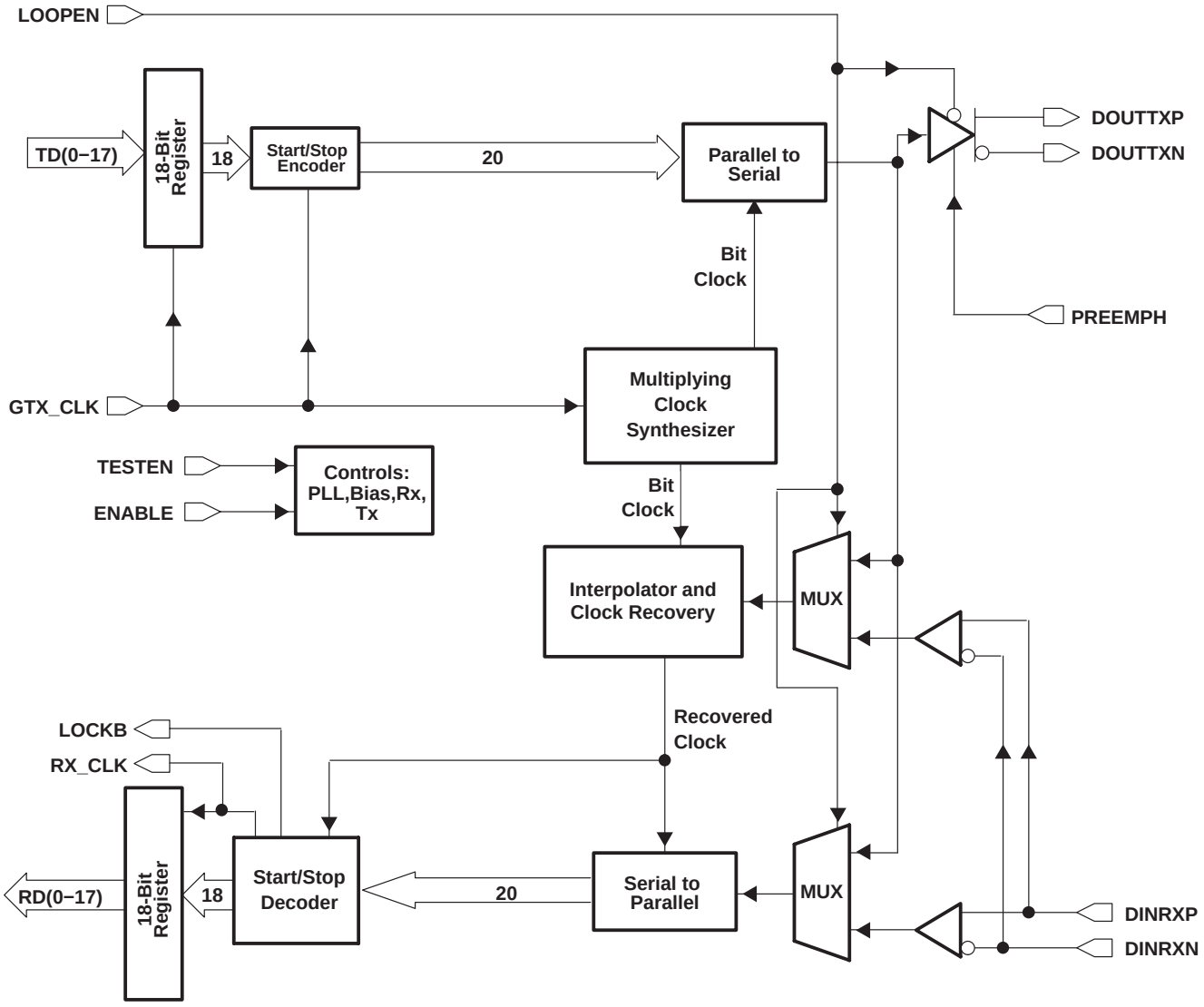
The TLK2521 is housed in a high performance, thermally enhanced, 64-pin HTQFP PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. It is strongly recommended that the TLK2521 PowerPAD be soldered to the grounded thermal land on the board, since the PowerPAD also constitutes a major electrical ground connection for the TLK2521. All ac performance specifications in this data sheet are measured with the PowerPAD soldered to the test board.

The TLK2521 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer allowing the protocol device a functional self-check of the physical interface.

The TLK2521 is designed to be hot plug capable. An on-chip power-on reset circuit holds the RX_CLK low and places the parallel side output signal pins, DOUTTXP and DOUTTXN, into a high-impedance state during power up.

The TLK2521 uses a 2.5-V supply. The I/O section is 3-V compatible. The TLK2521 is characterized for operation from −40°C to 85°C.

## functional block diagram




## transmit interface

The transmitter portion registers valid incoming 18-bit wide data (TXD[0:17]) on the rising edge of GTX_CLK. The data is then framed with a start and a stop bit, serialized and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (GTX_CLK) by a factor of 10 times creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register, which transmits data on both the rising and falling edges of the bit clock providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (D0) first.

### transmit data bus

The transmit bus interface accepts 18-bit wide single-ended TTL parallel data at the TXD[0:17] pins. Data is valid on the rising edge of GTX_CLK. The GTX_CLK is used as the word clock. The data and clock signals must be properly aligned as shown in Figure 1. Detailed timing information can be found in the *TTL input electrical characteristics* table.

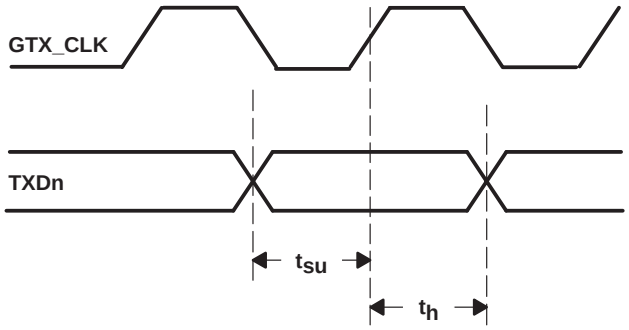



**Figure 1. Transmit Timing Waveform**

### transmission latency

The data transmission latency of the TLK2521 is defined as the delay from the initial 18-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. Figure 2 illustrates the timing relationship between the transmit data bus, GTX_CLK, and serial transmit pins. Detailed latency information can be found in the *transmitter/receiver characteristics* table.

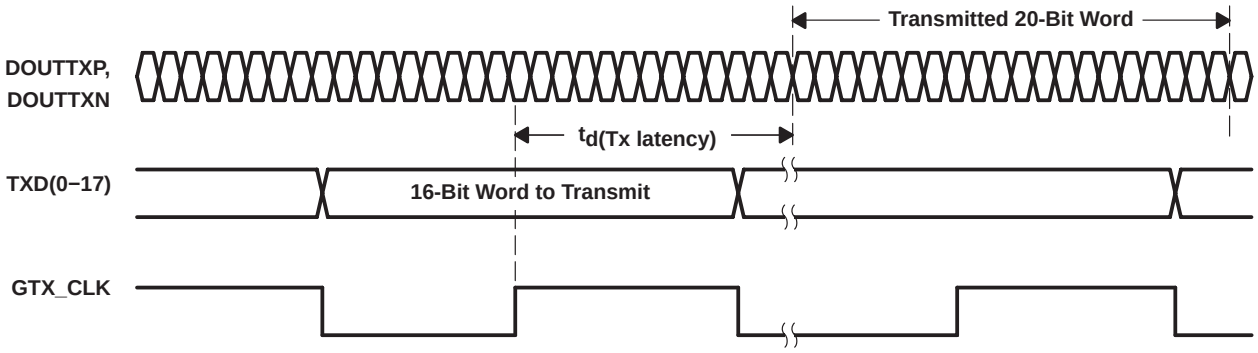



**Figure 2. Transmitter Latency**

### start/stop framing logic

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions in which to stay locked onto the data stream. The signal coding also provides a mechanism for the receiver to identify the byte boundary for correct deserialization. The TLK2521 wraps a start bit (1) and a stop bit (0) around the 18-bit data payload as shown in Figure 3. This is transparent to the user as the TLK2521 internally adds the framing bits to the data such that the user reads and writes actual 18-bit data.

### start/stop framing logic (continued)


**Figure 3. Serial Output Data Stream with Start and Stop Bit**

### parallel-to-serial

The parallel-to-serial shift register takes in the 20-bit wide data word multiplexed from the framing logic and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the GTX_CLK input frequency. The LSB (TD0) is transmitted first as shown in Figure 3.

### high-speed data output

The high-speed data output driver consists of a PECL-compatible differential pair that can be optimized for a particular transmission line impedance and length. The line can be directly coupled or ac coupled. AC-coupling is only recommended if the parallel TX data stream is encoded to achieve a dc-balanced data stream. See Figure 11 and Figure 12 for termination details. No external pullup or pulldown resistors are required.

The TLK2521 provides a selectable signal preemphasis option for driving lossy media. The first bit of a run length of same-value bits is driven to a larger output swing, which precompensates for signal inter-symbol interference (ISI) in lossy media such as copper cables or printed circuit board traces due to preemphasis.

## receive interface

The receiver portion of the TLK2521 accepts 20-bit framed differential serial data. The interpolator and clock recovery circuit locks to the data stream and extracts the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to the 20-bit word boundary by finding the start/stop bits, and the 18-bit data is output on a 18-bit wide parallel bus synchronized to the extracted receive clock.

### receive data bus

The receive bus interface drives 18-bit wide single-ended TTL parallel data at the RXD[0:17] pins. Data is valid on the rising edge of RX_CLK. The RX_CLK is used as the recovered word clock. The data and clock signals are aligned as shown in Figure 4. Detailed timing information can be found in the TTL output switching characteristics table.

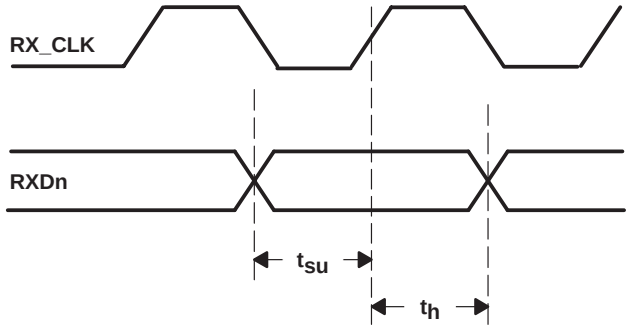



**Figure 4. Receive Timing Waveform**

### data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RXD0 received as first bit. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. Figure 5 illustrates the timing relationship between the serial receive pins, the recovered word clock (RX_CLK), and the receive data bus. Detailed latency information can be found in the transmitter/receiver characteristics table.

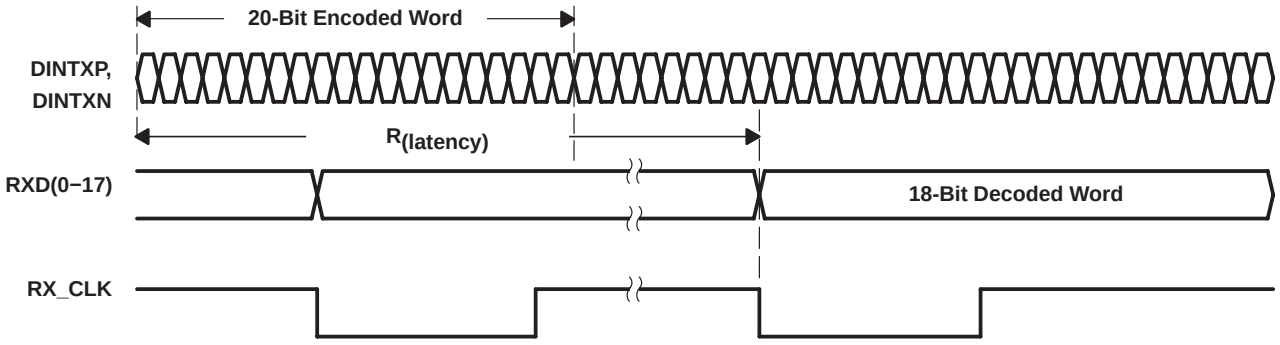



**Figure 5. Receiver Latency**

### serial-to-parallel

Serial data is received on the DINRXP and DINRXN pins. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers.

## synchronization mode

The deserializer PLL must synchronize to the serializer in order to receive valid data. Synchronization can be accomplished in one of two ways.

### rapid synchronization

The serializer has the capability to send specific SYNC patterns consisting of nine ones and nine zeros, switching at the input clock rate. The transmission of SYNC patterns enables the deserializer to lock to the serializer signal within a deterministic time frame. The transmission of SYNC patterns is selected via the SYNC input on the serializer. Upon receiving a valid SYNC pulse (wider than 6 clock cycles), 1026 cycles of SYNC pattern are sent.

When the deserializer detects edge transitions at the serial input, it attempts to lock to the embedded clock information. The deserializer LOCKB output remains inactive while its clock/data recovery (CDR) locks to the incoming data or SYNC patterns present on the serial input. When the deserializer locks to the serial data, the LOCKB output goes active. When LOCKB is active, the deserializer outputs represent incoming serial data. One approach is to tie the deserializer LOCKB output directly to the SYNC input of the transmitter.

### random lock synchronization

The deserializer can attain lock to a data stream without requiring the serializer to send special SYNC patterns. This allows the TLK2521 to operate in open-loop applications. Equally important is the deserializer's ability to support hot insertion into a running backplane. In the open-loop or hot-insertion case, it is assumed the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, the exact lock time cannot be predicted. The primary constraint on the random lock time is the initial phase relation between the incoming data and the GTX_CLK when the deserializer powers up.

**random lock synchronization (continued)**

The data contained in the data stream can also affect lock time. If a specific pattern is repetitive, the deserializer could enter false lock—falsely recognizing the data pattern as the start/stop bits. This is referred to as repetitive multitransition (RMT). This occurs when more than one low-high transition takes place per clock cycle over multiple clock cycles. In the worst case, the deserializer could become locked to the data pattern rather than the clock. Circuitry within the deserializer can detect that the possibility of false lock exists. Upon detection, the circuitry prevents the LOCKB from becoming active until the potential false-lock pattern changes. Notice that the RMT pattern only affects the deserializer lock time, and once the deserializer is in lock, the RMT pattern does not affect the deserializer state as long as the same data boundary happens each cycle. The deserializer does not go into lock until it finds a unique data boundary that consists of four consecutive start/stop bits at the same position.

The deserializer stays in lock until it cannot detect the same data boundary (start/stop bits) for four consecutive cycles. Then the deserializer goes out of lock and hunts for the new data boundary (start/stop bits). In the event of loss of synchronization, the LOCKB pin output goes inactive and the outputs (including RX_CLK) enter a high-impedance state. The user's system should monitor the LOCKB pin in order to detect a loss of synchronization. Upon detection of loss of lock, sending SYNC patterns for resynchronization is desirable if reestablishing lock within a specific time is critical. However, the deserializer can lock to random data as previously noted. LOCKB is held inactive for at least nine cycles after loss of lock is detected.

**power-down mode**

When the ENABLE pin is deasserted low, the TLK2521 goes into a power-down mode. In the power-down mode, the serial transmit pins (DOUTTXP, DOUTTXN) and the receive data bus pins (RXD[0:17]) go into a high-impedance state.

**reference clock input**

The reference clock (GTX_CLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edge clock providing a serial data rate that is 20 times the reference clock.

The receiver tracking logic uses clock phases from the internal PLL as it aligns the recovered clock phase with the incoming serial data stream; therefore, the input reference clock (GTX_CLK) is needed even if the transmit function of the TLK2521 is not being used. The receiver function has the ability to track an incoming serial data stream that is within ±200 ppm of the data rate that is set by GTX_CLK. This allows the use of clock sources with ±100 ppm frequency tolerance.

**operating frequency range**

The TLK2521 may operate at a serial data rate between 1 Gbit/s to 2.5 Gbit/s. GTX_CLK must be within ±100 PPM of the desired parallel data rate clock.

**testability**

The TLK2521 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The ENABLE pin allows for all circuitry to be disabled so that an IDDQ test can be performed.

**loop-back testing**

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loop-back path. Enabling this pin causes serial transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loop-back testing.)

### power-on reset

Upon application of minimum valid power, the TLK2521 generates a power-on reset. During the power-on reset the RXD pins are tri-stated. RX_CLK is held low. The length of the power-on reset cycle is dependent upon the REFCLK frequency but is less than 1 ms in duration.

## Terminal Functions

| TERMINAL | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **SIGNAL PIN** | | | |
| DOUTTXP | 60 | Output (High-Z power up) | Serial transmit outputs. DOUTTXP and DOUTTXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the GTX_CLK value. DOUTTXP and DOUTTXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low. During power-on reset, these pins are high impedance. |
| DOUTTXN | 59 | | |
| DINRXP | 54 | Input | Serial receive inputs. DINRXP and DINRXN together are the differential serial input interface from a copper or an optical I/F module. |
| DINRXN | 53 | | |
| GTX_CLK | 8 | Input | Reference clock. GTX_CLK is a continuous external input clock that synchronizes the transmitter interface TXD. The frequency range of GTX_CLK is 50 MHz to 125 MHz. The transmitter uses the rising edge of this clock to register the 18-bit input data (TXD) for serialization. |
| TXD0 | 62 | Input | Transmit data bus. These inputs carry the 18-bit parallel data output from a protocol device to the transceiver for encoding, serialization and transmission. This 18-bit parallel data is clocked into the transceiver on the rising edge of GTX_CLK as shown in Figure 9. |
| TXD1 | 63 | | |
| TXD2 | 64 | | |
| TXD3 | 2 | | |
| TXD4 | 3 | | |
| TXD5 | 4 | | |
| TXD6 | 6 | | |
| TXD7 | 7 | | |
| TXD8 | 10 | | |
| TXD9 | 11 | | |
| TXD1 | 12 | | |
| TXD11 | 14 | | |
| TXD12 | 15 | | |
| TXD13 | 16 | | |
| TXD14 | 17 | | |
| TXD15 | 19 | | |
| TXD16 | 20 | | |
| TXD17 | 22 | | |
| RXD0 | 51 | Output (High-Z on power up) | Receive data bus. These outputs carry 18-bit parallel data output from the transceiver to the protocol device, synchronized to RX_CLK. The data is valid on the rising edge of RX_CLK as shown in Figure 10. These pins are 3-stated during power-on reset. These pins are also high impedance when enable=0. |
| RXD1 | 50 | | |
| RXD2 | 49 | | |
| RXD3 | 47 | | |
| RXD4 | 46 | | |
| RXD5 | 45 | | |
| RXD6 | 44 | | |
| RXD7 | 42 | | |
| RXD8 | 40 | | |
| RXD9 | 39 | | |
| RXD10 | 37 | | |
| RXD11 | 36 | | |
| RXD12 | 35 | | |
| RXD13 | 34 | | |

| TERMINAL | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| RXD14 | 32 | | |
| RXD15 | 31 | | |
| RXD16 | 30 | | |
| RXD17 | 29 | | |
| RX_CLK | 41 | Output (low on power up) | Recovered clock. Output clock that is synchronized to RXD. RX_CLK is the recovered serial data rate clock divided by 20. RX_CLK is held low during power-on reset. These pins are also high impedance when enable=0. |
| SYNC | 25 | Input (w/pulldown) | Fast synchronization. When asserted high, the transmitter substitute the 18-bit pattern 111111111000000000 ,so that when the start/stop bits are framed around the data the receiver can immediately detect the proper deserialization boundary. This is typically used during initialization of the serial link. |
| PREEMPH | 56 | Input | Preemphasis. When asserted, the serial transmit outputs have an extra output swing on the first bit of any run-length of same value bits than when deasserted. |
| **TEST PIN** | | | |
| ENABLE | 24 | Input (w/pullup) | Device enable. When this pin is held low, the device is placed in power down mode. When asserted high while the device is in power-down mode, the transceiver goes into power-on reset before beginning normal operation. |
| LOOPEN | 21 | Input (w/pulldown) | Loop enable. When LOOPEN is active high, the internal loop−back path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTXP and DOUTTXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active. |
| LOCKB | 26 | Output | Receiver lock. When asserted low, it indicates that the receiver has acquired bit synchronization on the data stream and has located the start/stop bits, so that the deserialized data presented on the parallel receive bus is properly received. These pins are also high impedance when enable=0. |
| TESTEN | 27 | Input (w/pulldown) | Test mode enable. This pin should be left unconnected or tied low. |
| **POWER PIN** | | | |
| VDD | 1, 9, 23, 38, 48 | Supply | Digital logic power. Provides power for all digital circuitry and digital I/O buffers. |
| VDDA | 55, 57 | Supply | Analog power. VDDA provides a supply reference for the high-speed analog circuits, receiver and transmitter. |
| **GROUND PIN** | | | |
| GNDA | 52, 58, 61 | Ground | Analog ground. GNDA provides a ground reference for the high-speed analog circuits, RX and TX. |
| GND | 5, 13, 18, 28, 33, 43 | Ground | Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers. |

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1) . . . . . −0.3 V to 3 V
Voltage range at TXD, ENABLE, GTX_CLK, LOOPEN, SYNC, PREEMPH . . . . . −0.3 V to 4 V
Voltage range at any other terminal except above . . . . . −0.3 V to $V_{CC}$ + 0.3 V
Package power dissipation, $P_D$ . . . . . See Dissipation Rating Table
Storage temperature, $T_{stg}$ . . . . . −65°C to 150°C
Electrostatic discharge . . . . . HBM:2 kV, CDM:1.5 kV
Characterized free-air operating temperature range . . . . . −40°C to 85°C
Lead Temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR† ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| PAP64‡ | 3.22 W | 32.15 mW/°C | 1.77 W |
| PAP64§ | 0.94 W | 9.46 mW/°C | 0.52 W |
| PAP64¶ | 0.68 W | 6.78 mW/°C | 0.37 W |

† This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$)
‡ High K-board with solder
§ High K-board without solder
¶ Low K-board

NOTE: For more information, see the TI application note *PowerPAD™ Thermally Enhanced Package,* TI (SLMA002).

### electrical characteristics over recommended operating conditions

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 2.3 | 2.5 | 2.7 | V |
| $T_A$ | Operating free-air temperature | | −40 | | 85 | °C |
| $I_{CC}$ | Supply current | $V_{DD}$ = 2.5 V, Freq = 1 Gb/sec, PRBS pattern | | 71 | | mA |
| | | $V_{DD}$ = 2.5 V, Freq = 2.5 Gb/sec, PRBS pattern | | 170 | | |
| $P_D$ | Power dissipation | $V_{DD}$ = 2.5 V, Freq = 1 Gb/sec, PRBS pattern | | 178 | | mW |
| | | $V_{DD}$ = 2.5 V, Freq = 2.5 Gb/sec, PRBS pattern | | 424 | | |
| | | $V_{DD}$ = 2.75 V, Freq = 2.5 Gb/sec, worst case pattern | | | 730 | |
| | Shutdown current | ENABLE = 0, VDDA, VDD pins, $V_{DD}$ = max | | 130 | | µA |
| | PLL startup lock time | $V_{DD}$, VDDA = 2.3 V, EN ↑ to PLL acquire | | 0.1 | 0.4 | ms |
| | Data acquisition time | | | 1024 | | bits |

### reference clock (GTX_CLK) timing requirements over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_\omega$ | Frequency | Minimum data rate | TYP−0.01% | 50 | TYP+0.01% | MHz |
| | | Maximum data rate | TYP−0.01% | 125 | TYP+0.01% | MHz |
| | Frequency tolerance | | −100 | | 100 | ppm |
| | Duty cycle | | 40% | 50% | 60% | |
| | Jitter# | Peak-to-peak | | | 40 | ps |

# See the *Reference Lock Jitter Analysis For TLK2521* application note for more information.

## TTL input electrical characteristics over recommended operating conditions (unless otherwise noted)

### TTL Signals: TXD0 ...TXD17, GTX_CLK, LOOPEN, SYNC, PREEMPH

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | See Figure 6 | 2 | | 3.6 | V |
| $V_{IL}$ | Low-level input voltage | See Figure 6 | | | 0.8 | V |
| $I_{IH}$ | High-level input current | $V_{DD}$ = MAX, $V_{IN}$ = 2 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{DD}$ = MAX, $V_{IN}$ = 0.4 V | −40 | | | μA |
| $C_{IN}$ | Input capacitance | 0.8 V to 2 V | | | 4 | pF |
| $t_r$ | GTX_CLK, TXD rise time | 0.8 V to 2 V, C = 5 pF, See Figure 6 | | 1 | | ns |
| $t_f$ | GTX_CLK, TXD fall time | 2 V to 0.8 V, C = 5 pF, See Figure 6 | | 1 | | ns |
| $t_{su}$ | TXD setup to ↑ GTX_CLK | See Figure 6 | 1.5 | | | ns |
| $t_h$ | TXD hold to ↑ GTX_CLK | See Figure 6 | 0.4 | | | ns |

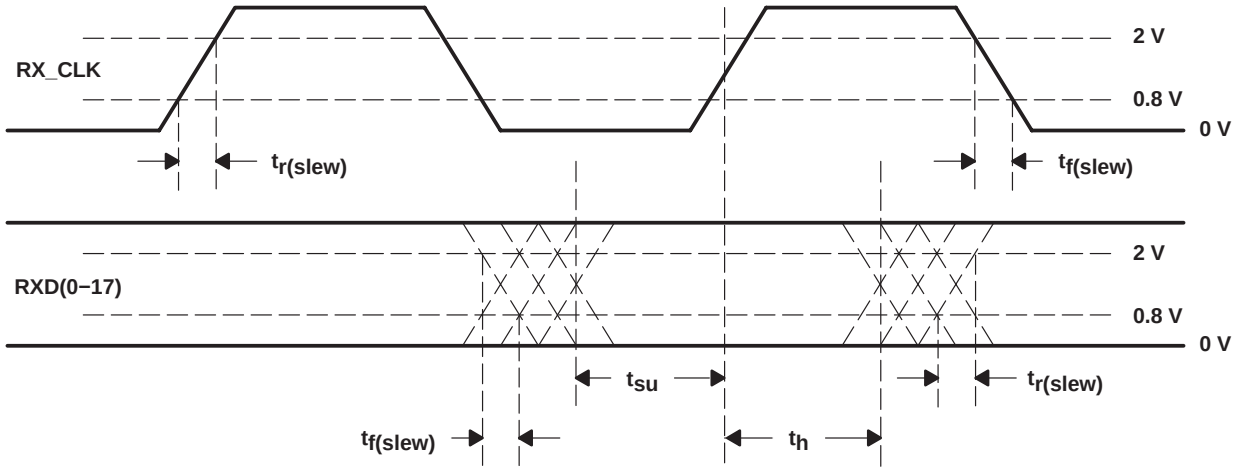



**Figure 6. TTL Data Input Valid Levels for AC Measurements**

### TTL output switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$= −1 mA, $V_{DD}$ = MIN | 2.1 | 2.3 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$= 1 mA, $V_{DD}$ = MIN | GND | 0.25 | 0.5 | V |
| $t_{r(slew)}$ | Magnitude of RX_CLK, RXD slew rate (rising) | 0.8 V to 2 V, C = 5 pF, See Figure 10 | 0.5 | | | V/ns |
| $t_{f(slew)}$ | Magnitude of RX_CLK, RXD slew rate (falling) | 0.8 V to 2 V, C = 5 pF, See Figure 10 | 0.5 | | | V/ns |
| $t_{su}$ | RXD setup to ↑ RX_CLK | 50% voltage swing, GTX_CLK = 50 MHz, See Figure 7 | 8 | | | ns |
| | | 50% voltage swing, GTX_CLK = 125 MHz, See Figure 7 | 3 | | | ns |
| $t_h$ | RXD hold to ↑ RX_CLK | 50% voltage swing, GTX_CLK = 50 MHz, See Figure 7 | 8 | | | ns |
| | | 50% voltage swing, GTX_CLK = 125 MHz, See Figure 7 | 3 | | | ns |

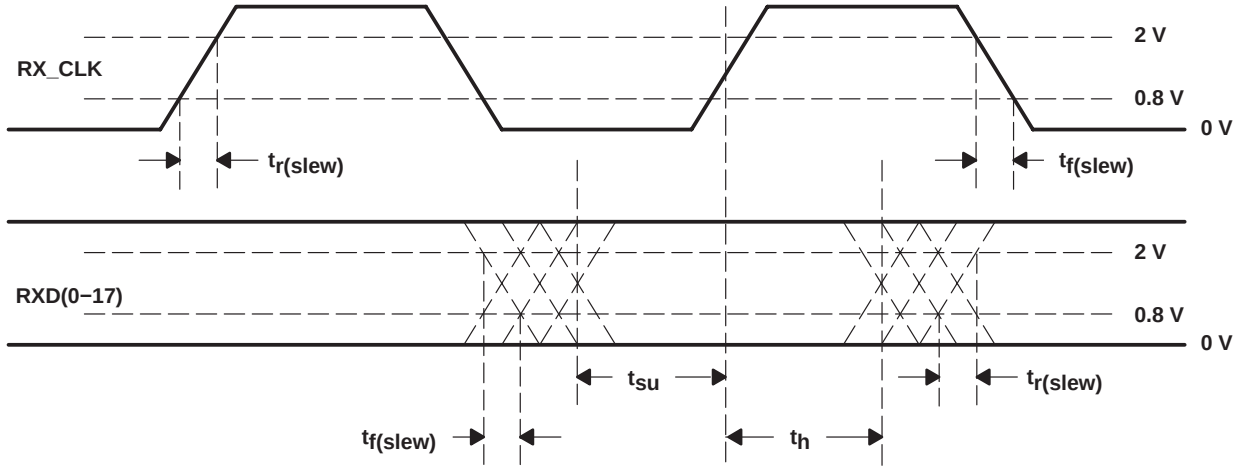



**Figure 7. TTL Data Output Valid Levels for AC Measurements**

## transmitter/receiver characteristics

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OD(p)}$ | $V_{OD(p)}$ = \|VTXP-VTXN\|, Preemphasis VOD, direct | DC coupled. Preemphasis = high, See Figure 8 | 675 | 900 | 1280 | mV |
| | | DC coupled. Preemphasis = low, See Figure 8 | 600 | 800 | 1210 | |
| $V_{OD(pp-p)}$ | Differential, peak to peak output voltage with preemphasis | DC coupled. Preemphasis = high, See Figure 8 | 1350 | 1800 | 2560 | mV |
| | | DC coupled. Preemphasis = low, See Figure 8 | 1200 | 1600 | 2420 | |
| $V_{OD(d)}$ | VD(d) = \|VTXP-VTXN\|, De-emphasis VOD, direct | DC coupled. See Figure 8 | 500 | 750 | 1100 | mV |
| $V_{OD(pp-d)}$ | Differential, peak to peak output voltage with deemphasis | DC coupled. See Figure 8 | 1000 | 1500 | 2200 | mV |
| $V_{(cmt)}$ | Transmit termination voltage range, (VTXP + VTXN)/2 | | 1000 | 1250 | 1400 | mV |
| $V_{ID}$ | Receiver input voltage differential VID= \|RXP – RXN\| | | 200 | | | mV |
| $V_{cmr}$ | Receiver common-mode voltage range, (VRXP + VRXN)/2 | | 1000 | | $V_{DD}$− 350 | mV |
| $I_{in}$ | Receiver input leakage | | −10 | | 10 | µA |
| $C_{in}$ | Receiver input capacitance | | | | 2 | pF |
| $t_t$, $t_f$ | Differential output signal rise, fall time (20% to 80%) | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 12 | 100 | 150 | | ps |
| | Serial transmit data total jitter (peak-to-peak) | Differential output jitter, random + deterministic, $2^{23}$–1 PRBS pattern at 2.5 Gbps | | 0.15 | | UI |
| | Receive jitter tolerance | Total input jitter, PRBS pattern, permitted eye closure at zero crossing | | 0.5 | | UI |
| $T_{latency}$ | TX latency | At 1 Gbps | 16 | | 19 | Bit times |
| | | At 2.5 Gbps | 18 | | 21 | |
| $R_{latency}$ | RX latency | At 1 Gbps | 88 | | 95 | Bit times |
| | | At 2.5 Gbps | 90 | | 103 | |

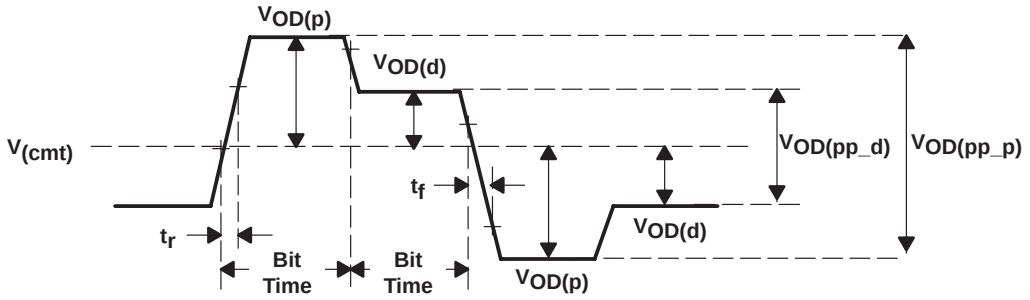



**Figure 8. Differential and Common-Mode Output Voltage Definitions**

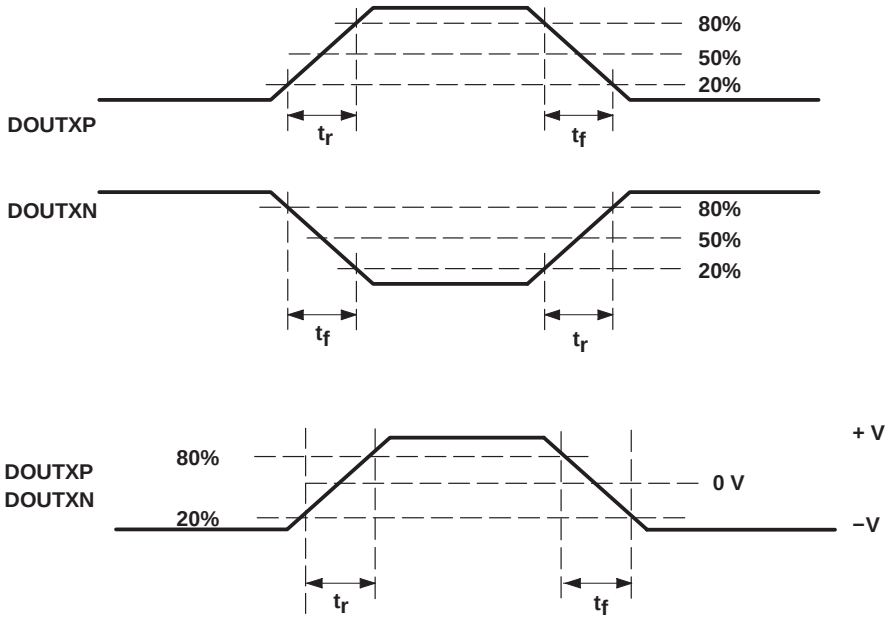



**Figure 9. Rise and Fall Time Definitions**

## thermal characteristics

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land | | 21.47 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 0.38 | | |
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land | | 42.2 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 0.38 | | |
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board mounted, no air flow, JEDEC test board | | 75.83 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 7.8 | | |

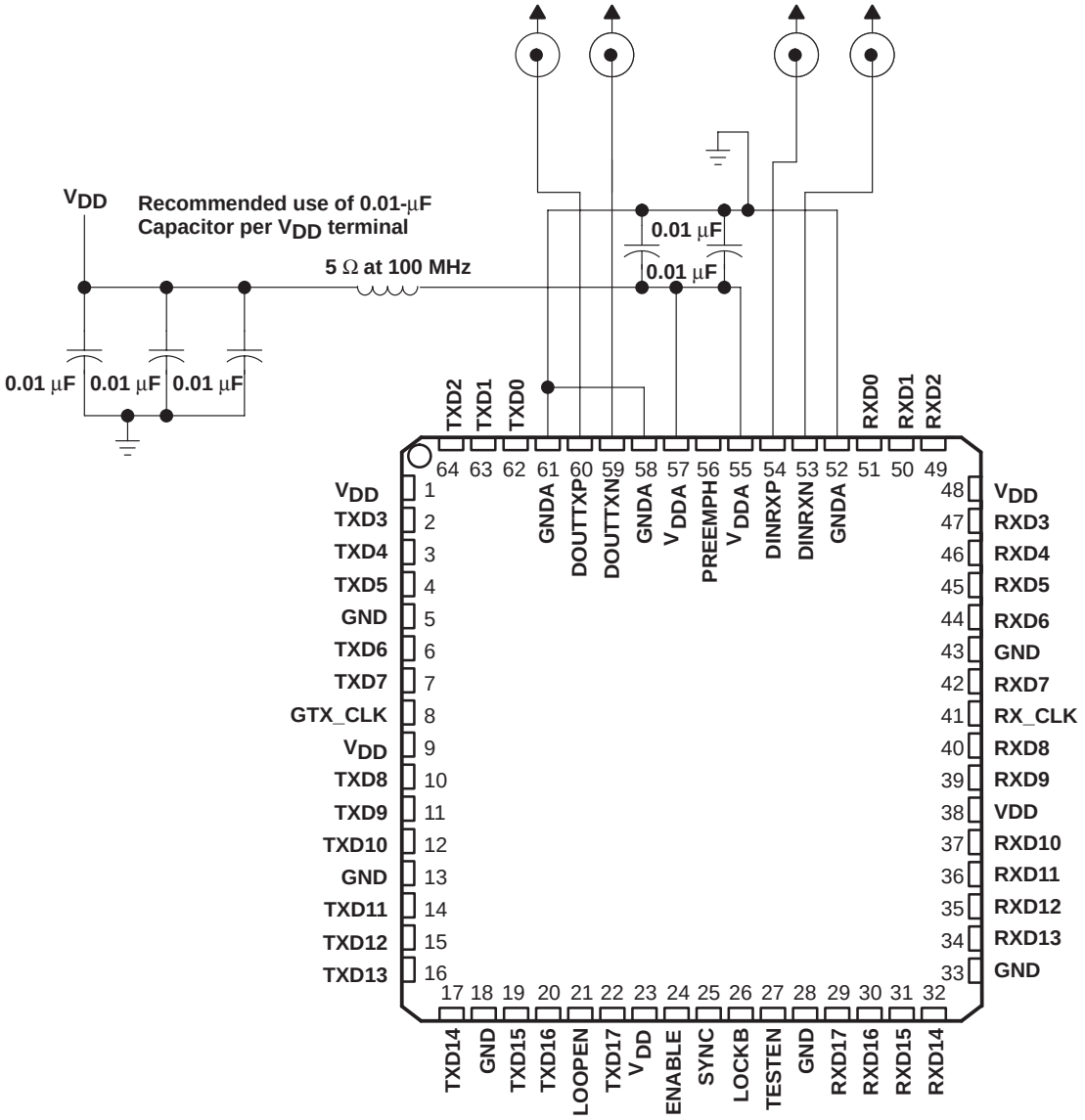



**Figure 10. External Component Interconnection**

**ORDERING INFORMATION**

| | Orderable |
|---|---|
| TLK2521 | TLK2521IPAP |

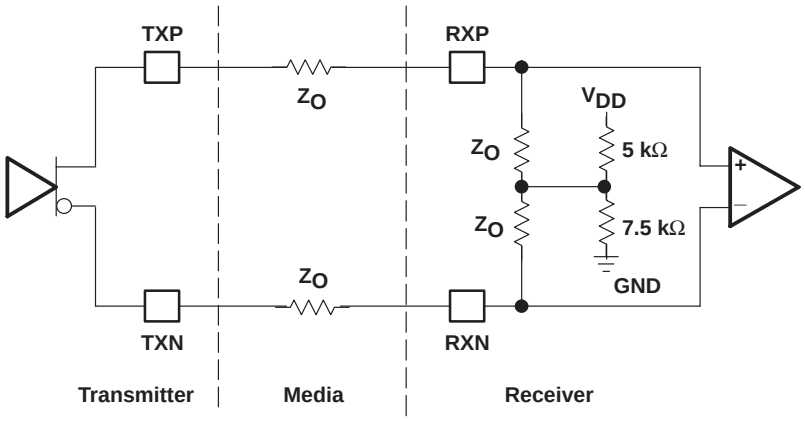



**Figure 11. High-Speed I/O Directly Coupled Mode**

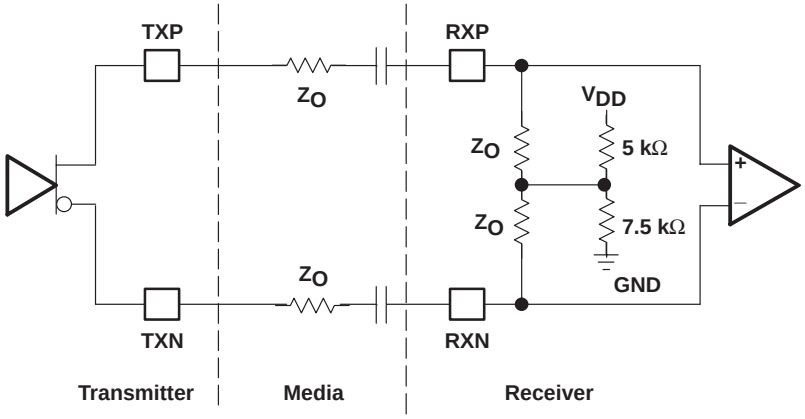



**Figure 12. High-Speed I/O AC-Coupled Mode**

AC-coupling is only recommended if the parallel TX data stream is encoded to achieve a dc-balanced data stream. Otherwise, the ac-caps can induce common-mode voltage drift due to the dc-unbalanced data stream.

## designing with PowerPAD

The TLK2521 is housed in a high-performance, thermally enhanced, 64-pin HTQFP (PAP64) PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. **It is strongly recommended that the PowerPAD be soldered to the thermal land.** The recommended convention, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keep out area for the 64-pin PAP PowerPAD package is 8 mm × 8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD™ Thermally Enhanced Package* application report, TI (SLMA002), available via the TI Web pages beginning at URL: http://www.ti.com.

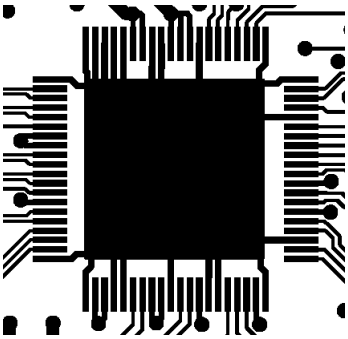


**Figure 13. Example of a Thermal Land**

For the TLK2521, this thermal land should be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground pin landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal pins. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI (SLLA020).

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