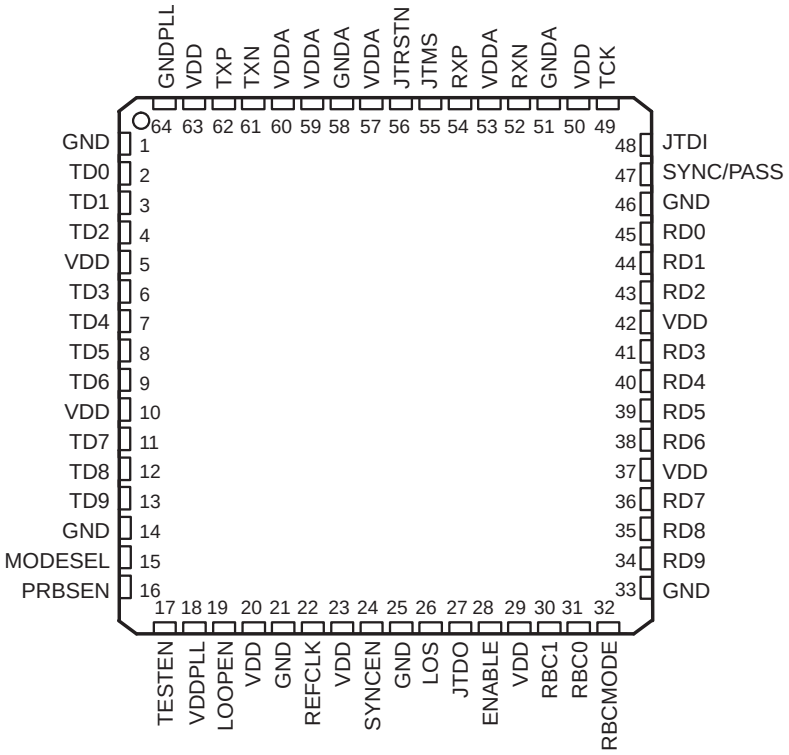
FEATURES

- **0.6-Gbps to 1.3-Gbps Serializer/Deserializer**
- **Low Power Consumption <200 mW at 1.25 Gbps**
- **LVPECL Compatible Differential I/O on High Speed Interface**
- **Single Monolithic PLL Design**
- **Support For 10-Bit Interface or Reduced Interface 5-Bit DDR (Double Data Rate) Clocking**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **IEEE 802.3 Gigabit Ethernet Compliant**
- **ANSI X3.230-1994 (FC-PH) Fibre Channel Compliant**
- **Advanced 0.25-µm CMOS Technology**
- **No External Filter Capacitors Required**
- **Comprehensive Suite of Built-In Testability**
- **IEEE 1149.1 JTAG Support**
- **2.5-V Supply Voltage for Lowest Power Operation**
- **3.3-V Tolerant on LVTTL Inputs**
- **Hot Plug Protection**
- **64-Pin VQFP With Thermally Enhanced Package (PowerPAD™)**
- **CPRI Data Rate Compatible (614 Mbps, 1.22 Gbps)**
- **Industrial Temperature Range Supported: –40°C to 85°C**



DESCRIPTION

The TLK1201A/TLK1201AI gigabit ethernet transceiver provides for ultrahigh-speed, full-duplex, point-to-point data transmissions. This device is based on the timing requirements of the 10-bit interface specification by the IEEE 802.3 gigabit ethernet specification and is also compliant with the ANSI X3.230-1994 (FC-PH) fibre channel standard. The device supports data rates from 0.6 Gbps to 1.3 Gbps.

The primary application of the transceiver is to provide building blocks for point-to-point baseband data transmission over controlled impedance media of 50 Ω or 75 Ω. The transmission media can be printed-circuit board traces, copper cables, or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

The transceiver performs the data serialization, deserialization, and clock extraction functions for a physical layer interface device. The transceiver operates at 1.25 Gbps (typical), providing up to 1 Gbps of data bandwidth over a copper or optical media interface.

The transceiver supports both the defined 10-bit interface (TBI) and a reduced 5-bit interface utilizing double data rate (DDR) clocking. In the TBI mode the serializer/deserializer (SERDES) accepts 10-bit wide 8b/10b parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially at PECL compatible voltage levels. The SERDES extracts clock information from the input serial stream and deserializes the data, outputting a parallel 10-bit data byte.

In the DDR mode the parallel interface accepts 5-bit wide 8b/10b encoded data aligned on both the rising and falling edges of the reference clock. The data is clocked most significant bit first (bits 0–4 of the 8b/10b encoded data) on the rising edge of the clock and the least significant bits (bits 5–9 of the 8b/10b encoded data) are clocked on the falling edge of the clock.

The transceiver provides a comprehensive series of built-in tests for self-test purposes including loopback and pseudorandom binary sequence (PRBS) generation and verification. An IEEE 1149.1 JTAG port is also supported.

The transceiver is housed in a high-performance, thermally enhanced, 64-pin VQFP PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. It is recommended that the device PowerPAD be soldered to the thermal land on the board.

The transceiver is characterized for operation from 0°C to 70°C (TLK1201A) or –40°C to 85°C (TLK1201AI).

The transceiver uses a 2.5-V supply. The I/O section is 3.3-V compatible. With a 2.5-V supply the chipset is very power-efficient, dissipating less than 200 mW typical power when operating at 1.25 Gbps.

The transceiver is designed to be hot plug capable. A power-on reset causes RBC0, RBC1, the parallel output signal terminals, TXP, and TXN to be held in a high-impedance state.

Differences Between TLK1201A/TLK1201AI and TNETE2201

The TLK1201A/TLK1201AI transceiver is the functional equivalent of the TNETE2201. There are several differences between the devices as noted below. See Figure 12 in the *Application Information* section for an example of a typical application circuit.

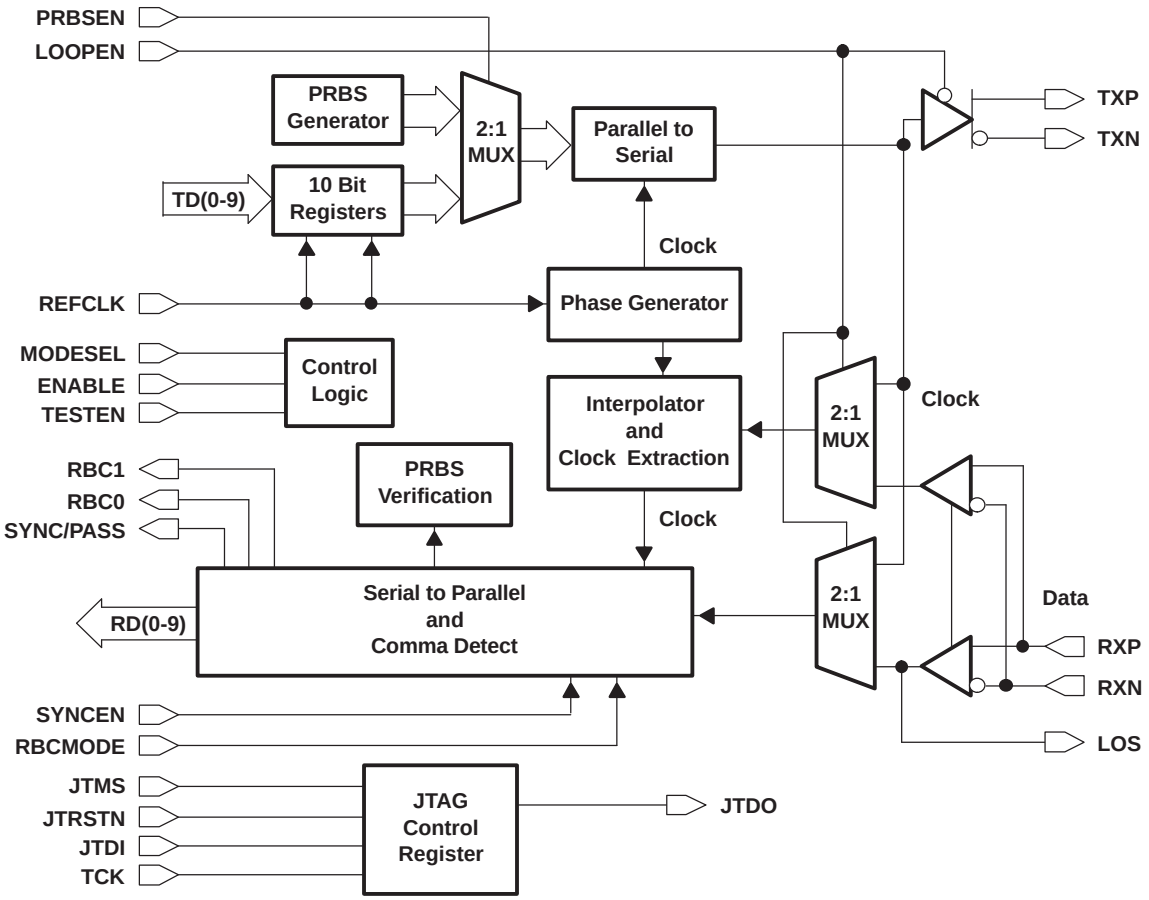
- The V_{CC} is 2.5 V for the TLK1201A vs 3.3 V for TNETE2201.
- The PLL filter capacitors on terminals 16, 17, 48, and 49 of the TNETE2201 are no longer required. The TLK1201A uses these terminals to provide added test capabilities. The capacitors, if present, do not affect the operation of the device.
- No pulldown resistors are required on the TXP/TXN outputs.

AVAILABLE OPTIONS

T_A	PACKAGE(1)
	PLASTIC QUAD FLAT PACK (RCP)
0°C to 70°C	TLK1201ARCP
–40°C to 85°C	TLK1201AIRCP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SIGNAL			
MODESEL	15	I P/D(1)	Mode select. This terminal selects between the 10-bit interface and a reduced 5-bit DDR interface. When low, the 10-bit interface (TBI) is selected. When pulled high, the 5-bit DDR mode is selected. The default mode is the TBI.
LOS	26	O	Loss of signal. Indicates a loss of signal on the high-speed differential inputs RXP and RXN. If the magnitude of RXP-RXN > 150 mV, then LOS = 1 which is a valid input signal. If the magnitude of RXP-RXN > 50 mV and < 150 mV, then LOS is undefined. If the magnitude of RXP-RXN < 50 mV, then LOS = 0 which is a loss of signal.
RBCMODE	32	I P/D(1)	Receive clock mode select. When RBCMODE and MODESEL are low, half-rate clocks are output on RBC0 and RBC1. When MODESEL is low and RBCMODE is high, a full baud-rate clock is output on RBC0 and RBC1 is held low. When MODESEL is high, RBCMODE is ignored and a full baud-rate clock is output on RBC0 and RBC1 is held low.
RBC0 RBC1	31 30	O	Receive byte clock. RBC0 and RBC1 are recovered clocks used for synchronizing the 10-bit output data on RD0–RD9. The operation of these clocks is dependent upon the receive clock mode selected. In the half-rate mode, the 10-bit output data words are valid on the rising edges of RBC0 and RBC1. These clocks are adjusted to half-word boundaries in conjunction with synchronous detect. The clocks are always expanded during data realignment and never slivered or truncated. RBC0 registers bytes 1 and 3 of received data. RBC1 registers bytes 0 and 2 of received data. In the normal rate mode, only RBC0 is valid and operates at 1/10th the serial data rate. Data is aligned to the rising edge. In the DDR mode, only RBC0 is valid and operates at 1/10th the serial data rate. Data is aligned on both the rising and falling edges.

(1) P/D = Internal pulldown

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RD0–RD9	45, 44, 43, 41, 40, 39, 38, 36, 35, 34	O	Receive data. When in TBI mode (MODESEL = low), these outputs carry 10-bit parallel data output from the transceiver to the protocol layer. The data is referenced to terminals RBC0 and RBC1, depending on the receive clock mode selected. RD0 is the first bit received. When in the DDR mode (MODESEL = high), only RD0–RD4 are valid. RD5–RD9 are held low. The 5-bit parallel data is clocked out of the transceiver on the rising edge of RBC0.
REFCLK	22	I	Reference clock. REFCLK is an external input clock that synchronizes the receiver and transmitter interface (60 MHz to 130 MHz). The transmitter uses this clock to register the input data (TD0–TD9) for serialization. In the TBI mode that data is registered on the rising edge of REFCLK. In the DDR mode, the data is registered on both the rising and falling edges of REFCLK with the most significant bits aligned on the rising edge of REFCLK.
RXP RXN	54 52	PECL I	Differential input receive. RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
SYNCEN	24	I P/U(2)	Synchronous function enable. When SYNCEN is high, the internal synchronization function is activated. When this function is activated, the transceiver detects the K28.5 comma character (0011111 negative beginning disparity) in the serial data stream and realigns data on byte boundaries if required. When SYNCEN is low, serial input data is unframed in RD0–RD9.
SYNC/PASS	47	O	Synchronous detect. The SYNC output is asserted high upon detection of the comma pattern in the serial data path. SYNC pulses are output only when SYNCEN is activated (asserted high). In PRBS test mode (PRBSEN = high), SYNC/PASS outputs the status of the PRBS test results (high = pass).
TD0–TD9	2-4, 6-9, 11-13	I	Transmit data. When in the TBI mode (MODESEL = low) these inputs carry 10-bit parallel data output from a protocol device to the transceiver for serialization and transmission. This 10-bit parallel data is clocked into the transceiver on the rising edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit. When in the DDR mode (MODESEL = high) only TD0–TD4 are valid. The 5-bit parallel data is clocked into the transceiver on the rising and falling edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit.
TXP TXN	62 61	PECL O	Differential output transmit. TXP and TXN are differential serial outputs that interface to a copper or an optical I/F module. TXP and TXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low.
TEST			
ENABLE	28	I P/U(3)	When this terminal is low, the device is disabled for Iddq testing. RD0–RD9, RBCn, TXP, and TXN are high impedance. The pullup and pulldown resistors on any input are disabled. When ENABLE is high, the device operates normally.
JTDI	48	I P/U(3)	Test data input. IEEE1149.1 (JTAG)
JTDO	27	O	Test data output. IEEE1149.1 (JTAG)
JTMS	55	I P/U(3)	Test mode select. IEEE1149.1 (JTAG)
JTRSTN	56	I P/U(3)	Reset signal. IEEE1149.1 (JTAG)
LOOPEN	19	I P/D(4)	Loop enable. When LOOPEN is high (active), the internal loop-back path is activated. The transmitted serial data is directly routed to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The TXP and TXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
PRBSEN	16	I P/D(4)	PRBS enable. When PRBSEN is high, the PRBS generation circuitry is enabled. The PRBS verification circuit in the receive side is also enabled. A PRBS signal can be fed to the receive inputs and checked for errors, that are reported by the SYNC/PASS terminal indicating low.
TCK	49	I	Test clock. IEEE1149.1 (JTAG)
TESTEN	17	I P/D(4)	Manufacturing test terminal

(2) P/U = Internal pullup
(3) P/U = Internal pullup
(4) P/D = Internal pulldown

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
POWER			
VDD	5, 10, 20, 23, 29, 37, 42, 50, 63	Supply	Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
VDDA	53, 57, 59, 60	Supply	Analog power. VDDA provides power for the high-speed analog circuits, receiver, and transmitter
VDDPLL	18	Supply	PLL power. Provides power for the PLL circuitry. This terminal requires additional filtering.
GROUND			
GND	1, 14, 21,25, 33, 46	Ground	Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers.
GNDA	51, 58	Ground	Analog ground. GNDA provides a ground for the high-speed analog circuits RX and TX.
GNDPLL	64	Ground	PLL ground. Provides a ground for the PLL circuitry.

DETAILED DESCRIPTION

Data Transmission

This device supports both the defined 10-bit interface (TBI) and a reduced 5-bit interface utilizing DDR clocking. When MODESEL is low, the TBI mode is selected. When MODESEL is high, the DDR mode is selected.

In the TBI mode, the transmitter portion registers incoming 10-bit wide data words (8b/10b encoded data, TD0–TD9) on the rising edge of REFCLK. The REFCLK is also used by the serializer, which multiplies the clock by a factor of 10, providing a signal that is fed to the shift register. The 8b/10b encoded data is transmitted sequentially bits 0 through 9 over the differential high-speed I/O channel.

In the DDR mode, the transmitter accepts 5-bit wide 8b/10b encoded data on pins TD0–TD4. In this mode, data is aligned to both the rising and falling edges of REFCLK. The data is then formed into a 10-bit wide word and sent to the serializer. The rising edge REFCLK clocks in bits 0–4, and the falling edge of REFCLK clocks in bits 5–9. Bit 0 is the first bit transmitted.

Transmission Latency

Data transmission latency is defined as the delay from the initial 10-bit word load to the serial transmission of bit 9. The minimum latency in TBI mode is 19 bit times. The maximum latency in TBI mode is 20 bit times. The minimum latency in DDR mode is 29 bit times, and maximum latency in DDR mode is 30 bit times.

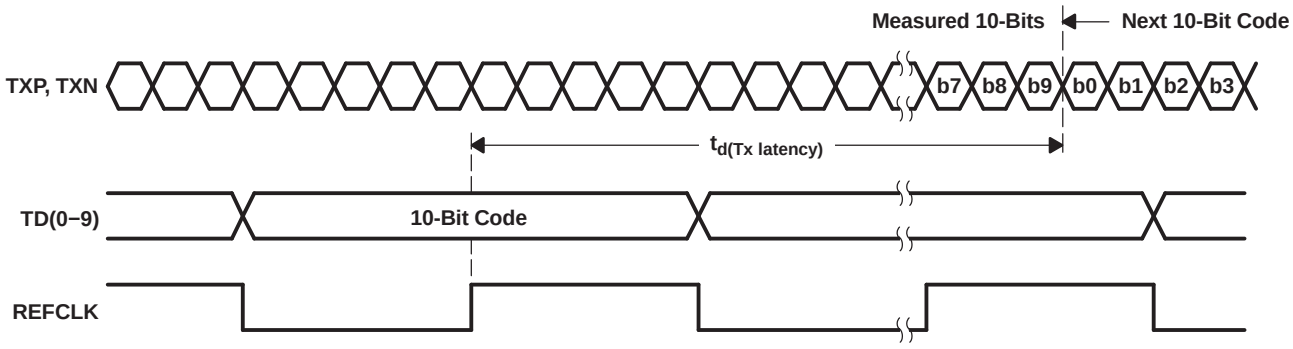


Figure 1. Transmitter Latency Full Rate Mode

Data Reception

The receiver portion deserializes the differential serial data. The serial data is retimed based on an interpolated clock generated from the reference clock. The serial data is then aligned to the 10-bit word boundaries and presented to the protocol controller along with receive byte clocks (RBC0 and RBC1).

Receiver Clock Select Mode

There are two modes of operation for the parallel bus: 1) the 10-bit (TBI) mode and 2) 5-bit (DDR) mode. When in TBI mode, there are two user-selectable clock modes that are controlled by the RBCMODE terminal: 1) full-rate clock on RBC0 and 2) half-rate clocks on RBC0 and RBC1. When in the DDR mode, only a full-rate clock is available on RBC0; see Table 1.

Table 1. Mode Selection

MODESEL	RBCMODE	MODE	RECEIVE BYTE CLOCK	
			TLK1201A	TLK1201AI
0	0	TBI half-rate	30–65 MHz	30–65 MHz
0	1	TBI full-rate	60–130 MHz	60–130 MHz
1	0	DDR	60–130 MHz	60–130 MHz
1	1	DDR	60–130 MHz	60–130 MHz

In the half-rate mode, two receive byte clocks (RBC0 and RBC1) are 180 degrees out of phase and operate at one-half the data rate. The clocks are generated by dividing down the recovered clock. The received data is output with respect to the two receive byte clocks (RBC0 and RBC1) allowing a protocol device to clock the parallel bytes using the RBC0 and RBC1 rising edges. The outputs to the protocol device, byte 0 of the received data is valid on the rising edge of RBC1. See the timing diagram shown in Figure 2.

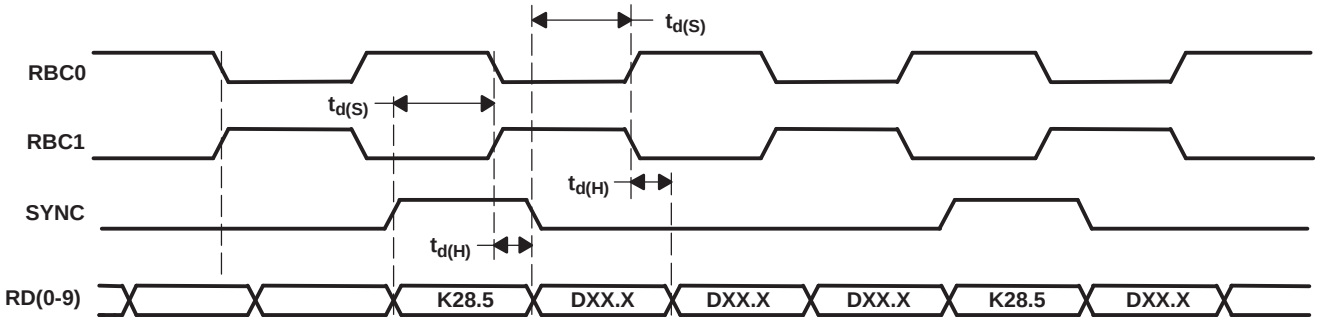


Figure 2. Synchronous Timing Characteristics Waveforms (TBI Half-Rate Mode)

In the normal-rate mode, only RBC0 is used and operates at full data rate (that is, 1.25-Gbps data rate produces a 125-MHz clock). The received data is output with respect to the rising edge of RBC0. RBC1 is low in this mode. See the timing diagram shown in Figure 3.

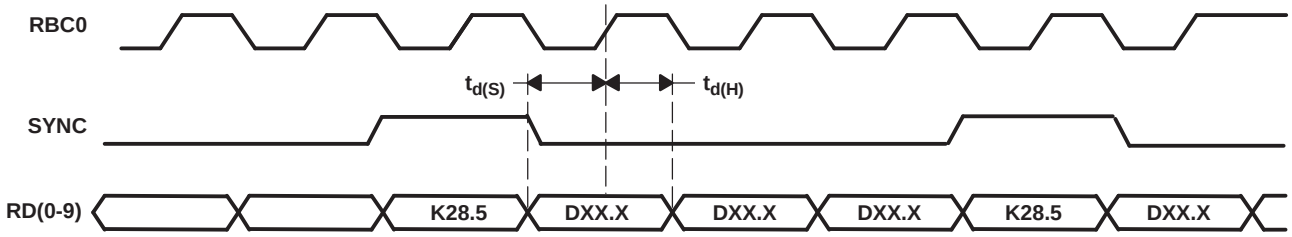


Figure 3. Synchronous Timing Characteristics Waveforms (TBI Full-Rate Mode)

In the double data rate mode, the receiver presents the data on both the rising and falling edges of RBC0. RBC1 is low impedance. The data is clocked bit 0 first, and aligned to the rising edge of RBC0. See the timing diagram shown in Figure 4.

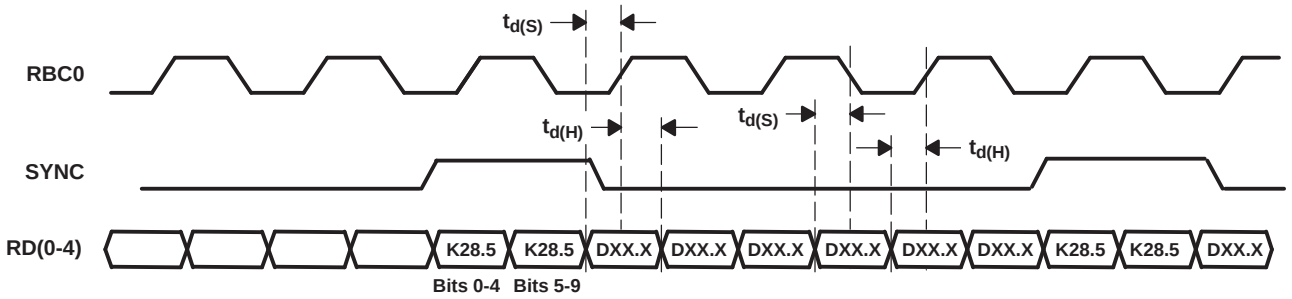


Figure 4. Synchronous Timing Characteristics Waveforms (DDR Mode)

The receiver clock interpolator can lock to the incoming data without the need for a lock-to-reference preset. The received serial data rate (RXP and RXN) is at the same baud rate as the transmitted data stream, 0.02% (200 PPM) for proper operation (see the recommended operating tables).

Receiver Word Alignment

This device uses the IEEE 802.3 gigabit ethernet defined 10-bit K28.5 character (comma character) word alignment scheme. The following sections explain how this scheme works and how it realigns itself.

Comma Character on Expected Boundary

This device provides 10-bit K28.5 character recognition and word alignment. The 10-bit word alignment is enabled by forcing the SYNCEN terminal high. This enables the function that examines and compares serial input data to the 7-bit synchronization pattern. The K28.5 character is defined by 8-bit/10-bit coding scheme as a pattern consisting of 0011111010 (a negative number beginning with disparity) with the 7 MSBs (0011111), referred to as the comma character. The K28.5 character was implemented specifically for aligning data words. As long as the K28.5 character falls within the expected 10-bit boundary, the received 10-bit data is properly aligned and data realignment is not required. Figure 2 shows the timing characteristics of RBC0, RBC1, SYNC, and RD0–RD9 while synchronized. (Note: the K28.5 character is valid on the rising edge of RBC1.)

Comma Character Not on Expected Boundary

If synchronization is enabled and a K28.5 character straddles the expected 10-bit word boundary, then word realignment is necessary. Realignment or shifting the 10-bit word boundary truncates the character following the misaligned K28.5, but the following K28.5 and all subsequent data is aligned properly as shown in Figure 5. The RBC0 and RBC1 pulse widths are stretched or stalled in their current state during realignment. With this design, the maximum stretch that occurs is 20 bit times. This occurs during a worst case scenario when the K28.5 is aligned to the falling edge of RBC1 instead of the rising edge. Figure 5 shows the timing characteristics of the data realignment.

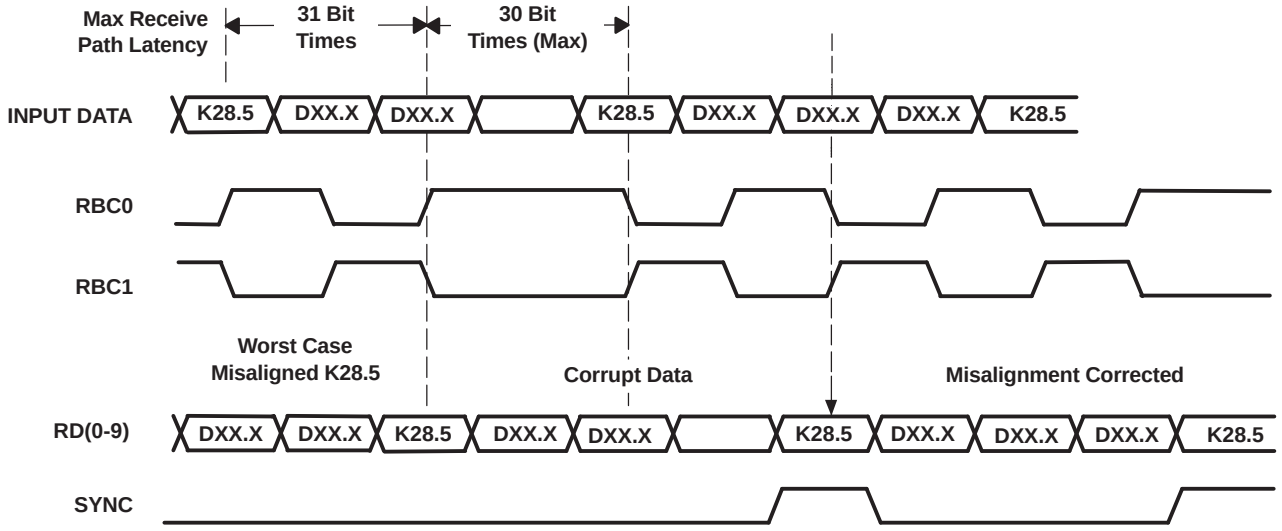


Figure 5. Word Realignment Timing Characteristics Waveforms

Systems that do not require framed data may disable byte alignment by tying SYNCEN low.

When a SYNC character is detected, the SYNC signal is brought high and is aligned with the K28.5 character. The duration of the SYNC pulse is equal to the duration of the data when in TBI mode. When in DDR mode the SYNC pulse is present for the entire RBC0 period.

Data Reception Latency

The serial-to-parallel data latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RD0 received as first bit. The minimum latency in TBI mode is 21 bit times, and the maximum latency is 31 bit times. The minimum latency in DDR mode is 27 bit times and maximum latency is 34 bit times.

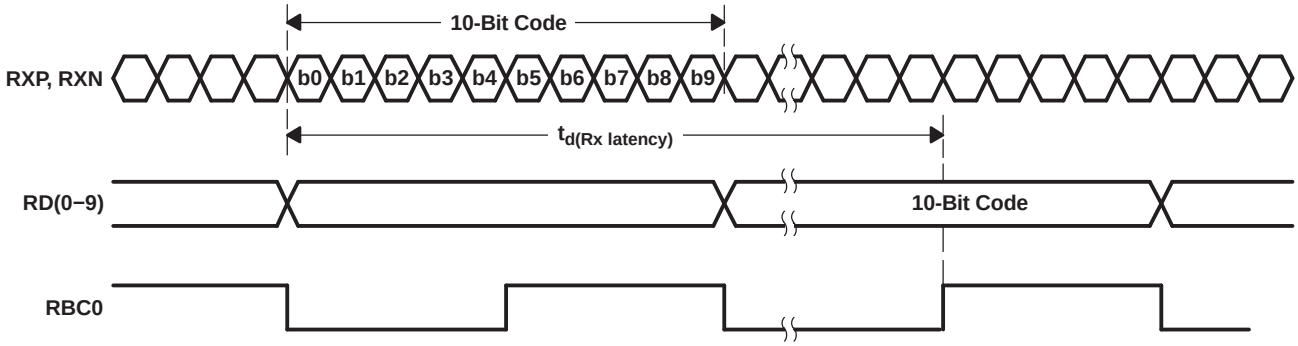


Figure 6. Receiver Latency - TBI Normal Mode Shown

Loss of Signal Detection

This device has a loss-of-signal (LOS) detection circuit for conditions where the incoming signal no longer has sufficient voltage level to keep the clock recovery circuit in lock. The LOS is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. Under a PRBS serial input pattern, LOS is high for signal amplitudes greater than 150 mV. The LOS is low for all amplitudes below 50 mV. Between 50 mV and 150 mV, LOS is undetermined.

Testability

The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable function allows for all circuitry to be disabled so that an Iddq test can be performed. The PRBS function also allows for a BIST (built-in self test). The terminal setting, TESTEN high, enables the test mode. The terminal TESTEN has an internal pulldown resistor, so it defaults to normal operation. The TESTEN is only used for factory testing, and is not intended for end-user control.

Loopback Testing

The transceiver can provide a self-test function by enabling (setting LOOPEN to high level) the internal loopback path. Enabling this function causes serial transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. The external differential output is held in a high-impedance state during the loopback testing.

Enable Function

When held low, ENABLE disables all quiescent power in both the analog and digital circuitry. This allows an ultralow-power idle state when the link is not active.

PRBS Function

This device has a built-in 2^7–1 PRBS function. When the PRBSEN control bit is set high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel transmitter input bus. Data from the normal parallel input source is ignored during PRBS test mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT) or to the receiver of another TLK1201AI. Since the PRBS is not really random and is really a predetermined sequence of 1s and 0s, the data can be captured and checked for errors by a BERT. This device also has a built-in BERT function on the receiver side that is enabled by PRBSEN. It can receive a PRBS pattern and check for errors, and then reports the errors by forcing the SYNC/PASS terminal low. When PRBS is enabled, RBCMODE is ignored. MODESEL must be low for the PRBS verifier to function correctly. The PRBS testing supports two modes (normal and latched), which are controlled by the SYNCEN input. When SYNCEN is low, the result of the PRBS bit error rate test is passed to the SYNC/PASS terminal. When SYNCEN is high the result of the PRBS verification is latched on the SYNC/PASS output (that is, a single failure forces SYNC/PASS to remain low).

JTAG

The TLK1201A supports an IEEE1149.1 JTAG function while maintaining compatibility with the industry standard 64 pin QFP package footprint. In this way, the TLK1201A installed on a board layout that was designed for the industry standard footprint such as for the TNETE2201B. (Provided the supply voltage can be programmed from the older 3.3 V to 2.5 V.) The JTAG pins on the TLK1201A are chosen to either be on the ‘vender-unique’ pins of the industry standard footprint, or are on pins that were previously power or ground. The TRSTN pin has been placed on pin 56, which is a ground on the industry standard footprint. In this way, a TLK1201A installed onto the older footprint has the JTAG tap controller held in reset, and thus disabled. If the JTAG function is desired, then the 5 JTAG pins TRSTN, TMS, TCK, TDI, and TDO can be used in the usual manner for a JTAG function. If the JTAG function is not desired, then connecting TRSTN to ground is recommended. TMS and TDI have internal pullup resistors, and can thus be left unconnected if not used. TDO is an output and should be left unconnected if JTAG is not used. TCK does not have an internal pullup, and can be tied to GND or PWR if not used, but with TRSTN low, this input is not used, and thus can be left unconnected.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		TLK1201A/TLK1201AI
Supply voltage, V_{DD} (see (2))		–0.3 V to 3 V
Input voltage range at TTL terminals, V_I		–0.5 V to 4 V
Input voltage range at any other terminal		–0.3 V to V_{DD} +0.3 V
Storage temperature, T_{stg}		–65°C to 150°C
Electrostatic discharge		CDM: 1 kV, HBM:2 kV
Characterized free-air operating temperature range	TLK1201A	0°C to 70°C
	TLK1201AI	–40°C to 85°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
RCP64(2)	5.25 W	46.58 mW/°C	2.89 W
RCP64(3)	3.17 W	23.70 mW/°C	1.74 W
RCP64(4)	2.01 W	13.19 mW/°C	1.11 W

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\Theta JA}$).
(2) 2 oz. Trace and copper pad with solder
(3) 2 oz. Trace and copper pad without solder
(4) Standard JEDEC high-K board

Thermal Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{\Theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		21.47		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		42.2		
		Board-mounted, no air flow, JEDEC test board		75.83		
$R_{\Theta JC}$	Junction-to-case-thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		0.38		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		0.38		
		Board-mounted, no air flow, JEDEC test board		7.8		

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, $V_{DD(A)}$		2.3	2.5	2.7	V
Total supply current, I_{DD}, $I_{DD(A)}$	Frequency = 1.25 Gbps, PRBS pattern			90	mA
Total power dissipation, P_D	Frequency = 1.25 Gbps, PRBS pattern		250		mW
	Frequency = 1.25 Gbps, worst case(1)			245	mW
Total shutdown current, I_{DD}, $I_{DD(A)}$	Enable = 0, $V_{DD(A)}$, V_{DD} = 2.7 V			50	µA
Startup lock time, PLL	V_{DD}, $V_{DD(A)}$ = 2.5 V, EN↑ to PLL acquire			500	µs
Operating free-air temperature, T_A	TLK1201A	0		70	°C
	TLK1201AI	-40		85	

(1) The worst case pattern is a pattern that creates a maximum transition density on the serial transceiver.

REFERENCE CLOCK (REFCLK) TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	TLK1201A	TYP–0.01%	60	TYP+0.01%	MHz
		TLK1201AI	TYP–0.01%	60	TYP+0.01%	
Frequency	Maximum data rate		TYP–0.01%	130	TYP+0.01%	
Accuracy			100		100	ppm
Duty cycle			40%	50%	60%	
Jitter	Random plus deterministic				40	ps

TTL ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –400 µA	V_{DD}–0.2	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND	0.25	0.5	V
V_{IH}	High-level input voltage		1.7		3.6	V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level Input current	V_{DD} = 2.3 V, V_{IN} = 2 V			40	µA
I_{IL}	Low-level Input current	V_{DD} = 2.3 V, V_{IN} = 0.4 V	–40			µA
C_{IN}	Input capacitance				4	pF

TRANSMITTER/RECEIVER CHARACTERISTICS

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
	V_{OD} = |TxD-TxN|		R_t = 50Ω	600	850	1100	mV
			R_t = 75 Ω	800	1050	1200	
$V_{(cm)}$	Transmit common mode voltage range		R_t = 50Ω	1100	1250	1400	mV
			R_t = 75 Ω				
	Receiver input voltage requirement, V_{ID} = |RxP - RxN|			200		1600	mV
	Receiver common mode voltage range, (RxP + RxN)/2			1000	1250	2250	mV
$I_{lkg(R)}$	Receiver input leakage current			-350		350	µA
C_I	Receiver input capacitance					2	pF
$t_{(TJ)}$	Serial data total jitter (peak-to-peak)		Differential output jitter, Random + deterministic, PRBS pattern, R_ω = 125 MHz			0.24	UI
			Differential output jitter, Random + deterministic, PRBS pattern, R_ω = 106.25 MHz			0.2	UI
$t_{(DJ)}$	Serial data deterministic jitter (peak-to-peak)		Differential output jitter, PRBS pattern, R_ω = 125 MHz			0.10	UI
t_r, t_f	Differential signal rise, fall time (20% to 80%)		R_L = 50 Ω, C_L = 5 pF, See Figure 7	100		250	ps
	Serial data jitter tolerance minimum required eye opening, (per IEEE-802.3 specification)		Differential input jitter, Random + deterministic, R_ω = 125 MHz	0.25			UI
			Differential input jitter, random + determinisitc, PRBS pattern at zero crossing	0.3			UI
	Receiver data acquisition lock time from powerup					500	µs
	Data relock time from loss of synchronization					1024	Bit times
$t_{d(Txlatency)}$	Tx latency	TBI modes	See Figure 1	19		20	UI
		DDR mode		29		30	
$t_{d(Rxlatency)}$	Rx latency	TBI modes	See Figure 6	20		31	UI
		DDR mode		27		34	
		TBI mode	600–620 Mbps	24		28	
		DDR mode	600–620 Mbps	27		31	
		TBI mode	1228.8 Mbps	25		29	
		DDR mode	1228.8 Mbps	27		33	

(1) UI = serial bit time

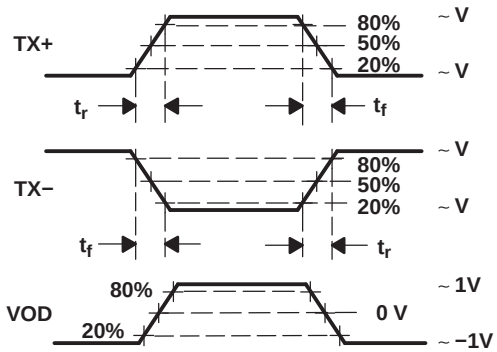


Figure 7. Differential and Common-Mode Output Voltage Definitions

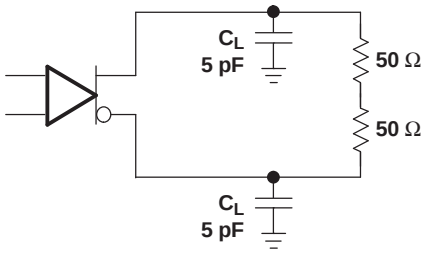


Figure 8. Transmitter Test Setup

LVTTL OUTPUT SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(RBC)}$	Clock rise time	80% to 20% output voltage, C = 5 pF (see Figure 9)	0.3		1.5	ns
$t_{f(RBC)}$	Clock fall time		0.3		1.5	
t_r	Data rise time		0.3		1.5	ns
t_f	Data fall time		0.3		1.5	
$t_{su(D1)}$	Data setup time (RD0–RD9), Data valid prior to RBC0 rising	TBI normal mode, (see Figure 3), R_ω = 125 MHz	2.5			ns
		TBI normal mode, (see Figure 3), R_ω = 61.44 MHz	5			
$t_{h(D1)}$	Data hold time (RD0–RD9), Data valid after RBC0 rising	TBI normal mode, (see Figure 3), R_ω = 125 MHz	2			ns
		TBI normal mode, (see Figure 3), R_ω = 61.44 MHz	4			
$t_{su(D2)}$	Data setup time (RD0–RD4)	DDR mode, R_ω = 125 MHz, (see Figure 4)	2			ns
$t_{h(D2)}$	Data hold time (RD0–RD4)	DDR mode, R_ω = 125 MHz, (see Figure 4)	0.8			ns
$t_{su(D3)}$	Data setup time (RD0–RD9)	TBI half-rate mode, R_ω = 125 MHz, (see Figure 2)	2.5			ns
$t_{h(D3)}$	Data hold time (RD0–RD9)	TBI half-rate mode, R_ω = 125 MHz, (see Figure 2)	1.5			ns

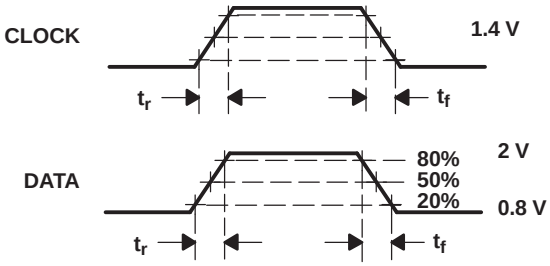


Figure 9. TTL Data I/O Valid Levels for AC Measurement

TRANSMITTER TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(D4)}$	Data setup time (TD0–TD9)	TBI modes	1.6			ns
$t_{h(D4)}$	Data hold time (TD0–TD9)		0.8			
$t_{su(D5)}$	Data setup time (TD0–TD9)	DDR modes	0.7			ns
$t_{h(D5)}$	Data hold time (TD0–TD9)		0.5			
t_r, t_f	TD[0,9] data rise and fall time	See Figure 9			2	ns

APPLICATION INFORMATION

8B/10B TRANSMISSION CODE

The PCS maps GMII signals into 10-bit code groups and vice versa, using an 8b/10b block coding scheme. The PCS uses the transmission code to improve the transmission characteristics of information to be transferred across the link. The encoding defined by the transmission code ensures that sufficient transitions are present in the PHY bit stream to make clock recovery possible in the receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. The 8b/10b transmission code specified for use has a high-transition density, is run length limited, and is dc-balanced. The transition density of the 8b/10b symbols range from 3 to 8 transitions per symbol. The definition of the 8b/10b transmission code is specified in IEEE 802.3 gigabit ethernet and ANSI X3.230-1994 (FC-PH), clause 11.

The 8b/10b transmission code uses letter notation describing the bits of an unencoded information octet. The bit notation of A,B,C,D,E,F,G,H for an unencoded information octet is used in the description of the 8b/10b transmission code-groups, where A is the LSB. Each valid code group has been given a name using the following convention: /Dx.y/ for the 256 valid data code-groups and /Kx.y/ for the special control code-groups, where y is the decimal value of bits EDCBA and x is the decimal value of bits HGF (noted as K<HGF.EDCBA>). Thus, an octet value of FE representing a code-group value of K30.7 would be represented in bit notation as 111 11110.

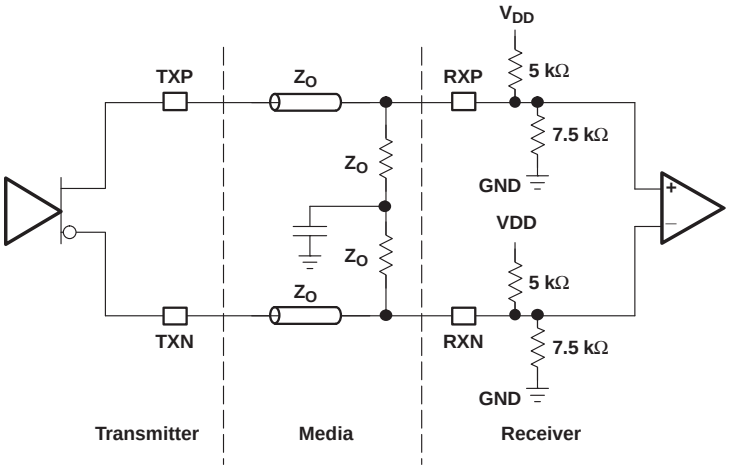


Figure 10. High-Speed I/O Directly-Coupled Mode

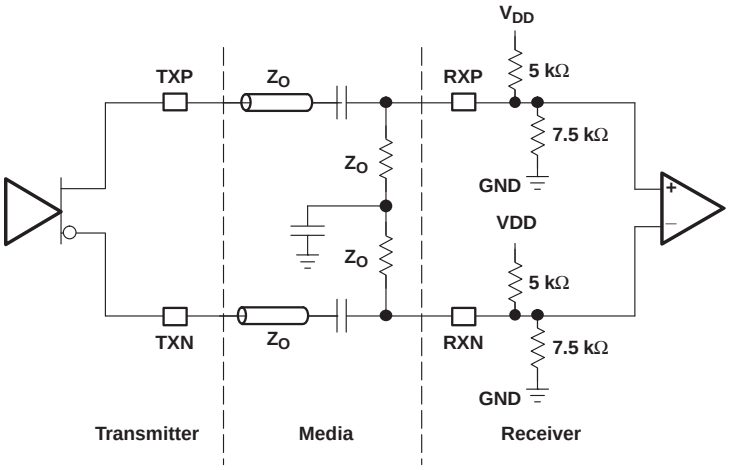


Figure 11. High-Speed I/O AC-Coupled Mode

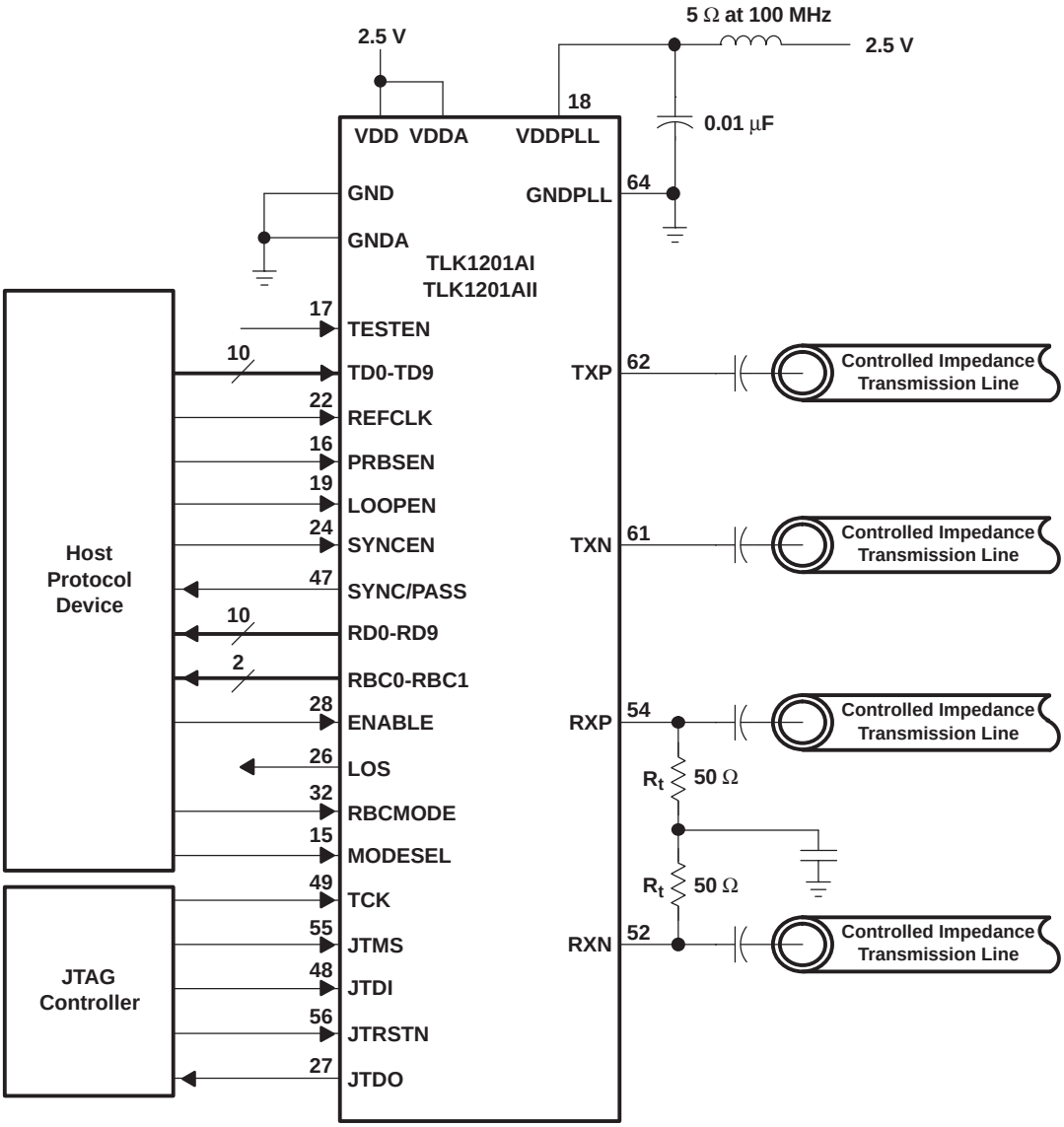


Figure 12. Typical Application Circuit (AC Mode)

DESIGNING WITH PowerPAD™

The TLK1201A/TLK1201AI is housed in a high-performance, thermally enhanced, 64-pin VQFP (RCP64) PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. It is strongly recommended that the PowerPAD be soldered to the thermal land. The recommended convention, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keepout area for the 64-pin PFP PowerPAD package is 8 mm ɔ8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com.

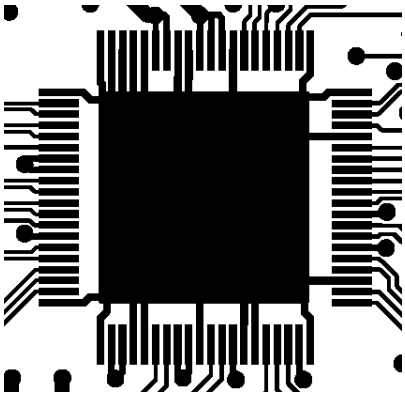


Figure 13. Example of a Thermal Land

For the TLK1201AI, this thermal land must be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size must be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low-impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

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