- **Complies With ITU G.992.2 Standard**
- **14-Bit Integrated A/D and D/A Converters**
- **1.104 Msps Update Rate for the RX Channel**
- **276 ksps Update Rate for the TX Channel**
- **Minimum 50 dB Missing Tone Rejection for DMT Signals**
- **Integrated TX/RX Filters**
- **Integrated Digital Phase Lock Loop (DPLL) and VCXO DAC**
- **Integrated Equalizer for Receive Channel**
- **Integrated PGA in Receive, and PAA in Transmit Channels**
- **Direct Single Serial Interface to TI's C54x or C6x DSP (Data and Control)**
- **Eight General-Purpose I/O Pins**
- **Software and Hardware Power-Down Modes**
- **Industrial Temperature Range (–40°C to 85°C)**
- **Integrated Auxiliary Amplifiers for System Flexibility**
- **Single 3.3 V Supply**
- **80-Pin LQFP (PN) Package**
- **2s Complement Data Format**

## description

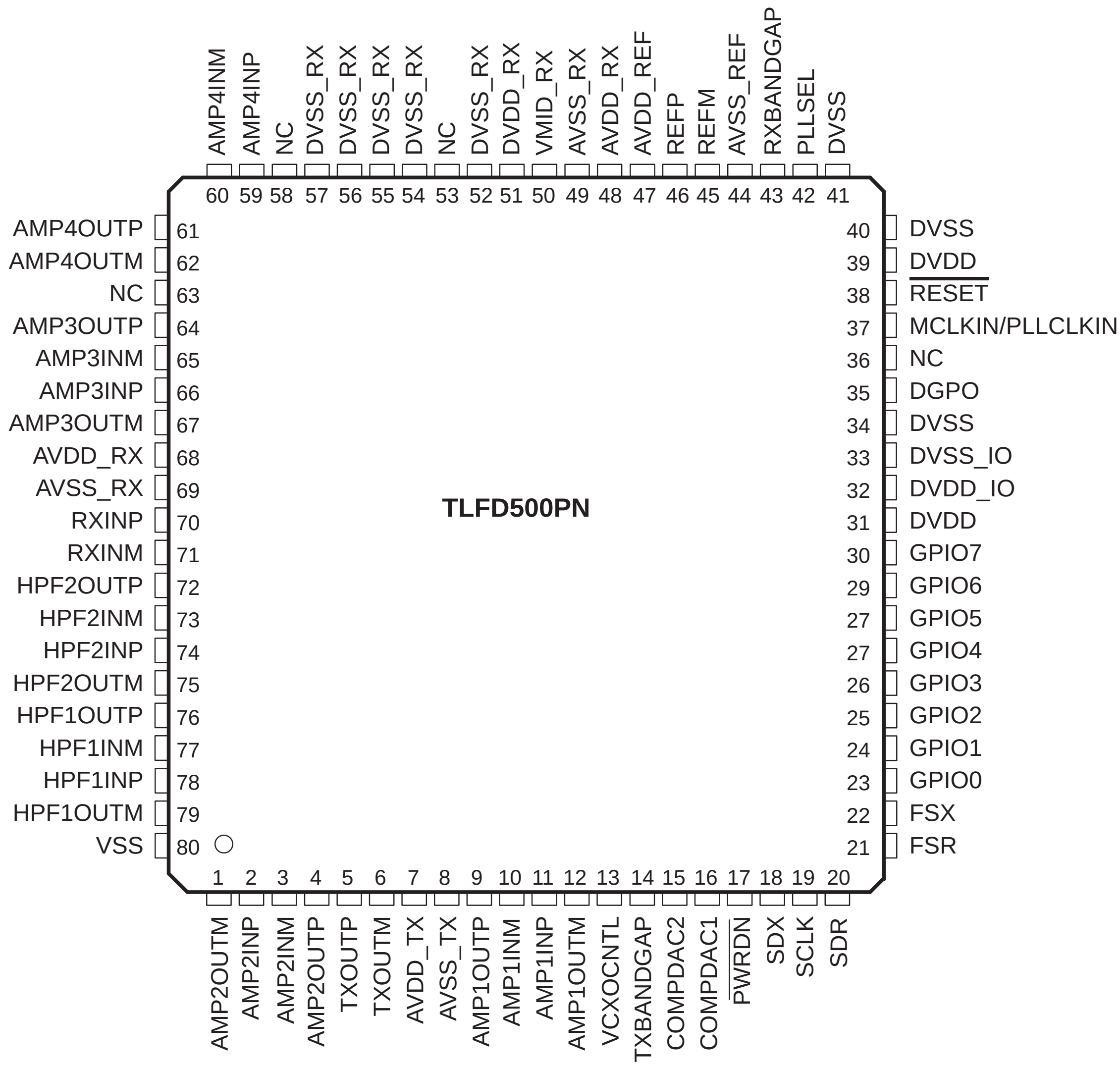
The TLFD500PN is a high-speed analog front end for a remote terminal-side ADSL G.Lite modem. The device is designed to perform transmit encoding (D/A conversion), receive decoding (A/D conversion), transmit and receive filtering functions, and receive equalizer functions for a frequency division multiplex (FDM) G.Lite application. The receive channel has an update rate of 1.104 Msps, while the transmit channel has an update rate of 276 ksps. Both channels use 2s complement data format.

When used in a G.Lite system, the TLFD500PN requires a minimum number of external components. The device incorporates integrated filtering, DPLL, VCXO DAC (uses 2s complement data format), and 8 general-purpose I/O ports. The general-purpose I/O ports provide a means of reading or writing status bits in the system. Four auxiliary amplifiers on the chip can be configured (external components may be required) to provide additional onboard filtering and amplification.

A simple serial interface for data transfer on the digital side reduces system component count. The interface can be connected directly to the TI C6x and C54x families of DSPs.

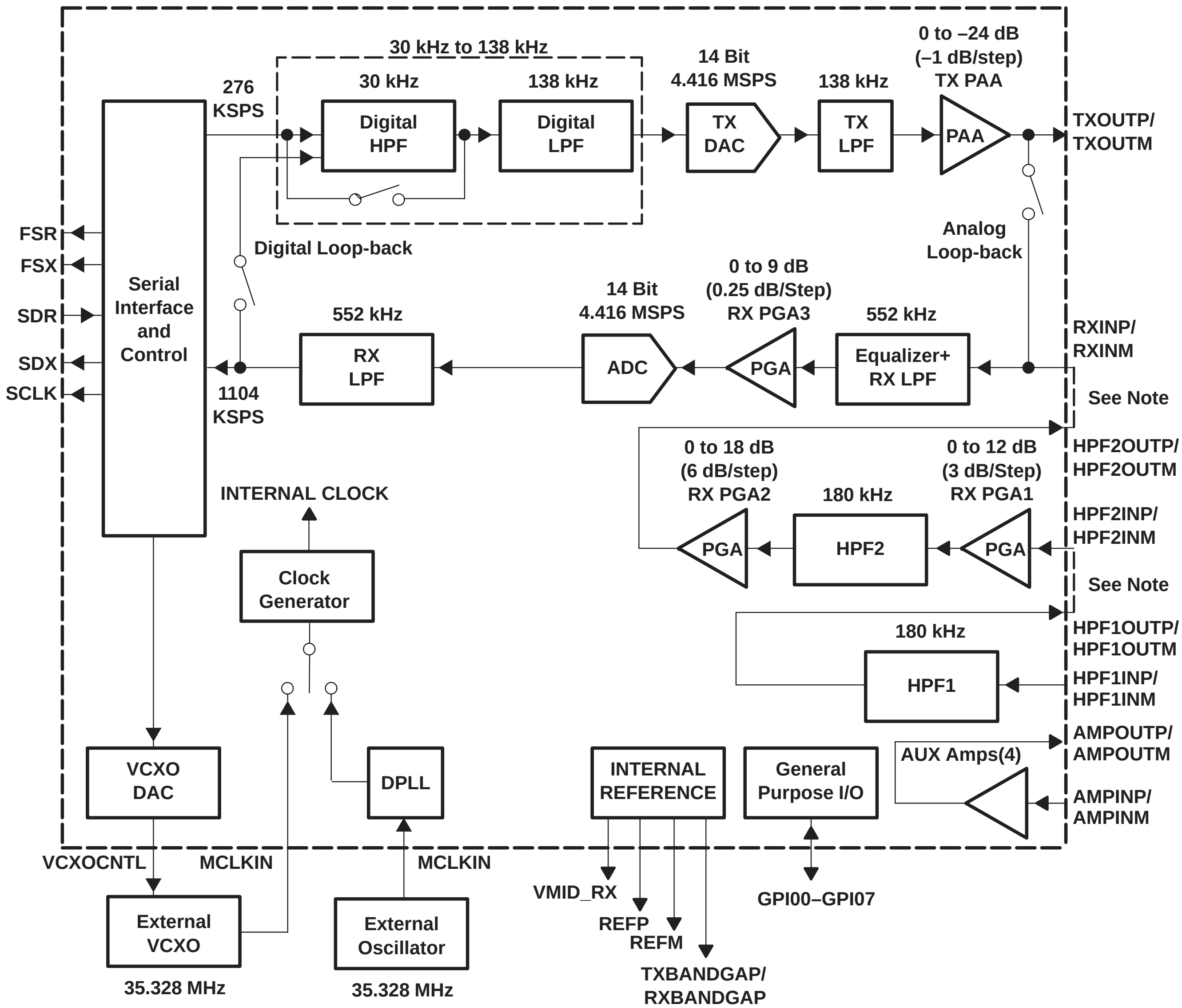
The TLFD500PN device is available in an 80-pin PN LQFP package.

**PN PACKAGE**
**(TOP VIEW)**




NC – No connection

## functional block diagram




NOTE: Refer to Figure 17 for application details.

## Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AMP1INP– AMP4INP | 11,2,66,59 | I | Auxiliary amplifier 1–4 positive input |
| AMP1INM– AMP4INM | 10,3,65,60 | I | Auxiliary amplifier 1–4 negative input |
| AMP1OUTP– AMP2OUTP | 9,4 | O | Auxiliary amplifier 1–2 positive output. Outputs are self-biased to AVDD_TX/2. |
| AMP3OUTP– AMP4OUTP | 64, 61 | O | Auxiliary amplifier 3–4 positive output. Outputs are self-biased to AVDD_RX/2. |
| AMP1OUTM– AMP2OUTM | 12,1 | O | Auxiliary amplifier 1–2 negative output. Outputs are self-biased to AVDD_TX/2. |
| AMP3OUTM– AMP4OUTM | 67,62 | O | Auxiliary amplifier 3–4 negative output. Outputs are self-biased to AVDD_RX/2. |
| AVDD_REF | 47 | I | Analog supply for reference circuit |
| AVDD_RX | 48,68 | I | RX channel analog supply |
| AVDD_TX | 7 | I | TX channel analog supply |
| AVSS_REF | 44 | I | Analog supply return for reference(analog ground) |
| AVSS_RX | 49,69 | I | RX channel analog supply return (analog ground) |
| AVSS_TX | 8 | I | TX channel analog supply return (analog ground) |
| COMPDAC1 | 16 | I | TX channel decoupling cap input A. Add 1 μF capacitor to AVDD_TX |
| COMPDAC2 | 15 | I | TX channel decoupling cap input B. Add 1 μF capacitor to AVDD_TX |
| DGPO | 35 | O | Direct general-purpose output. This pin reflects the last value written to the DGPO bit location in the SDR data stream. It is a general-purpose output that does not require a secondary transfer to control. |
| DVDD | 31,39 | I | Digital power supply |
| DVDD_IO | 32 | I | Digital I/O buffer supply |
| DVDD_RX | 51 | I | RX channel digital supply |
| DVSS | 34,40,41 | I | Digital ground |
| DVSS_IO | 33 | I | Digital I/O buffer supply return (digital ground) |
| DVSS_RX | 52,54,55, 56,57 | I | RX channel digital supply return (digital ground) |
| FSX | 22 | O | Serial port frame sync transmit signal |
| FSR | 21 | O | Serial port frame sync receive signal |
| GPIO0–GPIO7 | 23–30 | I/O | General-purpose I/O |
| HPF1INP | 78 | I | RX channel stage 1 amplifier positive input. Input signal needs to have AVDD_RX/2 common mode voltage. |
| HPF1INM | 77 | I | RX channel stage 1 amplifier negative input. Input signal needs to have AVDD_RX/2 common mode voltage. |
| HPF2INP | 74 | I | RX channel stage 2 positive input. Input signal need to have AVDD_RX/2 common mode voltage. |
| HPF2INM | 73 | I | RX channel stage 2 negative input. Input signal need to have AVDD_RX/2 common mode voltage. |
| HPF1OUTP | 76 | O | RX channel stage 1 amplifier positive output. Used to connect external components to obtain stage 1 HPF. |
| HPF1OUTM | 79 | O | RX channel stage 1 amplifier negative output. Used to connect external components to obtain stage 1 HPF. |
| HPF2OUTP | 72 | O | RX channel stage 2 positive output. Output signal has AVDD_RX/2 common mode voltage. |
| HPF2OUTM | 75 | O | RX channel stage 2 negative output. Output signal has AVDD_RX/2 common mode voltage. |
| MCLKIN/PLLCLKIN | 37 | I | Multiplexed pin based on value of PLLSEL. Selects master clock input, or clock input for PLL mode. |

## Terminal Functions (Continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| NC | 36,53, 58, 63 | | No connection. Keep floating. |
| PLLSEL | 42 | I | Selects between VCXO mode and DPLL mode. If the pin is tied high PLL mode is selected. Pin should be tied low for VCXO mode. Cannot be left floating. |
| $\overline{\text{PWRDN}}$ | 17 | I | Power-down pin. When $\overline{\text{PWRDN}}$ is pulled low the device goes into power-down mode. The default state of this pin is low. |
| REFM | 45 | O | Negative reference filter node. This terminal is provided for low-pass filtering of the internal band-gap reference. The optimal ceramic capacitor value is 10 µF (tantalum) and 0.1 µF (ceramic), connected to analog ground. The nominal dc voltage at this terminal is 0.5 V. |
| REFP | 46 | O | Positive reference filter node. This terminal is provided for low-pass filtering of the internal band-gap reference. The optimal ceramic capacitor value is 10 µF (tantalum) 0.1 µF (ceramic), connected to analog ground. The nominal dc voltage at this terminal is 2.5 V. |
| $\overline{\text{RESET}}$ | 38 | I | Device reset input pin. Initializes all the device's internal registers to their default values. The default state of this pin is low. |
| RXBANDGAP | 43 | O | RX channel band-gap filter node. This terminal is provided for decoupling of the 1.5-V band-gap reference. The optimal capacitor value is 10 µF (tantalum) and 0.1 µF (ceramic). This node should not be used as a voltage source. |
| RXINP | 70 | I | RX channel stage 3 positive input. The input is self-biased at AVDD_RX/2. |
| RXINM | 71 | I | RX channel stage 3 negative input. The input is self-biased at AVDD_RX/2. |
| SCLK | 19 | O | Serial port shift clock (transmit and receive) |
| SDR | 20 | I | Serial data receive from DSP |
| SDX | 18 | O | Serial data transmit to DSP |
| TXBANDGAP | 14 | O | TX channel band-gap filter node. This terminal is provided for decoupling of the 1.5-V band-gap reference. The optimal capacitor value is 10 µF (tantalum) and 0.1 µF (ceramic). This node should not be used as a voltage source. |
| TXOUTP | 5 | O | TX channel positive output |
| TXOUTM | 6 | O | TX channel negative output |
| VCXOCNTL | 13 | O | DAC output to control onboard VCXO |
| VMID_RX | 50 | I/O | Decoupling Vmid for ADC. Add 10 µF (tantalum) and 0.1 µF (ceramic) capacitors to analog ground. |
| VSS | 80 | I | Substrate. Connect to analog ground. |

## detailed description

### transmit

The transmit channel is powered by a high performance DAC. The transmit channel update rate is 276 kHz. The DAC is a 14-bit DAC at 4.416-MHz. This provides 16X oversampling. A band-pass filter limits the output of the transmitter to a frequency range of 30 kHz to 138 kHz. A differential amplifier drives the output into the external line driver. The differential amplifier has programmable attenuation for added flexibility. The transmitter high-pass filter can be bypassed by writing the appropriate bit to the filter bypass control register (BCR).

The output spectrum of the DAC complies with the nonoverlapped power spectrum density (PSD) mask specified in the ITU draft recommendation G.992.2 for G.Lite.

The TXPAA is a programmable-attenuation amplifier. It provides 0 dB to 24 dB of attenuation in1-dB steps. The TXPAA is controlled via the PAA control register (PCR). For details about register programming see the register programming section.

## detailed description (continued)

### receive

The receive channel consists of a high-pass filter, a programmable gain amplifier, an ADC, and filters. In addition, it has an equalizer to attain maximum system performance. The input of the receiver is fully differential.

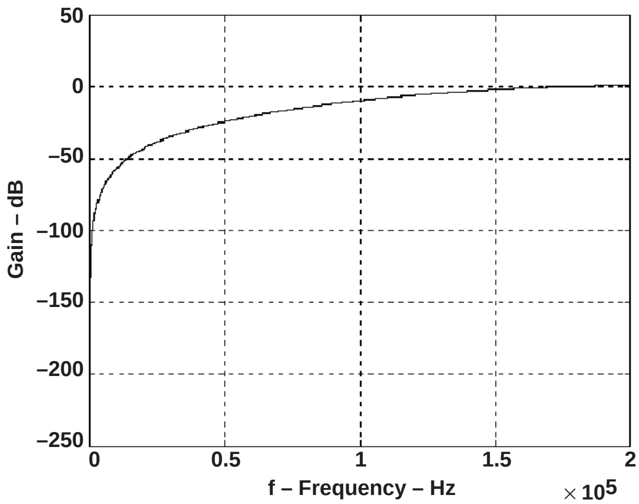
The ADC in the receive channel is a 14-bit converter which samples at 4.416 Msps for 4X oversampling. An on-chip decimator reduces the sampling frequency to 1.104 MHz. The low pass filtering of the receive channel limits the converted data to frequencies below 552 kHz.

The high-pass analog filter is used to reject the near-end echo to maximize the dynamic range of the ADC. The high-pass filter consists of two stages: (1) a second order high-pass filter (HPF1) and, (2) a third order elliptic high-pass filter (HPF2). Both stages have a cutoff at 180 kHz. The filter is divided into two stages to minimize the noise from a single stage being amplified throughout. Together, the two high-pass filters typically attenuate the echo power by 30 dB. There is a programmable gain amplifier (PGA) between the two filters for coarse gain adjustments of 0-dB –12-dB in 3-dB steps. After the high-pass filter stage, the receiver channel has a 0-dB –18-dB PGA that can be adjusted in 6-dB steps. HPF2 and PGAs are integrated in one block. Figure 1(a), 1(b), and 1(c) show the frequency response of HPF1 and HPF2 (with PGAs).

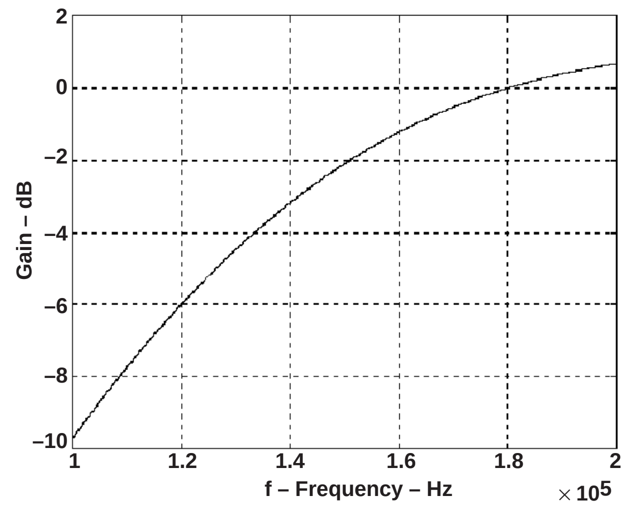
The PGA is followed by a 552-kHz low-pass filter with a programmable 25-dB/MHz slope (5-dB/MHz step) equalizer incorporated. After the equalizer, there is a fine-gain adjustment PGA of 0-dB to 9-dB in 0.25-dB steps.

All the RX PGAs are controlled via the PGA control registers (PCR–RX1 and PCR–RX2). See the register programming section for details about register programming.

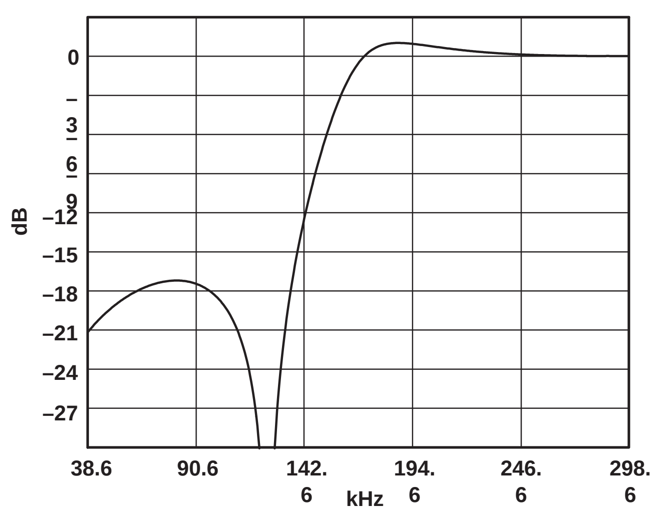
## detailed description (continued)




(a) RX-Stage HPF1 Frequency Response (0 to 200 kHz)




(b) RX-Stage HPF1 Frequency Response (100 kHz to 200 kHz)




(c) RX-Stage HPF2 Frequency Response (PGA1 = PGA2 = 0 dB)

**Figure 1. RX Stage HPF1 and HPF2 Frequency Response**

### clock control – VCXO mode

The VCXODAC uses a 12-bit, 2s complement number to control a 0-V to 3-V analog output. The two 8-bit registers, VCR-M and VCR-L, are used to generate the 12-bit control code (2s complement). This implies the use of 16 bits to obtain a 12-bit number.

VCR-M register occupy the most significant 8 bits in the 12-bit number and the lower 4 bits of the VCR-L register (VCR-L[3:0] ) are used for the low 4 bits of the 12-bit number. The 12-bit code is updated every time either register is updated. VCR-L[7:4] must always be zero.

### clock control – DPLL mode

As an alternative to the VCXODAC and VCXO, an off-chip crystal oscillator (XO) followed by an on-chip digital PLL are also implemented. Refer to Figure 7 for an internal function block diagram. The input clock (35.328 MHz) goes to a programmable frequency divider to generate sampling clock for the ADC and DAC converters. By changing the divide ratio, the phase of the sampling clock can be adjusted. Setting PLLSEL (pin 42) high will enable the DPLL mode. Refer to DPLL section for detail.

### clock generation

The clock generation block creates the necessary internal and external clocks needed by the device. All the clocks generated are produced from the CLKIN signal.

The following are recommended operational parameters for the external VCXO:

3.3-V supply, 35.328 MHz ±50 PPM center frequency, and input control voltage range of 0 V–3 V.
The recommended duty cycle is 50/50.

### clock generation – SCLK

SCLK is an output and is used for serial data transfer. It runs at 35.328 MHz. Although SCLK and MCLK run at the same speed, there is no fixed phase relationship between them.

### serial interface

The serial interface on the TLFD500PN connects directly to TI’s C54x or C6x families of DSPs. The interface operates at 35.328 MHz. The serial port consists of five signals: SCLK, FSX, FSR, SDX, and SDR. A typical connection diagram is shown in Figure 2.

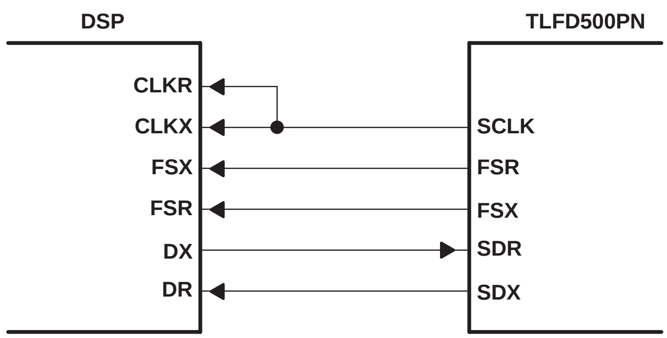



**Figure 2. Typical Serial Port Connection**

The serial port utilizes a primary/secondary scheme to transfer conversion data and control register data. A primary transfer scheme, used to transfer conversion data, occurs every conversion period. A secondary transfer scheme, used to transfer control data, happens only when requested by the host processor. The host processor requests a secondary transfer by using the LSB of the SDR data of the primary scheme. A value of 1 indicates a secondary transfer request. Once the secondary request is made and the primary transfer has been completed, secondary frame sync pulse (FSX/FSR) are transmitted to the host processor to indicate the beginning of the secondary transfer. The secondary FSX signal arrives 16 SCLKs after the primary FSX, and thus 48 SCLKs after the host processor request. This is because the span between FSX pulses for primary transfers is always 32 SCLKs. Each bit is read/written at the rising edge of the SCLK clock. Data bit mappings and example data transfers are shown in Table 1.

## detailed description (continued)

**Table 1. SDR LSB Control Function**

| CONTROL BIT D0 | CONTROL BIT FUNCTION |
|---|---|
| 0 | No secondary transfer requested |
| 1 | Secondary transfer requested |

### primary transfer data mapping

The data bit mapping of a primary transfer is shown in Figure 3. Bits D2–D15 of the SDR data stream are DAC data. D1 is the control bit for the DGPO pin. The value written to this bit is reflected on the DGPO pin. See the timing diagram in Figures 5 and 6 for detailed timing information. D0 is the secondary transfer request bit. When a 1 is written to this bit, the host is requesting a secondary data transfer.

In the SDX data stream, D2–D15 contain the ADC conversion data. D0 and D1 can be set to reflect the values of GPIO1 and GPIO2. To set D0 and D1 to reflect the GPIO values, the proper bit in the MCR register needs to be set.

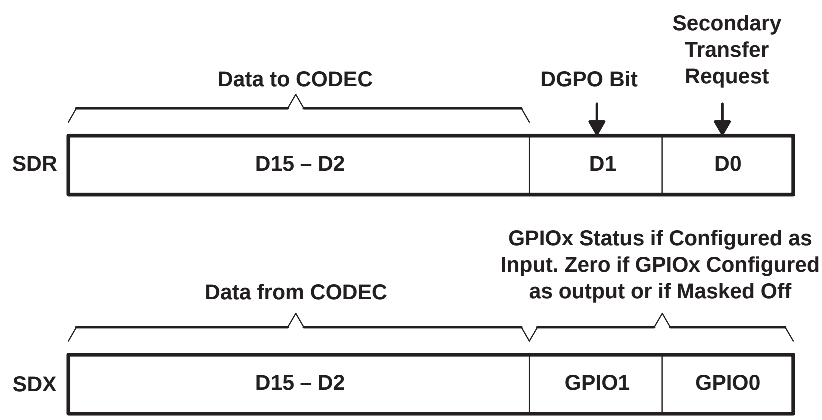



**Figure 3. Primary Transfer Data Bit Mapping**

### secondary transfer data mapping

Secondary serial communication is used to configure the device. The data bit mapping for a secondary transfer is shown in Figure 4. Bits D10–D14 of the SDR data from the host contain the address of the control register involved in the transfer. D15 is a R/$\overline{W}$ bit. To read out the control register by the host processor, bit R/$\overline{W}$ must be set to 1. To write to the control register by the host processor, bit R/$\overline{W}$ must be set to 0. During a read operation, bits D0–D7 are don't care. For a write operation, bits D0–D7 contain the data for the register addressed by D10–D14. The eight bits of SDX always reflect the status of GPI00–7.

If the secondary transfer is a read operation, the contents of the control register addressed by D10–D14 of the SDR data are reflected in bits D0–D7 of the SDX data stream. If the secondary transfer is a write operation, bits D0–D7 on SDX will be all zeroes.

### secondary transfer data mapping (continued)

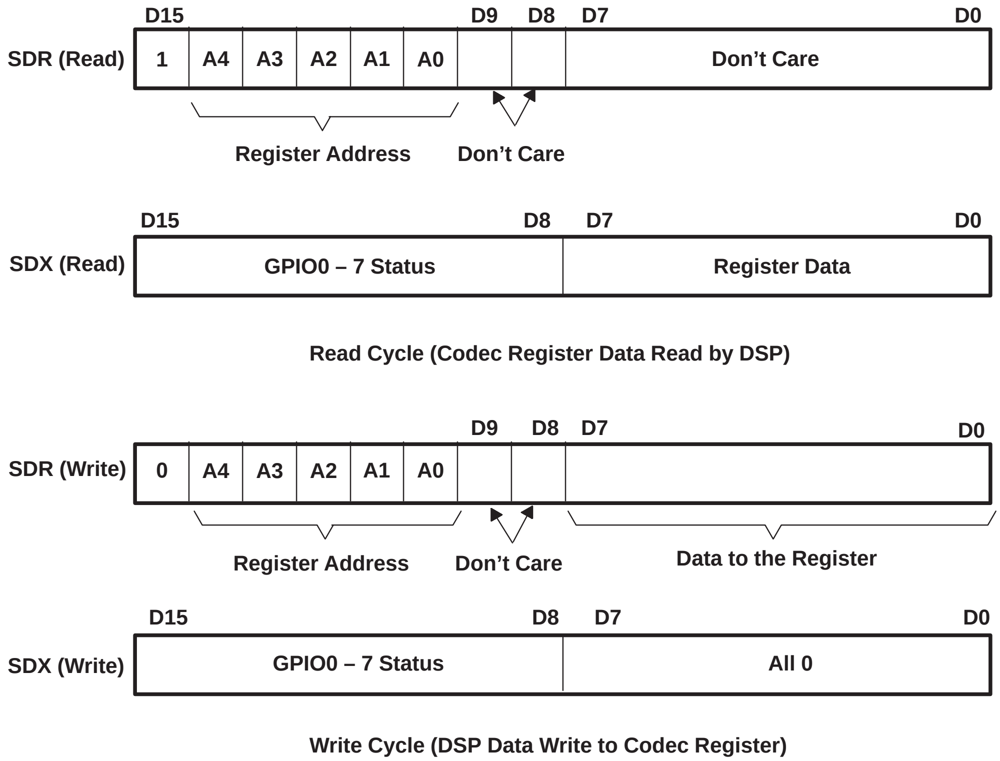



**Figure 4. Secondary Transfer Data Bit Mapping**

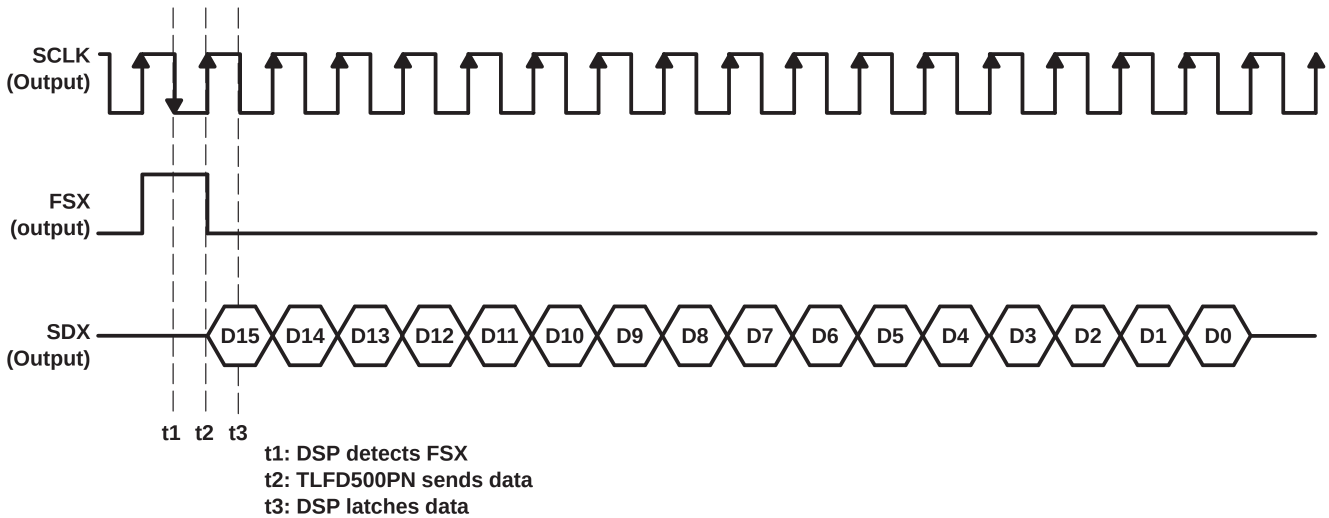
### example data transfers

Figures 5(a) and 5(b) show the timing relationship for SCLK, FSX, SDX, FSR, and SDR in a primary communication. The timing sequence for this operation is as follows:

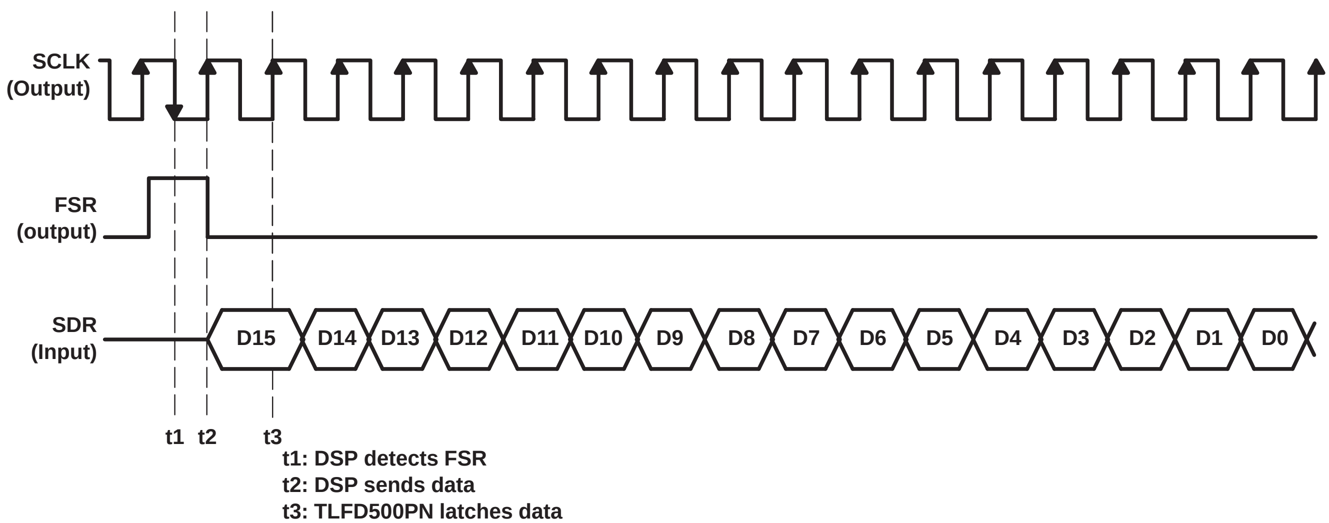
1. FS is set high and remains high during one SCLK period, then returns to low.
2. A 16-bit word is transmitted from the ADC (SDX), and a 16-bit word is received for DAC conversion (SDR).

Figure 6(a) and 6(b) shows the timing relationship with secondary request.

## detailed description (continued)




(a) TLFD500PN to DSP




(b) DSP to TLFD500PN

NOTE: TI DSP requires 10 ns after the positive edge of the SCLK to give the SDR data. This plus the board delay, output buffer (for SCLK) and input buffer delay (for SDR) to around 17 ns. As a consequence the SDR data can not be latched at the negative edge of SCLK.

**Figure 5. Data Transfers**

## detailed description (continued)

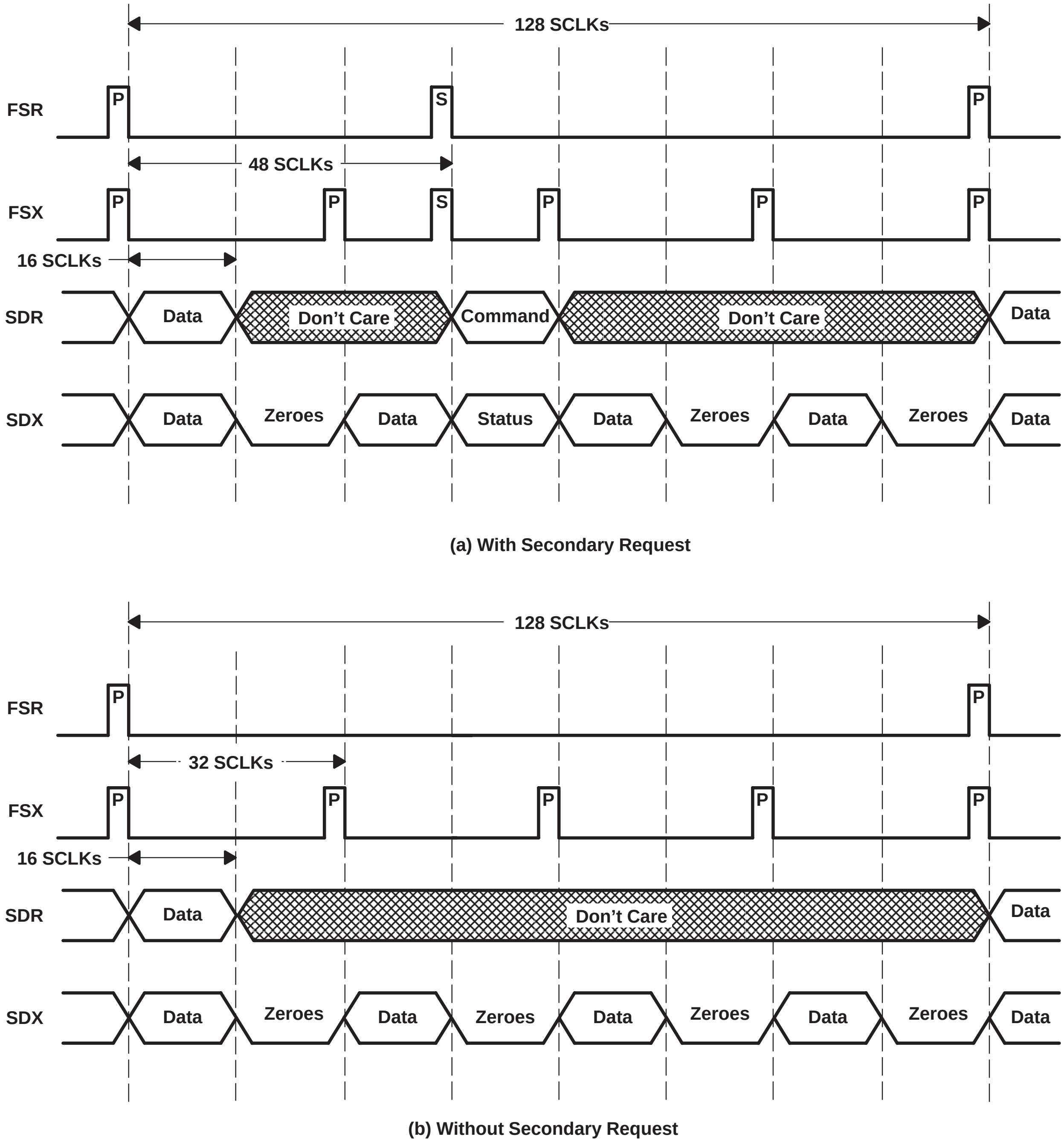



**Figure 6. Data Transfers**

## detailed description (continued)

### general purpose I/O port (GPIO)

The general-purpose I/O port provides eight input/output pins and one output-only pin for control of external circuitry, or for reading the status of external devices. The eight input/output pins are labeled GPIO0 –GPIO7. The output-only pin is labeled DGPO (direct general-purpose output). This pin is labeled as direct because a secondary transfer is not required to write to this pin.

The GPIO pins are controlled and read in the GPR-D register. The GPR-C register is used to configure the GPIO pins as input or output pins. The default reset condition is 11111111b, indicating that all are configured as inputs. For further details on register programming see the register programming section. The DGPO pin does not need configuring and is controlled by the D1 bit in the SDR data stream (that is, from the DSP to the TLFD500PN) during primary data transfers. In addition, a secondary transfer is not required to read GPIO0 and GPIO1 when they are configured as inputs. Their values can be mapped into the lower two bits of the SDX data stream (that is, from TLFD500PN to DSP) during primary data transfers. To map the values of GPIO0 and GPIO1 into the lower two bits of the SDX ADC data stream, set the appropriate bit in the MCR register.

For more flexibility, the values of GPIO0 – GPIO7 are mapped into the upper eight data bits of the SDX data stream on secondary data transfers. This allows the host processor to read the values of the GPIO pins and the contents of another control register during the same secondary data transfer. When a GPIO pin is being configured as an output, its corresponding status bit in the SDX data stream will be the last value written to the output pin.

Each output is capable of driving 2 mA.

### reference system

The integrated reference provides voltage and current to the internal analog blocks. It is also brought out to external pins for noise decoupling. They should not be used as dc voltage source.

When the internal reference is being used by the device, the device may be powered down by writing the appropriate reference control bit in the main control register (MCR) to achieve power savings during periods of device inactivity.

### auxiliary amplifiers

Four auxiliary high-performance operational amplifiers on the chip allow for additional onboard filtering and amplification with minimal component count. Each op-amp has differential inputs and outputs, with 2 input pins and 2 output pins. Each op-amp can be enabled by register programming.

The typical specifications for the operational amplifiers are as follows:

| | |
|---|---|
| DC Gain: | 126 dB |
| Bandwidth: | 116 MHz |
| PSRR: | 100 dB at dc, 70 dB at 1 MHz, and 40 dB at 4 MHz |
| Output common-mode: | AVDD_RX/2 (auxiliary amplifier 3,4) or AVDD_TX/2 (auxiliary amplifier 1,2) |
| Input interface: | AC coupled |

### device power-up sequence

All digital and analog supplies must be properly biased. All supply pins are mandatory. The power supply can not be switched, even when the codec has been powered down or parts of the codec are in power-down mode.

Reset must be held at least 20 µs after power up. To reset the reference circuit and registers requires 100 ms. When the chip is woken up from hardware power-down mode, it takes100 ms to reset the reference circuit before the chip works in normal mode. When the chip is woken up from software power-down mode, only 20 µs is needed before valid data comes out (reference must be kept on). Register values will not change in either wake-up operation.

## detailed description (continued)

### register programming

The codec registers are listed in Table 2, with each bit of each register defined. All registers are 8-bit wide.

**NOTE:**
Bits not defined in the table are reserved for future use. During a read, the reserved bit read value is not guaranteed. During a write, only zeroes can be written to reserved bits.

**Table 2. Codec Registers**

| REGISTER | | MODE | FUNCTION |
|---|---|---|---|
| NAME | ADDRESS A4 A3 A2 A1 A0 | | |
| BCR | 00001 | R/W | D0: Power-down RX HP filter 1<br>D1: Power-down RX HP filter 2<br>D2: Bypass TX digital HP filter<br>D3: Echo mode: Echo SDR data back to SDX<br>D4: Reserved<br>D5: Reserved<br>D6: Reserved |
| PCR-RX1 | 00010 | R/W | D[5:0] = RXPGA3[5:0]; Fine gain, 0 to 9 dB, 0.25-dB steps |
| PCR-RX2 | 00011 | R/W | D[2:0] = RXPGA1[2:0]; 0 to 12dB, 3-dB steps<br>D[4:3] = RXPGA2[1:0]; 0 to 18 dB, 6-dB steps |
| PCR-TX | 00100 | R/W | D[4:0] = TX PAA[4:0]; 0 to –24dB, –1-dB steps |
| EQR | 00101 | R/W | D[2:0] = EQ[2:0] 0 to 25 dB, 5 dB/MHz steps; D[6:4] = EQ_PGA[2:0] 0 to 6 dB, 1 dB steps |
| VCR-M | 00110 | R/W | D[7:0] = VCXO DAC control Bit[11:4]. |
| VCR-L | 00111 | R/W | D[3:0] = VCXO DAC control Bit[3:0]. D[7:4] must always be zero. |
| GPR-C | 01000 | R/W | D[7:0] = GPIO1 I/O control (0 = output, 1 = input) |
| GPR-D | 01001 | R/W | D[7:0] = GPIO data register |
| Reserved | 01010 | R/W | For future use. Read or write of register not allowed. |
| AUXR | 01011 | R/W | D0: Enable auxiliary amplifier 2<br>D1: Enable auxiliary amplifier 1<br>D2: Enable auxiliary amplifier 3<br>D3: Enable auxiliary amplifier 4 |
| NCO_DEF | 01100 | R/W | D[7:0] = Default NCO divide number |
| NCO_DIV_DELAY | 01101 | R/W | D[7:0] = Number of samples, from current secondary transfer, after which effect of delta will occur. |
| NCO_DELTA | 01110 | R/W | D[7:4] = Delta from default for first sample of data frame (–8 through 7)<br>D[3:0] = Number of times NCO divider remains changed from default before being set back to default (0 through 15) |
| MCR | 01111 | R/W | D0: S/W Power-down main reference<br>D1: S/W Power-down TX channel with reference still on<br>D2: S/W Power-down RX channel with reference still on<br>D3: S/W Power-down VCXO with reference still on<br>D4: S/W Reset<br>D5: Analog loop back (refer to block diagram)<br>D6: Digital loop back (refer to block diagram)<br>D7: Enable GPIO 1 and 2 to show in SDX primary data |

## BCR – bypass control register

**Address: 00001b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | ECHO | TXHPEN | RXHP2PD | RXHP1PD |

**Table 3. EQR Bit Definition**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REG. VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | R | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | R | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | – | R | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | – | – | 0 | – | – | – | – | ECHO | Do not echo SDR data on SDX |
| – | – | – | – | 1 | – | – | – | 0x08 | | Echo SDR data on SDX (see Note 1) |
| – | – | – | – | – | 0 | – | – | – | TXHPEN | Enable TX HP Filter |
| – | – | – | – | – | 1 | – | – | 0x04 | | Bypass TX HP Filter |
| – | – | – | – | – | – | 0 | – | – | RXHP2PD | Power up RX HP Filter 2 |
| – | – | – | – | – | – | 1 | – | 0x02 | | Power down RX HP Filter 2 |
| – | – | – | – | – | – | – | 0 | – | RXHP1PD | Power up RX HP Filter 1 |
| – | – | – | – | – | – | – | 1 | 0x01 | | Power down RX HP Filter 1 |

NOTE 1: ECHO mode allows for a quick verification of the serial interface operation. It sends back the data from input data buffer to the output data buffer and does not exercise the RX or TX channel.

## PCR-RX1 – programmable gain control register 1 for RX channel PGA3

**Address: 00010b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | RXPGA3[5] | RXPGA3[4] | RXPGA3[3] | RXPGA3[2] | RXPGA3[1] | RXPGA3[0] |

### Table 4. PCR-RX1 Gain

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | R | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 | RXPGA3[5:0] | 0dB |
| – | | 0 | 0 | 0 | 0 | 0 | 1 | 0x01 | | 0.25dB |
| – | – | 0 | 0 | 0 | 0 | 1 | 0 | 0x02 | | 0.50dB |
| – | – | 0 | 0 | 0 | 0 | 1 | 1 | 0x03 | | 0.75dB |
| – | – | 0 | 0 | 0 | 1 | 0 | 0 | 0x04 | | 1.00dB |
| – | – | 0 | 0 | 0 | 1 | 0 | 1 | 0x05 | | 1.25dB |
| – | – | 0 | 0 | 0 | 1 | 1 | 0 | 0x06 | | 1.50dB |
| – | – | 0 | 0 | 0 | 1 | 1 | 1 | 0x07 | | 1.75dB |
| – | – | 0 | 0 | 1 | 0 | 0 | 0 | 0x08 | | 2.00dB |
| – | – | 0 | 0 | 1 | 0 | 0 | 1 | 0x09 | | 2.25dB |
| – | – | 0 | 0 | 1 | 0 | 1 | 0 | 0x0A | | 2.50dB |
| – | – | 0 | 0 | 1 | 0 | 1 | 1 | 0x0B | | 2.75dB |
| – | – | 0 | 0 | 1 | 1 | 0 | 0 | 0x0C | | 3.00dB |
| – | – | 0 | 0 | 1 | 1 | 0 | 1 | 0x0D | | 3.25dB |
| – | – | 0 | 0 | 1 | 1 | 1 | 0 | 0x0E | | 3.50dB |
| – | – | 0 | 0 | 1 | 1 | 1 | 1 | 0x0F | | 3.75dB |
| – | – | 0 | 1 | 0 | 0 | 0 | 0 | 0x10 | | 4.00dB |
| – | – | 0 | 1 | 0 | 0 | 0 | 1 | 0x11 | | 4.25dB |
| – | – | 0 | 1 | 0 | 0 | 1 | 0 | 0x12 | | 4.50dB |
| – | – | 0 | 1 | 0 | 0 | 1 | 1 | 0x13 | | 4.75dB |
| – | – | 0 | 1 | 0 | 1 | 0 | 0 | 0x14 | | 5.00dB |
| – | – | 0 | 1 | 0 | 1 | 0 | 1 | 0x15 | | 5.25dB |
| – | – | 0 | 1 | 0 | 1 | 1 | 0 | 0x16 | | 5.50dB |
| – | – | 0 | 1 | 0 | 1 | 1 | 1 | 0x17 | | 5.75dB |
| – | – | 0 | 1 | 1 | 0 | 0 | 0 | 0x18 | | 6.00dB |
| – | – | 0 | 1 | 1 | 0 | 0 | 1 | 0x19 | | 6.25dB |
| – | – | 0 | 1 | 1 | 0 | 1 | 0 | 0x1A | | 6.50dB |
| – | – | 0 | 1 | 1 | 0 | 1 | 1 | 0x1B | | 6.75dB |
| – | – | 0 | 1 | 1 | 1 | 0 | 0 | 0x1C | | 7.00dB |
| – | – | 0 | 1 | 1 | 1 | 0 | 1 | 0x1D | | 7.25dB |
| – | – | 0 | 1 | 1 | 1 | 1 | 0 | 0x1E | | 7.50dB |
| – | – | 0 | 1 | 1 | 1 | 1 | 1 | 0x1F | | 7.75dB |
| – | – | 1 | 0 | 0 | 0 | 0 | 0 | 0x20 | | 8.00dB |
| – | – | 1 | 0 | 0 | 0 | 1 | 1 | 0x21 | | 8.25dB |
| – | – | 1 | 0 | 0 | 1 | 0 | 0 | 0x22 | | 8.50dB |

**Table 4. PCR-RX1 Gain (Continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| – | – | 1 | 0 | 0 | 0 | 1 | 1 | 0x23 | RXPGA3[5:0] | 8.75dB |
| – | – | 1 | 0 | 0 | 1 | 0 | 0 | 0x24 | | 9.00dB |
| – | – | 1 | 0 | 0 | 1 | 0 | 1 | 0x25 | | INVALID |
| – | – | 1 | 0 | 0 | 1 | 1 | 0 | 0x26 | | INVALID |
| – | – | 1 | 0 | 0 | 1 | 1 | 1 | 0x27 | | INVALID |
| – | – | 1 | 0 | 1 | 0 | 0 | 0 | 0x28 | | INVALID |
| – | – | 1 | 0 | 1 | 0 | 0 | 1 | 0x29 | | INVALID |
| – | – | 1 | 0 | 1 | 0 | 1 | 0 | 0x2A | | INVALID |
| – | – | 1 | 0 | 1 | 0 | 1 | 1 | 0x2B | | INVALID |
| – | – | 1 | 0 | 1 | 1 | 0 | 0 | 0x2C | | INVALID |
| – | – | 1 | 0 | 1 | 1 | 0 | 1 | 0x2D | | INVALID |
| – | – | 1 | 0 | 1 | 1 | 1 | 0 | 0x2E | | INVALID |
| – | – | 1 | 0 | 1 | 1 | 1 | 1 | 0x2F | | INVALID |
| – | – | 1 | 1 | 0 | 0 | 0 | 0 | 0x30 | | INVALID |
| – | – | 1 | 1 | 0 | 0 | 0 | 1 | 0x31 | | INVALID |
| – | – | 1 | 1 | 0 | 0 | 1 | 0 | 0x32 | | INVALID |
| – | – | 1 | 1 | 0 | 0 | 1 | 1 | 0x33 | | INVALID |
| – | – | 1 | 1 | 0 | 1 | 0 | 0 | 0x34 | | INVALID |
| – | – | 1 | 1 | 0 | 1 | 0 | 1 | 0x35 | | INVALID |
| – | – | 1 | 1 | 0 | 1 | 1 | 0 | 0x36 | | INVALID |
| – | – | 1 | 1 | 0 | 1 | 1 | 1 | 0x37 | | INVALID |
| – | – | 1 | 1 | 1 | 0 | 0 | 0 | 0x38 | | INVALID |
| – | – | 1 | 1 | 1 | 0 | 0 | 1 | 0x39 | | INVALID |
| – | – | 1 | 1 | 1 | 0 | 1 | 0 | 0x3A | | INVALID |
| – | – | 1 | 1 | 1 | 0 | 1 | 1 | 0x3B | | INVALID |
| – | – | 1 | 1 | 1 | 1 | 0 | 0 | 0x3C | | INVALID |
| – | – | 1 | 1 | 1 | 1 | 0 | 1 | 0x3D | | INVALID |
| – | – | 1 | 1 | 1 | 1 | 1 | 0 | 0x3E | | INVALID |
| – | – | 1 | 1 | 1 | 1 | 1 | 1 | 0x3F | | INVALID |

NOTE 2: The formula to convert bit value to RXPGA3 gain in dB is
RXPGA3 gain (in dB) = RXPGA3[5:0] (in decimal) x 0.25dB
Similarly one can compute the RXPGA3 [5:0] bit combination needed, given the gain in dB.

**CAUTION:**
**Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.**

## PCR-RX2 – programmable gain control register 2 for RX channel PGA1 and PGA2

**Address: 00011b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | RXPGA2[1] | RXPGA2[0] | RXPGA1[2] | RXPGA1[1] | RXPGA1[0] |

### Table 5. PCR-RX2 Gain

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | R | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | R | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | – | 0 | 0 | – | – | – | 0x00 | RXPGA2[1:0] | 0dB |
| – | – | – | 0 | 1 | – | – | – | 0x08 | | 6dB |
| – | – | – | 1 | 0 | – | – | – | 0x10 | | 12dB |
| – | – | – | 1 | 1 | – | – | – | 0x18 | | 18dB |
| – | – | – | – | – | 0 | 0 | 0 | 0x00 | RXPGA1[2:0] | 0dB |
| – | – | – | – | – | 0 | 0 | 1 | 0x01 | | 3dB |
| – | – | – | – | – | 0 | 1 | 0 | 0x02 | | 6dB |
| – | – | – | – | – | 0 | 1 | 1 | 0x03 | | 9dB |
| – | – | – | – | – | 1 | 0 | 0 | 0x04 | | 12dB |
| – | – | – | – | – | 1 | 0 | 1 | 0x05 | | INVALID |
| – | – | – | – | – | 1 | 1 | 0 | 0x06 | | INVALID |
| – | – | – | – | – | 1 | 1 | 1 | 0x07 | | INVALID |

NOTES: 3. The formula to convert bit value to RXPGA2 gain in dB is
RXPGA2 gain (in dB) = RXPGA2[1:0] (in decimal) x 6dB
Similarly the needed RXPGA2[1:0] bit combination can be computed, given the gain in dB.
4. The formula to convert bit value to RXPGA1 gain in dB is
RXPGA1 gain (in dB) = RXPGA1[2:0] (in decimal) x 3dB
Similarly the needed RXPGA1[2:0] bit combination can be computed, given the gain in dB.

**CAUTION:**
**Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.**

## PCR-TX – programmable attenuation control register for TX channel

**Address: 00100b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | TXPAA[4] | TXPAA[3] | TXPAA[2] | TXPAA[1] | TXPAA[0] |

## PCR-TX – programmable attenuation control register for TX channel (continued)

### Table 6. PCR-TX Attenuation

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | R | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | R | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | – | 0 | 0 | 0 | 0 | 0 | 0x00 | TXPAA[4:0] | –0 dB |
| – | – | – | 0 | 0 | 0 | 0 | 1 | 0x01 | | –1 dB |
| – | – | – | 0 | 0 | 0 | 1 | 0 | 0x02 | | –2 dB |
| – | – | – | 0 | 0 | 0 | 1 | 1 | 0x03 | | –3 dB |
| – | – | – | 0 | 0 | 1 | 0 | 0 | 0x04 | | –4 dB |
| – | – | – | 0 | 0 | 1 | 0 | 1 | 0x05 | | –5 dB |
| – | – | – | 0 | 0 | 1 | 1 | 0 | 0x06 | | –6 dB |
| – | – | – | 0 | 0 | 1 | 1 | 1 | 0x07 | | –7 dB |
| – | – | – | 0 | 1 | 0 | 0 | 0 | 0x08 | | –8 dB |
| – | – | – | 0 | 1 | 0 | 0 | 1 | 0x09 | | –9 dB |
| – | – | – | 0 | 1 | 0 | 1 | 0 | 0x0A | | –10 dB |
| – | – | – | 0 | 1 | 0 | 1 | 1 | 0x0B | | –11 dB |
| – | – | – | 0 | 1 | 1 | 0 | 0 | 0x0C | | –12 dB |
| – | – | – | 0 | 1 | 1 | 0 | 1 | 0x0D | | –13 dB |
| – | – | – | 0 | 1 | 1 | 1 | 0 | 0x0E | | –14 dB |
| – | – | – | 0 | 1 | 1 | 1 | 1 | 0x0F | | –15 dB |
| – | – | – | 1 | 0 | 0 | 0 | 0 | 0x10 | | –16 dB |
| – | – | – | 1 | 0 | 0 | 0 | 1 | 0x11 | | –17 dB |
| – | – | – | 1 | 0 | 0 | 1 | 0 | 0x12 | | –18 dB |
| – | – | – | 1 | 0 | 0 | 1 | 1 | 0x13 | | –19 dB |
| – | – | – | 1 | 0 | 1 | 0 | 0 | 0x14 | | –20 dB |
| – | – | – | 1 | 0 | 1 | 0 | 1 | 0x15 | | –21 dB |
| – | – | – | 1 | 0 | 1 | 1 | 0 | 0x16 | | –22 dB |
| – | – | – | 1 | 0 | 1 | 1 | 1 | 0x17 | | –23 dB |
| – | – | – | 1 | 1 | 0 | 0 | 0 | 0x18 | | –24 dB |
| – | – | – | 1 | 1 | 0 | 0 | 1 | 0x19 | | INVALID |
| – | – | – | 1 | 1 | 0 | 1 | 0 | 0x1A | | INVALID |
| – | – | – | 1 | 1 | 0 | 1 | 1 | 0x1B | | INVALID |
| – | – | – | 1 | 1 | 1 | 0 | 0 | 0x1C | | INVALID |
| – | – | – | 1 | 1 | 1 | 0 | 1 | 0x1D | | INVALID |
| – | – | – | 1 | 1 | 1 | 1 | 0 | 0x1E | | INVALID |
| – | – | – | 1 | 1 | 1 | 1 | 1 | 0x1F | | INVALID |

NOTE 5: The formula to convert bit value to TXPAA attenuation in dB is

TXPAA attenuation (in dB) = TXPAA[4:0] (in decimal) x (–1)dB

Similarly one can compute the TXPAA[4:0] bit combination needed, given the attenuation in dB.

**CAUTION:**

**Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.**

## EQR – equalizer slope and gain control register

**Address: 00101b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | EQPGA[2] | EQPGA[1] | EQPGA[0] | Reserved | EQ[2] | EQ[1] | EQ[0] |

**Table 7. EQR Slope and Gain**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | 0 | 0 | 0 | – | – | – | – | 0x00 | EQPGA[2:0] | 0dB |
| – | 0 | 0 | 1 | – | – | – | – | 0x10 | | 1dB |
| – | 0 | 1 | 0 | – | – | – | – | 0x20 | | 2dB |
| – | 0 | 1 | 1 | – | – | – | – | 0x30 | | 3dB |
| – | 1 | 0 | 0 | – | – | – | – | 0x40 | | 4dB |
| – | 1 | 0 | 1 | – | – | – | – | 0x50 | | 5dB |
| – | 1 | 1 | 0 | – | – | – | – | 0x60 | | 6dB |
| – | 1 | 1 | 1 | – | – | – | – | 0x70 | | INVALID |
| – | – | – | – | R | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | – | – | – | 0 | 0 | 0 | 0x00 | EQ[2:0] | 0dB slope |
| – | – | – | – | – | 0 | 0 | 1 | 0x01 | | 5dB slope |
| – | – | – | – | – | 0 | 1 | 0 | 0x02 | | 10dB slope |
| – | – | – | – | – | 0 | 1 | 1 | 0x03 | | 15dB slope |
| – | – | – | – | – | 1 | 0 | 0 | 0x04 | | 20dB slope |
| – | – | – | – | – | 1 | 0 | 1 | 0x05 | | 25dB slope |
| – | – | – | – | – | 1 | 1 | 0 | 0x06 | | INVALID |
| – | – | – | – | – | 1 | 1 | 1 | 0x07 | | INVALID |

NOTES: 6. The formula to convert bit value to EQPGA gain in dB is
EQPGA gain (in dB) = EQPGA[2:0] (in decimal) x 1 dB
Similarly one can compute the EQPGA[2:0] bit combination needed, given the gain in dB.
7. The formula to convert bit value to EQ slope in dB is
EQ slope (in dB/MHz) =EQ[2:0] (in decimal) x 5 dB/MHz
Similarly one can compute the EQ[2:0] bit combination needed, given the slope in dB/MHz.

**CAUTION:**
**Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.**

## VCR-M – VCXO DAC control register MSB

**Address: 00110b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| VCR–M[7] | VCR–M[6] | VCR–M[5] | VCR–M[4] | VCR–M[3] | VCR–M[2] | VCR–M[1] | VCR–M[0] |

## VCR-L – VCXO DAC control register LSB

**Address: 00111b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | VCR–L[3] | VCR–L[2] | VCR–L[1] | VCR–L[0] |

Table 8 shows some representative analog outputs.

**Table 8. Representative Analog Outputs**

| OPERATION | HEX RESULT | ANALOG OUTPUT | COMMENTS |
|---|---|---|---|
| VCR–M[7:0] * $2^4$ + VCR–L[3:0] | 0x800 | 0 V | Min scale |
| | 0x801 | ∆V | Just above min |
| | … | … | … |
| | 0xFFF | 2047∆V | Just below mid |
| | 0x000 | 2048∆V | Mid scale |
| | 0x001 | 2049∆V | Just above mid |
| | … | … | … |
| | 0x7FE | 4094∆V | Just below max |
| | 0x7FF | 4095∆V | Max scale |

Where step–size, ∆ = (3/4095) V.

For example, if 0xAA7 is desired, VCR-M and VCR-L should be set to 0xAA and 0x07;
if 0x539 is desired, VCR-M and VCR-L should be set to 0x53 and 0x09.

## GPR-C – GPIO I/O direction control register

**Address: 01000b** **Contents at reset: 11111111b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| GPIOC[7] | GPIOC[6] | GPIOC[5] | GPIOC[4] | GPIOC[3] | GPIOC[2] | GPIOC[1] | GPIOC[0] |

### Table 9. GPR-C Direction Control

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REG VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | – | – | – | – | – | – | – | – | GPIOC[7] | Configure GPIO 7 pin as output |
| 1 | – | – | – | – | – | – | – | 0x80 | | Configure GPIO 7 pin as input |
| – | 0 | – | – | – | – | – | – | – | GPIOC[6] | Configure GPIO 6 pin as output |
| – | 1 | – | – | – | – | – | – | 0x40 | | Configure GPIO 6 pin as input |
| – | – | 0 | – | – | – | – | – | – | GPIOC[5] | Configure GPIO 5 pin as output |
| – | – | 1 | – | – | – | – | – | 0x20 | | Configure GPIO 5 pin as input |
| – | – | – | 0 | – | – | – | – | – | GPIOC[4] | Configure GPIO 4 pin as output |
| – | – | – | 1 | – | – | – | – | 0x10 | | Configure GPIO 4 pin as input |
| – | – | – | – | 0 | – | – | – | – | GPIOC[3] | Configure GPIO 3 pin as output |
| – | – | – | – | 1 | – | – | – | 0x08 | | Configure GPIO 3 pin as input |
| – | – | – | – | – | 0 | – | – | – | GPIOC[2] | Configure GPIO 2 pin as output |
| – | – | – | – | – | 1 | – | – | 0x04 | | Configure GPIO 2 pin as input |
| – | – | – | – | – | – | 0 | – | – | GPIOC[1] | Configure GPIO 1 pin as output |
| – | – | – | – | – | – | 1 | – | 0x02 | | Configure GPIO 1 pin as input |
| – | – | – | – | – | – | – | 0 | – | GPIOC[0] | Configure GPIO 0 pin as output |
| – | – | – | – | – | – | – | 1 | 0x01 | | Configure GPIO 0 pin as input |

NOTE 8: A particular GPIOC control bit configures direction for the corresponding GPIOD data bit.

## GPR-D – GPIO data register

**Address: 01001b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| GPIOD[7] | GPIOD[6] | GPIOD[5] | GPIOD[4] | GPIOD[3] | GPIOD[2] | GPIOD[1] | GPIOD[0] |

**CAUTION:**
**GPIOD[7:0] corresponds to pins GPIO7–GPIO0 respectively.**

## AUXR – auxiliary amplifier enable register

**Address: 01011b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Reserved | AMP4EN | AMP3EN | AMP1EN | AMP2EN |

**Table 10. Auxiliary Amplifier-Control**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REG VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | R | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | R | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | – | R | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | – | – | – | 0 | – | – | – | – | AMP4EN | Disable amplifier 4 |
| – | – | – | – | 1 | – | – | – | 0x08 | | Enable amplifier 4 |
| – | – | – | – | – | 0 | – | – | – | AMP3EN | Disable amplifier 3 |
| – | – | – | – | – | 1 | – | – | 0x04 | | Enable amplifier 3 |
| – | – | – | – | – | – | 0 | – | – | AMP1EN | Disable amplifier 1 |
| – | – | – | – | – | – | 1 | – | 0x02 | | Enable amplifier 1 |
| – | – | – | – | – | – | – | 0 | – | AMP2EN | Disable amplifier 2 |
| – | – | – | – | – | – | – | 1 | 0x01 | | Enable amplifier 2 |

**CAUTION:**
**Performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The default condition is with the amplifiers switched off.**

## NCO_DEF – numerically controlled oscillator default value register

**Address: 01100b** **Contents at reset: 01000000b (64 decimal)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Reserved | NCDEF[6] | NCDEF[5] | NCDEF[4] | NCDEF[3] | NCDEF[2] | NCDEF[1] | NCDEF[0] |

**Table 11. NCO Default Value Table**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| R | – | – | – | – | – | – | – | – | Reserved | Bit reserved for future use |
| – | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0×00 | NCDEF[7:0] | Decimal 0, INVALID |
| – | … | … | … | … | … | … | … | 0×01 – 0×2E | | Decimal 1 to 46, INVALID |
| – | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0×2F | | Decimal 47, INVALID |
| – | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0×30 | | Decimal 48, INVALID |
| – | … | … | … | … | … | … | … | 0×31 – 0×5C | | Decimal 49 to 92, VALID |
| – | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0×5D | | Decimal 93, INVALID |
| – | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0×5E | | Decimal 94, INVALID |
| – | … | … | … | … | … | … | … | 0×5F – 0×FF | | Decimal 95 onwards, INVALID |

**CAUTION:**
**The sum NCDEF[7:0] + NCDEL[3:0] should always be between 48 and 93. Out-of-bound values should not be used.**

## NCO_DIV_DELAY – numerically controlled oscillator delay control register

**Address: 01101b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| NCDLY[7] | NCDLY[6] | NCDLY[5] | NCDLY[4] | NCDLY[3] | NCDLY[2] | NCDLY[1] | NCDLY[0] |

**Table 12. NCO Default Value**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0×00 | NCDLY[7:0] | INVALID |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0×01 | | INVALID |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0×02 | | ADCLK jittered 2 sample clocks (of ADCLK) after write into the NCO_DIV_DELAY register (see Note 10) |
| … | … | … | … | … | … | … | … | 0×03 – 0×FD | | Jitter after 3 to 253 sample clocks (All individual values are valid) |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0×FE | | Jitter after 254 sample clocks |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0×FF | | Jitter after 255 sample clocks |

NOTES: 9. The formula to convert NCDLY[7:0] to delay is straightforward.
Delay (number of ADCLK periods) = NDCLK[7:0] (except for 0 and 1).
10. ADCLK–A/D converter sampling clock

**CAUTION:**
**This register is also the only means of communicating to the codec that the ADCLK must be jittered. Thus not writing a value implies that jitter will not take place even if other registers have non-default values. As a side consequence, this register does not remember its value. All the others store them unless RESET.**

**Writing 0 or 1 is not recommended**

### examples:

1. NCDEF[7:0] = 64 (dec.), NCDEL[4:0] = 1, NCRPT[2:0] = 2, NCDLY[7:0] = 5. This shows a default division value of 64, giving a normal ADCLK of 2.208 MHz (assuming 35.328 MHz input); the division ratio will be 64 + 1 = 65 to effect the jitter, that is, pulling in the clock phase. The jitter will be repeated for 2 consecutive samples. The jitter will take effect 5 ADCLK sample periods after writing to NCDLY.
2. NCDEF[7:0] = 63 (decimal), NCDEL[4:0] = –1, NCRPT[2:0] = 2, NCDLY[7:0] = 5. Similar to 1. The default frequency is slightly less than 2.208 MHz. Since the division ratio is 63 – 1 = 62, the clock phase is pushed out.
3. NCDEF[7:0] = 64 (decimal), NCDEL[4:0] = 0, NCRPT[2:0] = 2, NCDLY[7:0] = 5. Here the jitter will not be observed, since the delta register is zero.
4. NCDEF[7:0] = 64 (decimal), NCDEL[4:0] = 1, NCRPT[2:0] = 0, NCDLY[7:0] = 5. Here the jitter will not be observed, since the repeat register is zero.
5. NCDEF[7:0] = 64 (decimal), NCDEL[4:0] = 1, NCRPT[2:0] = 2, NCDLY[7:0] = 0. This is invalid and not recommended. NCDLY[7:0] can not be 0 or 1.
6. NCDEF[7:0] = 64 (decimal), NCDEL[4:0] = 1, NCRPT[2:0] = 2. Here the jitter will not occur since there was not writing to NCDLY. The other registers will retain their values as in all other cases.

## NCO_DELTA – numerically controlled oscillator delta value register

**Address: 01110b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| NCDEL[3] | NCDEL[2] | NCDEL[1] | NCDEL[0] | NCRPT[3] | NCRPT[2] | NCRPT[1] | NCRPT[0] |

**Table 13. NCO_DELTA – DELTA and REPEAT**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | – | – | – | – | 0×00 | NCDEL[3:0] | DELTA = 0 |
| 0 | 0 | 0 | 1 | – | – | – | – | 0×08 | | DELTA = 1 |
| 0 | 0 | 1 | 0 | – | – | – | – | 0×10 | | DELTA = 2 |
| 0 | 0 | 1 | 1 | – | – | – | – | 0×18 | | DELTA = 3 |
| 0 | 1 | 0 | 0 | – | – | – | – | 0×20 | | DELTA = 4 |
| 0 | 1 | 0 | 1 | – | – | – | – | 0×28 | | DELTA = 5 |
| 0 | 1 | 1 | 0 | – | – | – | – | 0×30 | | DELTA = 6 |
| 0 | 1 | 1 | 1 | – | – | – | – | 0×38 | | DELTA = 7 |
| 1 | 0 | 0 | 0 | – | – | – | – | 0×40 | | DELTA = –8 |
| 1 | 0 | 0 | 1 | – | – | – | – | 0×48 | | DELTA = –7 |
| 1 | 0 | 1 | 0 | – | – | – | – | 0×50 | | DELTA = –6 |
| 1 | 0 | 1 | 1 | – | – | – | – | 0×58 | | DELTA = –5 |
| 1 | 1 | 0 | 0 | – | – | – | – | 0×60 | | DELTA = –4 |
| 1 | 1 | 0 | 1 | – | – | – | – | 0×68 | | DELTA = –3 |
| 1 | 1 | 1 | 0 | – | – | – | – | 0×70 | | DELTA = –2 |
| 1 | 1 | 1 | 1 | – | – | – | – | 0×78 | | DELTA = –1 |
| – | – | – | – | 0 | 0 | 0 | 0 | 0×00 | NCRPT[3:0] | REPEAT = 0 (same as DELTA = 0) |
| – | – | – | – | 0 | 0 | 0 | 1 | 0×01 | | REPEAT =1 |
| – | – | – | – | 0 | 0 | 1 | 0 | 0×02 | | REPEAT =2 |
| – | – | – | – | 0 | 0 | 1 | 1 | 0×03 | | REPEAT =3 |
| – | – | – | – | 0 | 1 | 0 | 0 | 0×04 | | REPEAT =4 |
| – | – | – | – | 0 | 1 | 0 | 1 | 0×05 | | REPEAT =5 |
| – | – | – | – | 0 | 1 | 1 | 0 | 0×06 | | REPEAT =6 |
| – | – | – | – | 0 | 1 | 1 | 1 | 0×07 | | REPEAT =7 |
| – | – | – | – | 1 | 0 | 0 | 0 | 0×08 | | REPEAT =8 |
| – | – | – | – | 1 | 0 | 0 | 1 | 0×09 | | REPEAT =9 |
| – | – | – | – | 1 | 0 | 1 | 0 | 0×0A | | REPEAT =10 |
| – | – | – | – | 1 | 0 | 1 | 1 | 0×0B | | REPEAT =11 |
| – | – | – | – | 1 | 1 | 0 | 0 | 0×0C | | REPEAT =12 |
| – | – | – | – | 1 | 1 | 0 | 1 | 0×0D | | REPEAT =13 |
| – | – | – | – | 1 | 1 | 1 | 0 | 0×0E | | REPEAT =14 |
| – | – | – | – | 1 | 1 | 1 | 1 | 0×0F | | REPEAT =15 |

## MCR – master control register

**Address: 01111b** **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| GP12EN | DLBEN | ALBEN | SWRST | VCDACPD | RXPD | TXPD | SWREFPD |

**Table 14. MCR Control**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REG VALUE | BIT NAME | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | – | – | – | – | – | – | – | – | GP12EN | No effect on SDX |
| 1 | – | – | – | – | – | – | – | 0x80 | | Show GPIO 1 and 2 in SDX primary. |
| – | 0 | – | – | – | – | – | – | – | DLBEN | No effect on digital loop back |
| – | 1 | – | – | – | – | – | – | 0x40 | | Enable digital loop back |
| – | – | 0 | – | – | – | – | – | – | ALBEN | No effect on analog loop back |
| – | – | 1 | – | – | – | – | – | 0x20 | | Enable analog loop back |
| – | – | – | 0 | – | – | – | – | – | SWRST | No effect on reset |
| – | – | – | 1 | – | – | – | – | 0x10 | | Perform soft reset |
| – | – | – | – | 0 | – | – | – | – | VCDACPD | Power up VCXODAC |
| – | – | – | – | 1 | – | – | – | 0x08 | | Power down VCXODAC |
| – | – | – | – | – | 0 | – | – | – | RXPD | Power up RX channel |
| – | – | – | – | – | 1 | – | – | 0x04 | | Power down RX channel |
| – | – | – | – | – | – | 0 | – | – | TXPD | Power up TX channel |
| – | – | – | – | – | – | 1 | – | 0x02 | | Power down TX channel |
| – | – | – | – | – | – | – | 0 | – | SWREFPD | Power up (soft) main reference |
| – | – | – | – | – | – | – | 1 | 0x01 | | Power down (soft) main reference |

NOTES: 11. The SWRST and SWREFPD refer to the word software, since the reset is done by register programming as opposed to hard resets done by forcing pin logic levels.
12. Analog loop-back means looping back of the analog TX output to the RX input. This way the codec can be tested without need of external analog sources.
13. Digital loop-back means looping back the digital RX output to the TX input. Here we can test the code without the need for a DSP and serial data transfer.

**CAUTION:**
**All power downs of VCXODAC, RX, and TX channels occur with the reference still on.**

## DPLL detailed description

The default value of register NCO_DEF is 64. With the 35.328 MHz input clock, the output frequency of the PLL is $4 \times 35.328 = 141.312$ MHz. To obtain an ADC clock of 2.208 MHz the divide ratio (controlled by register NCO_DEF) needs to be 64. Increasing or decreasing this ratio (for example, 65 or 63) can effect a temporary phase shift. The ratio is controlled by the DSP through register programming.

In DPLL mode, the ADC clock (ADCLK) will work at 2.208 MHz instead of the 4.416 MHz used in the VCXO mode. The DAC clock (DACLK) will continue to work at 4.416 MHz. When the ADCLK is jittered, the DACLK is also jittered.

## DPLL detailed description (continued)

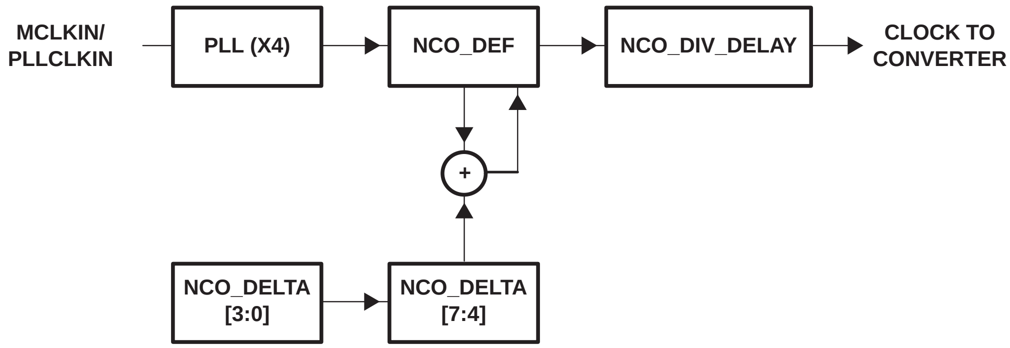



**Figure 7. DPLL Internal Function Block Diagram**

Example: Assume MCLKIN/PLLCLKIN=35.328 MHz. When NCO_DEF is programmed as 64, a 2.208 MHz clock is provided to the ADC converter according to the following formula:

$35.328 \times 4/64 = 2.208$

If NCO_DELTA [7:4] is set to –1, NCO_DELTA [3:0] is set to 3, and NCO_DIV_DELAY is set to 2 (NCO_DIV_DELAY should be the last register to be programmed), register NCO_DEF will change to 63,63,63,64 at the beginning of the third sampling period. Each number (63 or 64) only last one clock (2.208 MHz) cycle. And the combination 63,63,63,64 occurs only once. Reprogramming of register NCO_DIV_DELAY is needed if further adjustment is required.

Figure 7 shows the timing of SCLK with the following setting:

NCO_DELTA [7:4] = 1 (Delta)
NCO_DELTA [3:0] = 1 (Repeat)
NCO_DIV_DELAY = 2 (Delay)

Also note that in DPLL mode, the ADC clock will work at 2.208 MHz, 2 times oversampled, (instead of 4.416 MHz used in the VCXO mode) and the DAC clock will continue to work at 4.416 MHz.

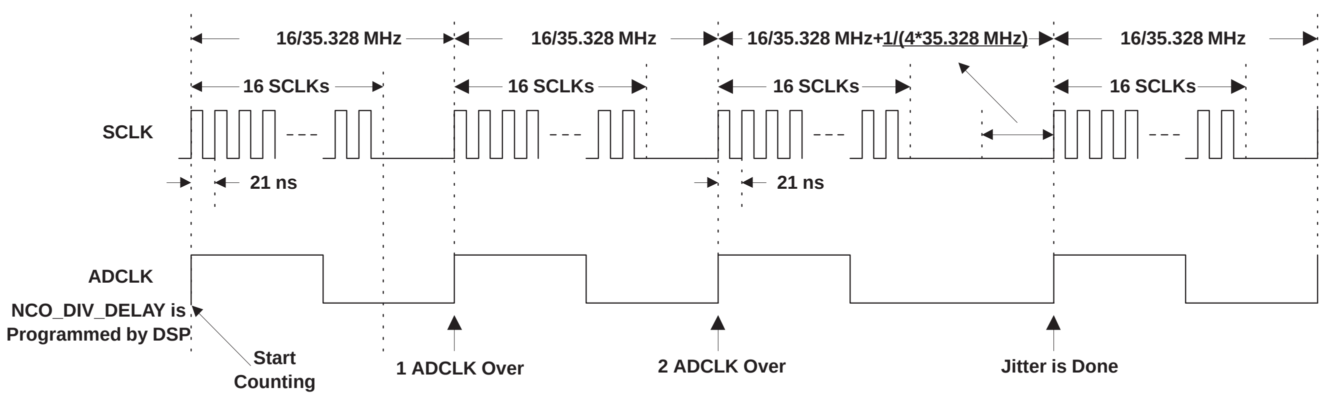



**Figure 8. ADCLK Jitter Example**

## DPLL detailed description (continued)

To prevent variation in the serial clock width (SCLK) due to jitter, the serial clock is modified to have a fixed high level of 14 ns and a low level of 7 ns, thus resulting in a period of 21 ns. The average clock frequency is still 35.328 MHz. After the 16 SCLKs are complete, the clock goes quiet (no toggle zone) until the rising edge of the next ADCLK. The length of the *no-toggle zone* varies with the ADCLK. Figure 9 illustrates an example.

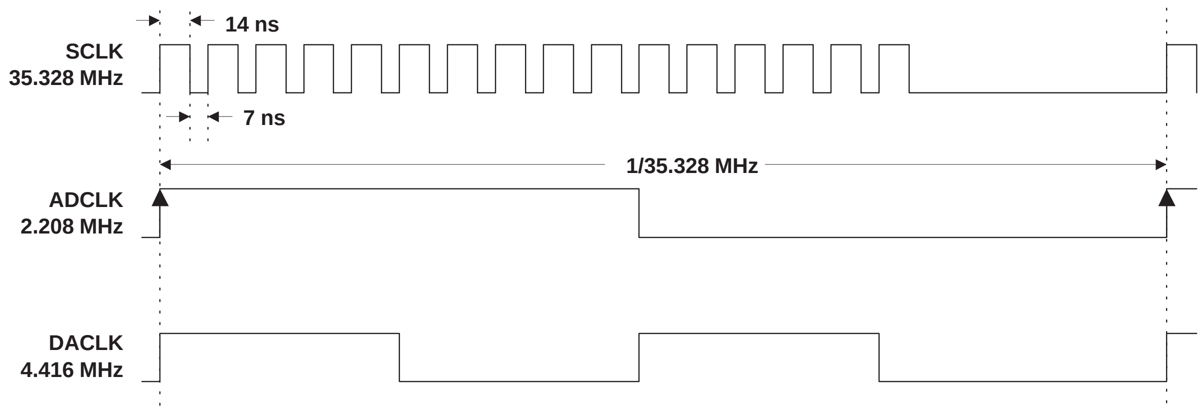



**Figure 9. Relation of SCLK With ADCLK/DACLK in DPLL Mode**

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AVDD to AGND, DVDD to DGND . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to 4.5 V
Analog input voltage range to AGND . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to AVDD+0.3 V
Digital input voltage range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to DVDD+0.3 V
Operating virtual junction temperature range, $T_J$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –40°C to 150°C
Operating free-air temperature range, $T_A$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –40°C to 85°C
Storage temperature range, $T_{str}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

### power supply

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | AVDD_RX, AVDD_TX, AVDD_REF | 3 | 3.3 | 3.6 | V |
| | DVDD, DVDD_IO, DVDD_RX | 3 | 3.3 | 3.6 | |

### digital inputs

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| High-level input voltage, $V_{IH}$ | Digital power supply = 3.3 V | 2.4 | | | V |
| Low-level input voltage, $V_{IL}$ | | | | 0.6 | |

### analog input

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog input signal range | AVDD_RX = 3.3 V, The input signal is measured single ended. | | AVDD_RX/2±0.75 | | V |
| | AVDD_RX = 3.3 V, The input signal is measured differentially. | | 3 | | Vp-p |

## recommended operating conditions (continued)

### clock

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input clock frequency | | | 35.328 | | MHz |
| Input clock duty cycle | | | 50% | | |

## electrical characteristics over recommended operating free-air temperature range, $f_{MCLKIN}$ = 35.328 MHz, AVDD_RX/AVDD_TX/AVDD_REF = 3.3 V, DVDD = DVDD_IO = DVDD_RX = 3.3 V, (unless otherwise noted)

### TX channel (measured differentially)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Gain error | | –1.5 | | 1.5 | dB |
| | PAA step gain error | | | ±0.25 | | dB |
| | DC offset | | | 50 | 100 | mV |
| | Cross-talk | RX to TX channel | | –70 | | dB |
| | Idle channel noise | | | 65 | | µVrms |
| | Group delay | | | 30 | | µs |
| | Power supply rejection ratio (PSRR) | 200 mVp-p at 75 kHz | | 70 | | dB |
| | Analog output voltage | Load = 2000 Ω | | 3 | | Vp-p |
| **AC Performance** | | | | | | |
| SNR | Signal-to-noise ratio | 70 kHz at –1 dB (see Note 14) | | 70 | | dB |
| THD | Total harmonic distortion ratio | 70 kHz at –1 dB (see Note 14) | | 75 | | dB |
| TSNR | Signal-to-noise + harmonic distortion ratio | 70 kHz at –1 dB (see Note 14) | | 68 | | dB |
| MT | Missing-tone test (see Note 15) | 30.1875 kHz | | –71 | | dB |
| | | 81.9375 kHz | | –71 | | dB |
| | | 129.375 kHz | | –71 | | dB |
| **Channel Frequency Response (Refer to Figure 13)** | | | | | | |
| | Filter gain relative to gain at 77.625 kHz | 30 kHz | –1.5 | | 1.5 | dB |
| | | Pass-band (ripple) | –1 | | 1 | dB |
| | | 180 kHz | | –70 | | dB |

NOTES: 14. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The normal differential output with this input condition is 3 $V_{pp}$.
15. 27 tones, 25.875 to 138 kHz, 4.3125 kHz/step, 0 dB

### reference outputs

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| REFP | AVDD_REF = 3.3 V | 2.2 | 2.5 | 2.8 | V |
| REFM | AVDD_REF = 3.3 V | 0.3 | 0.5 | 0.7 | V |
| TXBANDGAP | AVDD_REF = 3.3 V | 1.4 | 1.5 | 1.6 | V |
| RXBANDGAP | AVDD_REF = 3.3 V | 1.4 | 1.5 | 1.6 | V |
| VMID_RX | AVDD_REF = 3.3 V | | 1.5 | | V |

### digital outputs

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 2 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = –2 mA | | | 0.6 | V |

## electrical characteristics over recommended operating free-air temperature range, $f_{MCLKIN}$ = 35.328 MHz, AVDD_RX/AVDD_TX/AVDD_REF = 3.3 V, DVDD = DVDD_IO = DVDD_RX = 3.3 V, (unless otherwise noted) (continued)

### RX channel (measured differentially)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Gain error | | –1.5 | | 1.5 | dB |
| | PGA step gain error | PGA 1 (0 to 12 dB in 3-dB steps) | | ±1 | | dB |
| | | PGA 2 (0 to 18 dB in 6-dB steps) | | ±1 | | |
| | | PGA 3 (0 to 9 dB in 0.25-dB steps) | | ±0.15 | | |
| | DC offset | | | 50 | 100 | mV |
| | Cross-talk | TX to RX channel | | –55 | | dB |
| | Group delay | | | 25 | | µs |
| | Idle-channel noise | | | 100 | | µVrms |
| | Common-mode rejection ratio (CMRR) | | | 70 | | dB |
| | Power supply rejection ratio (PSRR) | 200 mVp-p at 75 kHz | | 70 | | dB |
| | Analog input self-bias dc voltage | | | 1.5 | | V |
| | Input impedance | RXINP/M | | 7 | | kΩ |
| | | HPF1INP/M | | 70 | | pF |
| | | HPF2INP/M | | 70 | | pF |
| **AC Performance** | | | | | | |
| SNR | Signal-to-noise ratio | 270 kHz at –1 dB (see Note 16) | | 72 | | dB |
| THD | Total harmonic distortion ratio | | | 82 | | |
| TSNR | Signal-to-noise + harmonic distortion ratio | | | 72 | | |
| MT | Missing-tone test (see Note 17) | 163.875 kHz | | –57 | | dB |
| | | 301.875 kHz | | –57 | | |
| | | 508.875 kHz | | –57 | | |
| **Channel Frequency Response (EQ[2:0] = 0 dB/MHz) (Refer to Figures 15 and 16)** | | | | | | |
| | Filter gain relative to gain at 276 kHz | 180 kHz | –1.5 | | 1.5 | dB |
| | | Pass-band (ripple) | –1 | | 1 | |
| | | 800 kHz | | –25 | | |

NOTES: 16. The analog input test signal is a sine wave with 0 dB = 3 Vp-p as the reference level.
17. 123 tones, 25.875 kHz to 552 kHz, 4.3125 kHz/step, –6 dB.

## electrical characteristics over recommended operating free-air temperature range, $f_{MCLKIN}$ = 35.328 MHz, AVDD_RX/AVDD_TX/AVDD_REF = 3.3 V, DVDD = DVDD_IO = DVDD_RX = 3.3 V, (unless otherwise noted) (continued)

### VCXO DAC

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Resolution | | | 12 | | Bits |
| DNL | Differential nonlinearity | | | | ±1 | LSB |
| INL | Integral nonlinearity | | | | ±4 | LSB |
| | Monotonicity | | | | 12 | Bits |
| | Channel gain error | | | | | dB |
| | Offset error | | –100 | | 100 | mV |
| **Analog Output** | | | | | | |
| | Full scale output voltage | Load = 50 kΩ, $V_{DD}$ = 3.3 V | | 3 | | V |
| | Output load | | | 50 | | kΩ |

### power dissipation

| | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Power dissipation | Active mode | | | | 700 | 850 | mW |
| | Power-down mode | Hardware power down | | | 50 | 100 | |
| | | Software power down | TX only | | | | mW |
| | | | RX only | | | | |
| | | | TX + RX + Reference | | | | |

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

### serial port (see Figures 7 and 8) and DGPO (see Figure 9)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c1}$ | Period, SCLK | | 28.3 | | ns |
| $t_{d1}$ | Delay time, FSR high before SCLK↓ | 7 | | | ns |
| $t_{d2}$ | Delay time, FSR high after SCLK↓ | 7 | | | ns |
| $t_{d3}$ | Delay time, FSX high before SCLK↓ | 7 | | | ns |
| $t_{d4}$ | Delay time, FSX high after SCLK↓ | 7 | | | ns |
| $t_{d5}$ | Delay time, SDX data valid after SCLK↑ | | | 7 | ns |
| $t_{d6}$ | Delay time, GPIO becomes valid after data is sent | | | 7 | ns |
| $t_f$ | Falling time, SCLK change from high to low | | | 4.4 | ns |
| $t_{h1}$ | Hold time, SDR keep valid after SCLK↑ | 2 | | | ns |
| $t_r$ | Rising time, SCLK change from low to high | | | 4.6 | ns |
| $t_{su1}$ | Setup time, SDR valid before SCLK↑ | 6 | | | ns |

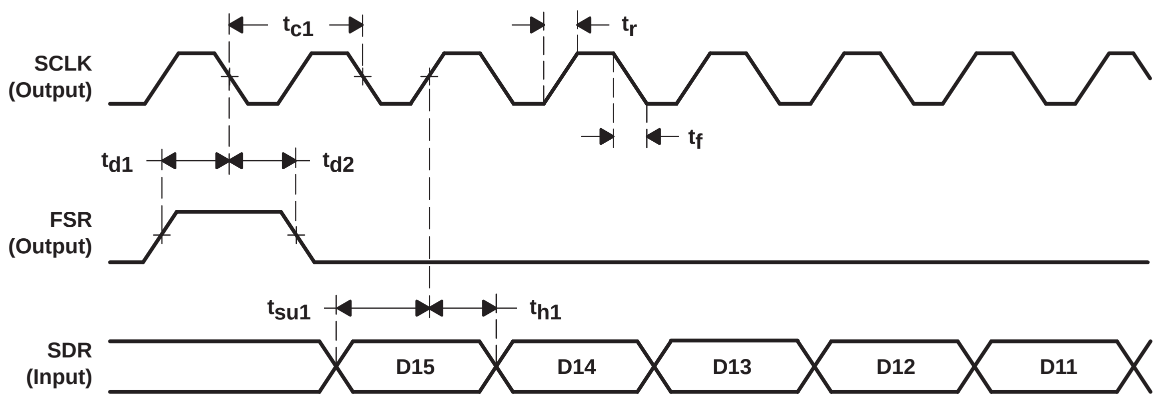



**Figure 10. Data Transfers From DSP to TLFD500PN**

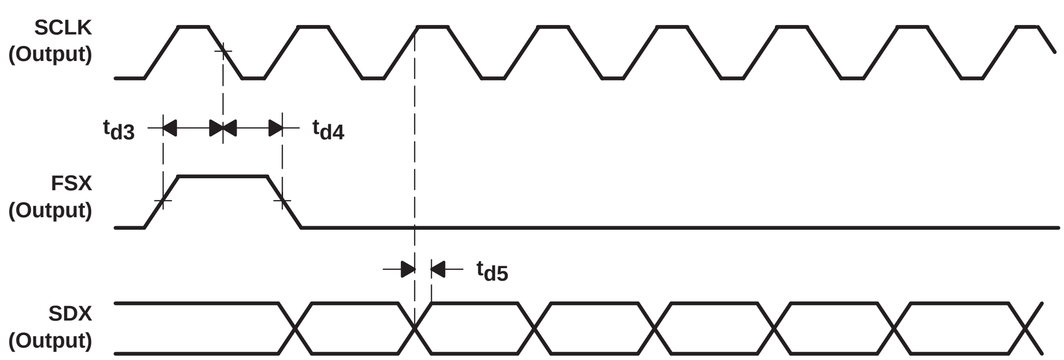



**Figure 11. Data Transfers From TLFD500PN to DSP**

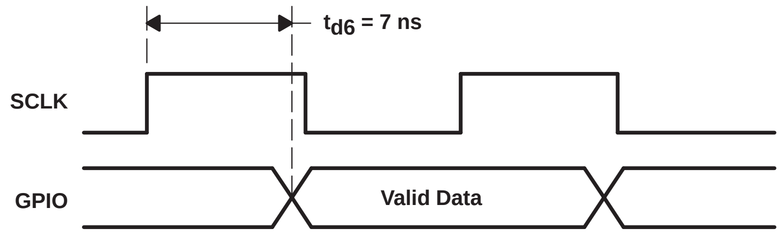



**Figure 12. GPIO Bit-to-Pin Update Timing**

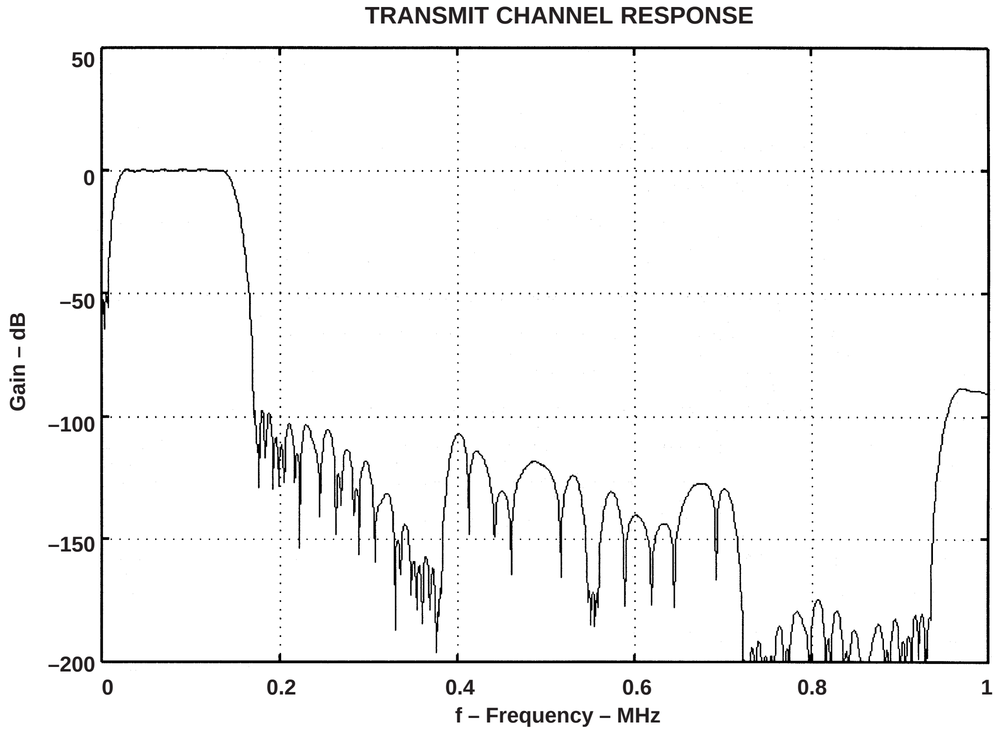



**Figure 13. Transfer Characteristic of the Transmit Filters (Complies with ITU G.992.2 PSD requirement)**

**TRANSMIT CHANNEL RESPONSE WITH HP FILTER BYPASSED**

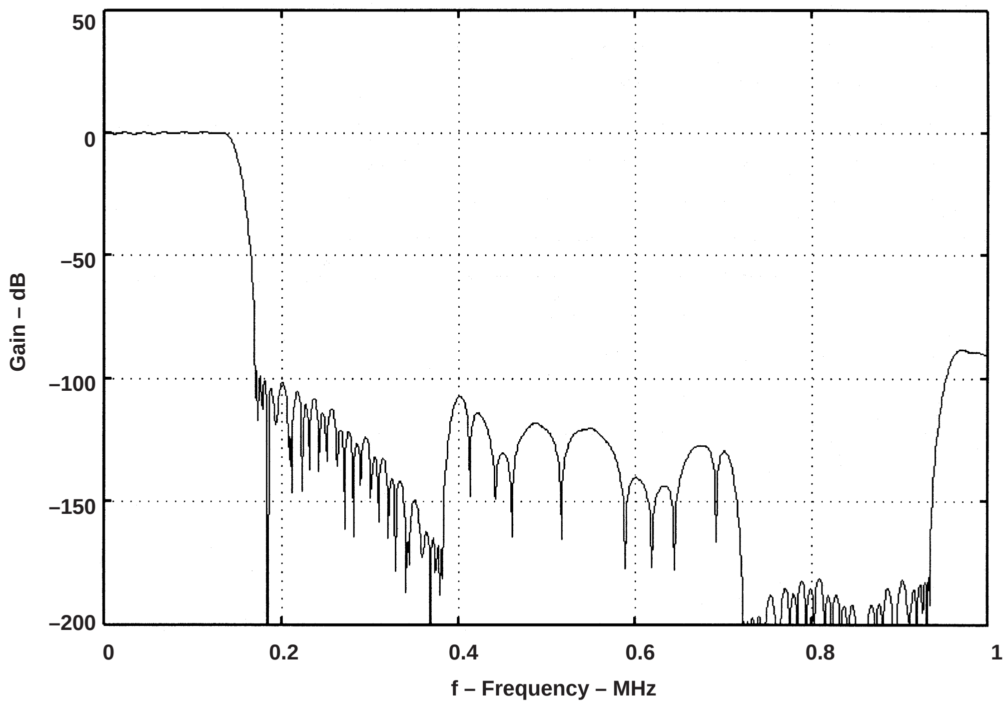



**Figure 14. Transfer Characteristic of the Transmit Filters With HP Filter Bypassed (Complies with ITU G.992.2 PSD requirement)**

**RECEIVE CHANNEL RESPONSE WITH DIFFERENT EQUALIZER SETTINGS**

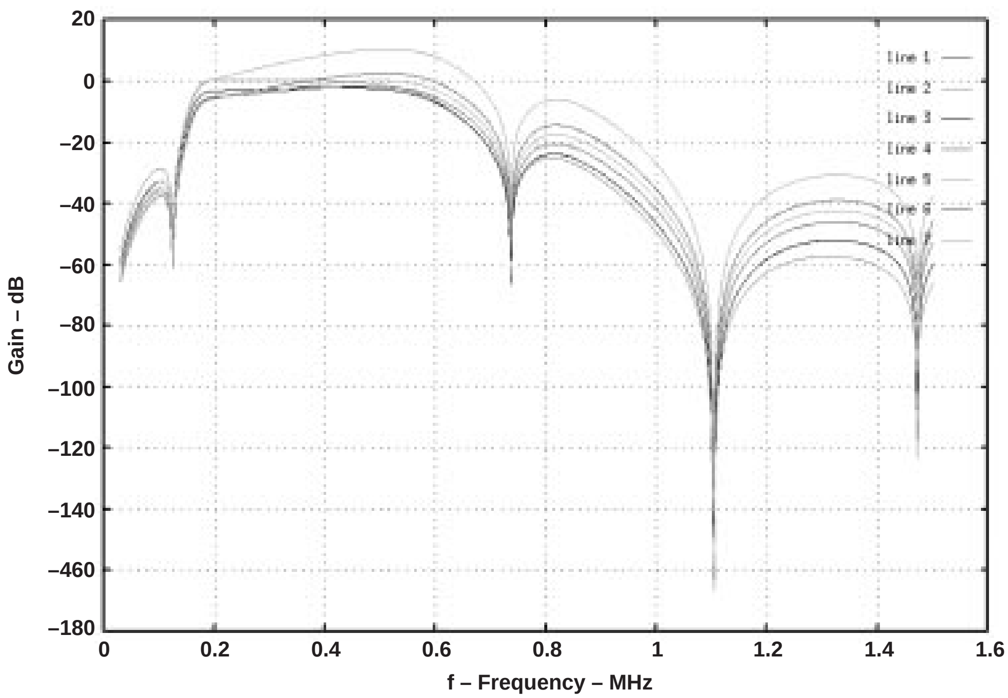



**Figure 15. Transfer Characteristic of the Receive Filters (including out of band 0–1.6 MHz) (Complies with ITU G.992.2 PSD requirement)**

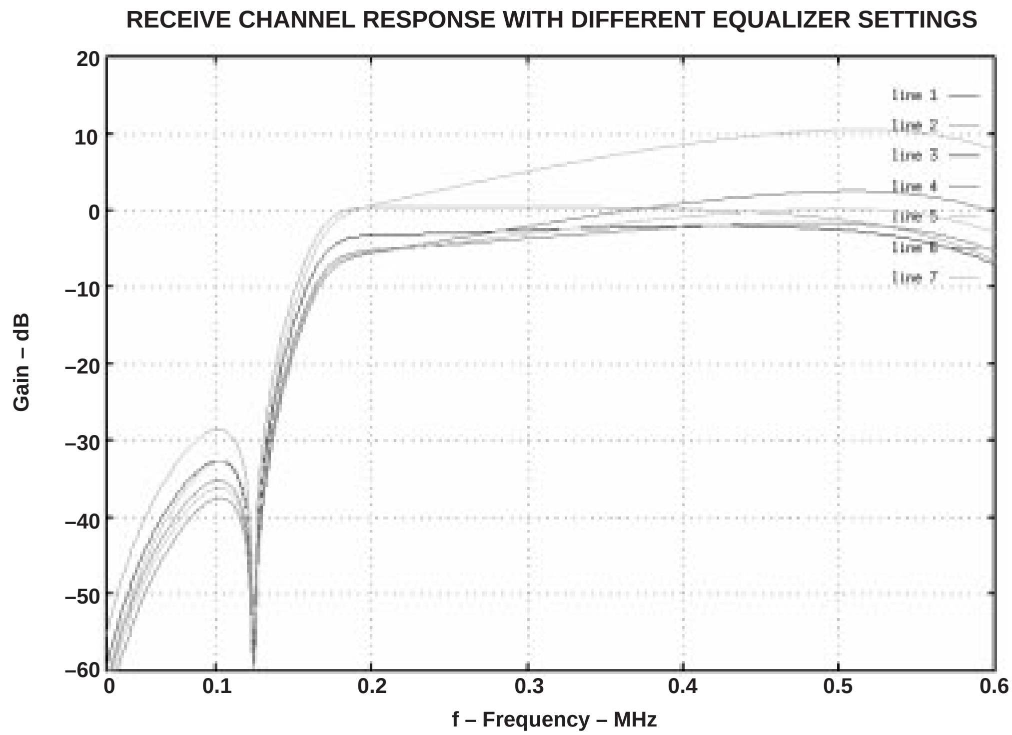



**Figure 16. Transfer Characteristic of the Receive Filters (in-band 0–0.6 MHz) (Complies with ITU G.992.2 PSD requirement)**

## APPLICATION INFORMATION

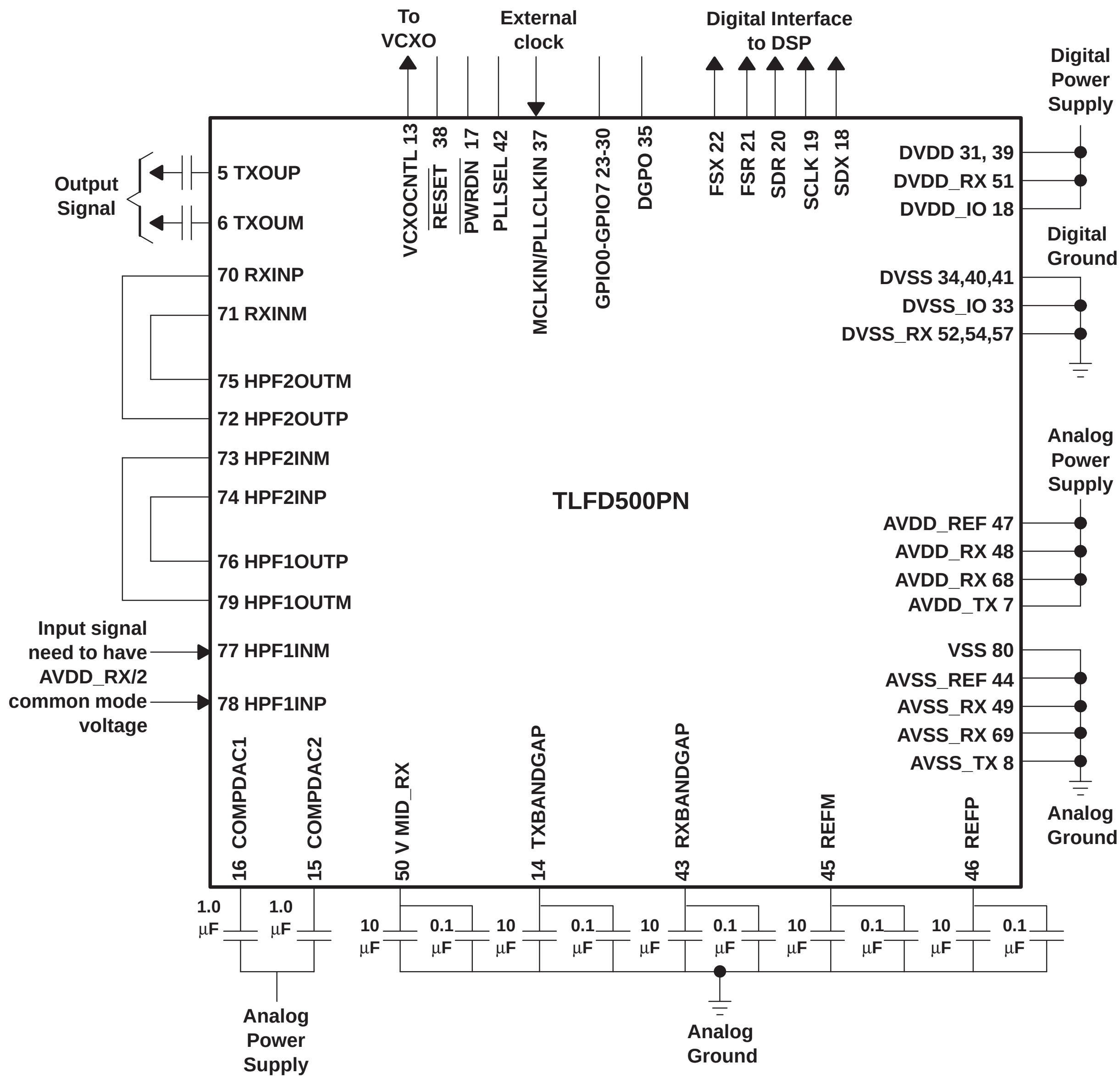
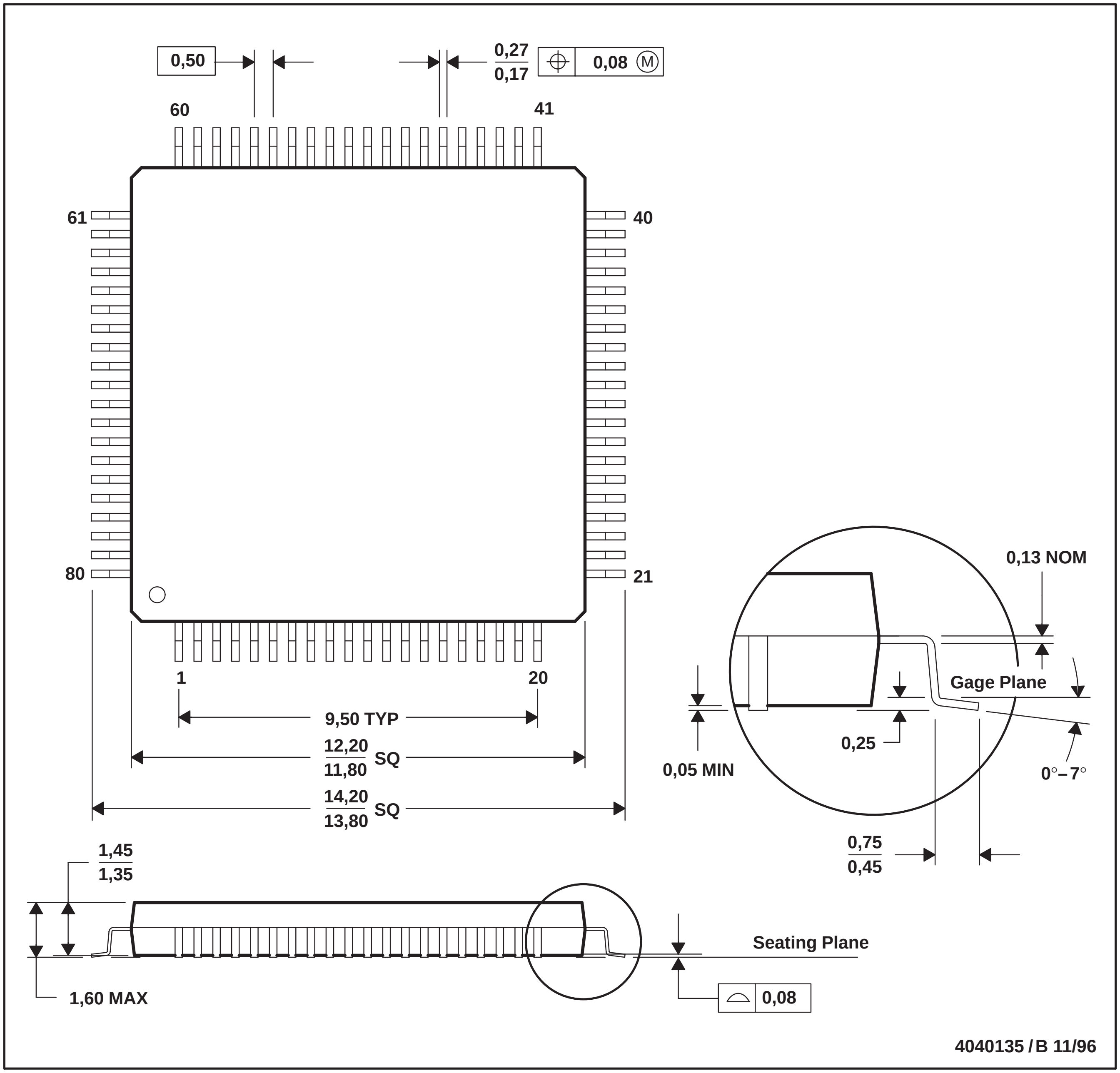



**Figure 17. Typical Application Circuit**

## MECHANICAL DATA

**PN (S-PQFP-G80)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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