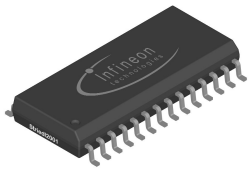
Smart Octal Low-Side Switch

Features

- Short Circuit Protection
- Overtemperature Protection
- Overvoltage Protection
- 8 bit Serial Data Input and Diagnostic Output (acc. SPI protocol)
- Direct Parallel Control of Four Channels for PWM Applications
- General Fault Flag
- Daisy chainable with other SPI devices
- Very Low Leakage Current (≤ 1µA)
- Compatible with 3V Micro Controllers
- **E**lecto**s**tatic **D**ischarge (ESD) Protection

Product Summary

Supply voltage	V_S	4.5 – 5.5	V
Drain source clamping voltage	$V_{DS(AZ)max}$	60	V
On resistance	R_{ON}	1.7	Ω
Output current (all outp.ON equal)	$I_{D(NOM)}$	200	mA
(individually)		500	mA



P-DSO 28
Ordering Code:
Q67007-A9413-A705

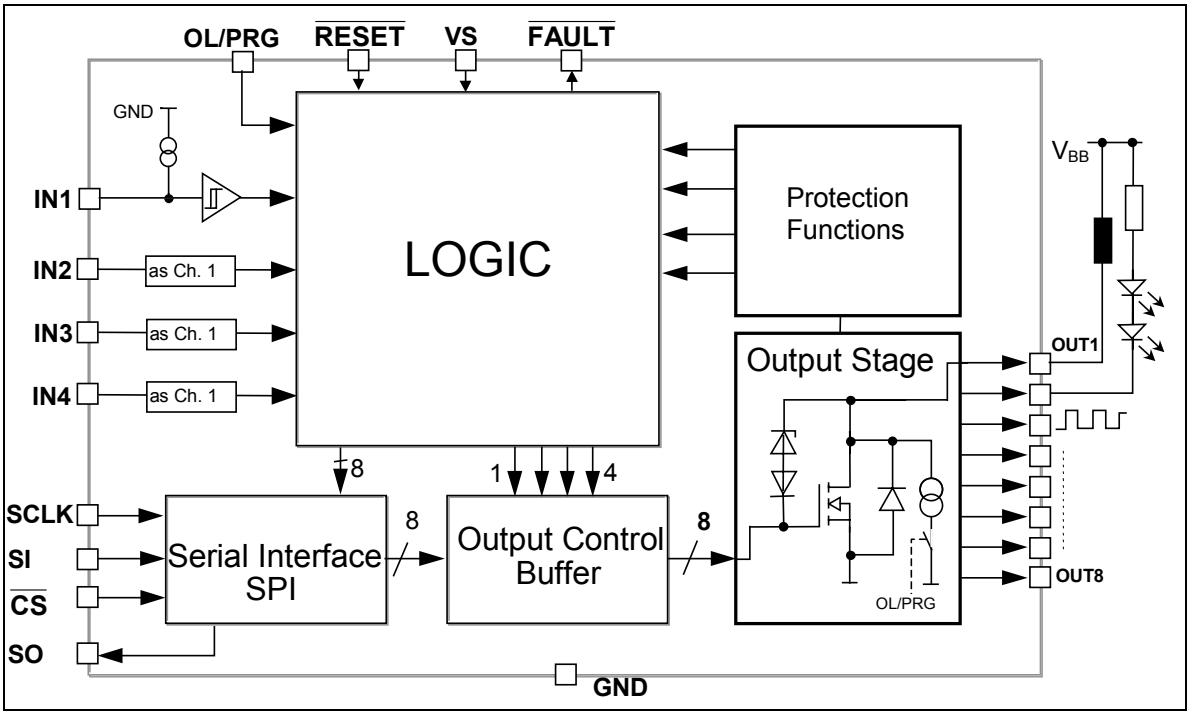
Application

- µC Compatible Power Switch for 12V and 24VApplications
- Switch for Automotive and Industrial System
- Solenoids, Relays, Resistive Loads, LEDs
- Robotic Controls

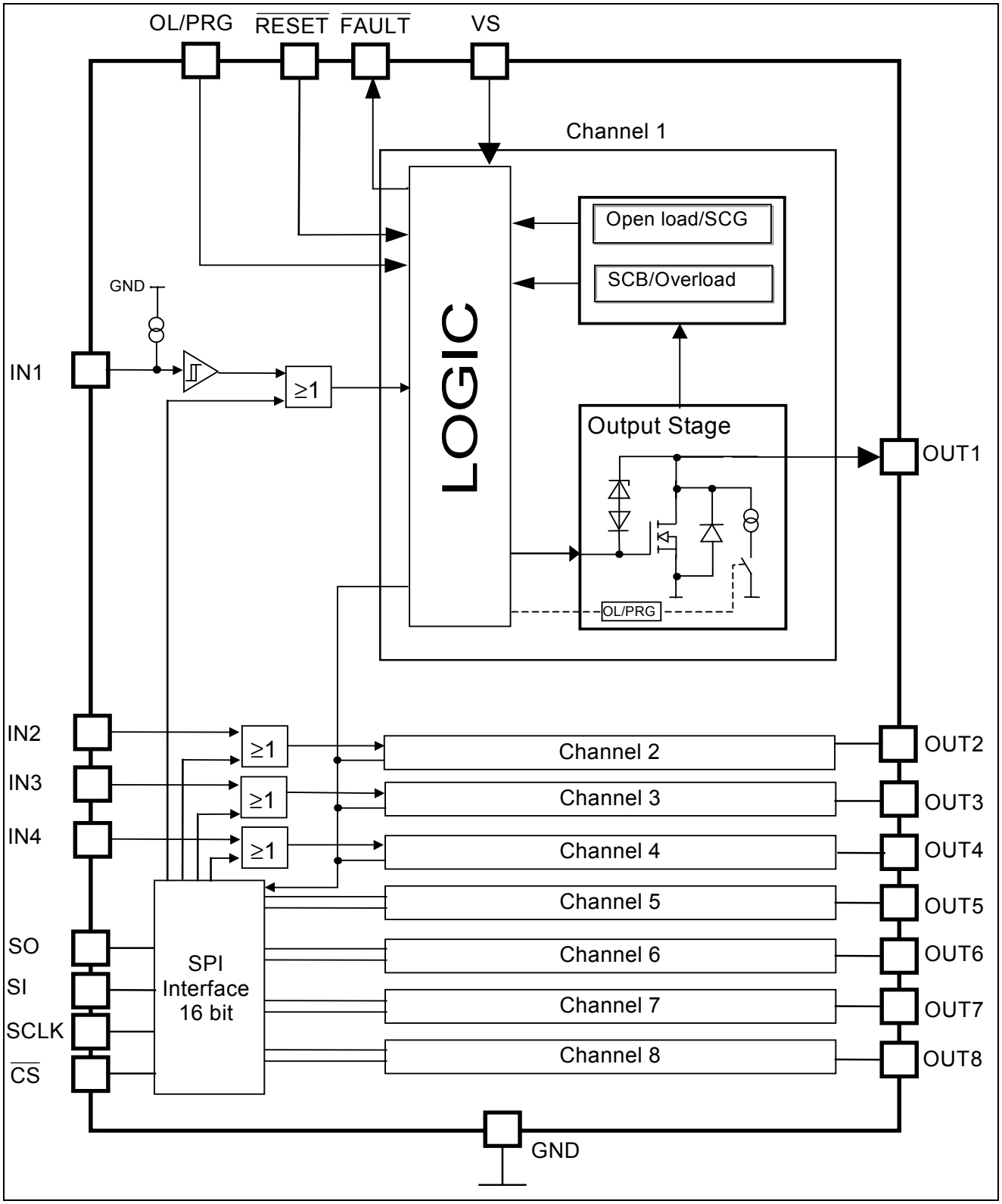
General description

Octal Low-Side Switch in Smart Power Technology (SPT) with a **S**erial **P**eripheral **I**nterface (SPI) and eight open drain DMOS output stages. The TLE 6236 G is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via an SPI Interface. Additionally four channels can be controlled direct in parallel for PWM applications. The open load detection (pull down sources) can be disabled via the OL/PRG pin. Then the leakage current is reduced to 1µA (max.) to avoid e.g. the glowing of LEDs in off state. Therefore the TLE 6236 G is particularly suitable for body control units, dash board illumination or engine management systems.

Block Diagram



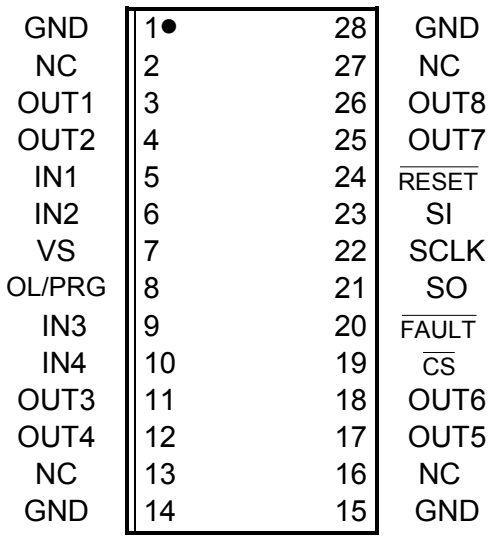
Detailed Block Diagram



Pin Description

Pin Configuration (Top view)

Pin	Symbol	Function
1	GND	Ground
2	NC	not connected
3	OUT1	Power Output Channel 1
4	OUT2	Power Output Channel 2
5	IN1	Input Channel 1
6	IN2	Input Channel 2
7	VS	Supply Voltage
8	OL/PRG	Open load actice/inactive Program Pin
9	IN3	Input Channel 3
10	IN4	Input Channel 4
11	OUT3	Power Output Channel 3
12	OUT4	Power Output Channel 4
13	NC	not connected
14	GND	Ground
15	GND	Ground
16	NC	not connected
17	OUT5	Power Output Channel 5
18	OUT6	Power Output Channel 6
19	$\overline{CS}$	Chip Select
20	$\overline{FAULT}$	General Fault Flag
21	SO	Serial Data Output
22	SCLK	Serial Clock
23	SI	Serial Data Input
24	$\overline{RESET}$	Reset
25	OUT7	Power Output Channel 7
26	OUT8	Power Output Channel 8
27	NC	not connected
28	GND	Ground



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Maximum Ratings for T_j = – 40°C to 150°C

Parameter	Symbol	Values	Unit
Supply Voltage	V_S	-0.3 ... +7	V
Continuous Drain Source Voltage (OUT1...OUT8)	V_{DS}	45	V
Input Voltage, All Inputs and Data Lines	V_{IN}	- 0.3 ... + 7	V
Operating Temperature Range Storage Temperature Range	T_j T_{stg}	- 40 ... + 150 - 55 ... + 150	°C
Output Current per Channel (see el. characteristics)	$I_{D(lim)}$	$I_{D(lim)\ min}$	A
Output Current per Channel @ T_A = 25°C (All 8 Channels ON; Mounted on PCB) [1)]	I_D	250	mA
Output Clamping Energy I_D = 0.25 A	E_{AS}	10	mJ
Power Dissipation (mounted on PCB) @ T_A = 25°C	P_{tot}	2	W
Electro**s**tatic **D**ischarge **V**oltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	2000	V
DIN Humidity Category, DIN 40 040		E	
IEC Climatic Category, DIN IEC 68-1		40/150/56	
Thermal Resistance junction - pin junction - ambient @ min. footprint	 R_{thJP} R_{thJA}	 25 80	 K/W

[1)] Output current rating so long as maximum junction temperature is not exceeded. At T_A = 125 °C the output current has to be calculated using R_{thJA} according mounting conditions.

Electrical Characteristics

Parameter and Conditions V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; Reset = H (unless otherwise specified)	Symbol	Values			Unit
		min	typ	max	
1. Power Supply					
Supply Voltage	V_S	4.5	--	5.5	V
Supply Current	I_S	--	1.5	3	mA
Supply Current (in Standby Mode, RESET = L)[1]	$I_{S(Stdby)}$	--		50	µA
2. Power Outputs					
ON Resistance V_S = 5 V; I_D = 500 mA T_J = 25°C T_J = 150°C	$R_{DS(ON)}$	-- --	1.7 3	-- 4	Ω
Output Clamping Voltage Output OFF	$V_{DS(AZ)}$	45	--	60	V
Current Limit	$I_{D(lim)}$	500	750	1000	mA
Output Leakage Current V_{Reset} = L [2]	$I_{D(lkg)}$	--	--	1	µA
Turn-On Time I_D = 0.25 A, resistive load	t_{ON}	--	6	10	µs
Turn-Off Time I_D = 0.25 A, resistive load	t_{OFF}	--	6	10	µs
3. Digital Inputs					
Input Low Voltage	V_{INL}	- 0.3	--	1.0	V
Input High Voltage	V_{INH}	2.0	--	--	V
Input Voltage Hysteresis	V_{INHys}	100	200	--	mV
Input Pull Down Current (IN1 ... IN4)	$I_{IN(1..4)}$	20	50	100	µA
OL/PRG, Reset Pull Up Current	$I_{IN(OL/PRG,Res)}$	20	50	100	µA
Input Pull Down Current (SI, SCLK)	$I_{IN(SI,SCLK)}$	10	20	50	µA
Input Pull Up Current ($\overline{CS}$)	$I_{IN(CS)}$	10	20	50	µA
4. Digital Outputs (SO, $\overline{FAULT}$)					
SO High State Output Voltage I_{SOH} = 2 mA	V_{SOH}	V_S – 0.5V	--	--	V
SO Low State Output Voltage I_{SOL} = 2 mA	V_{SOL}	--	--	0.4	V
SO Output Tri-state Leakage Current $\overline{CS}$ =H, 0 ≤ V_{SO} ≤ V_S	I_{SOlkg}	-10	0	10	µA
FAULT Output Low Voltage I_{FAULT} = 1.6 mA	V_{FAULTL}	--	--	0.4	V
5. Diagnostic Functions					
Open Load Detection Voltage	$V_{DS(OL)}$	0.6*V_S	0.7*V_S	0.8*V_S	V
Output Pull Down Current	$I_{PD(OL)}$	200	300	450	µA
Fault Delay Time	$t_{d(fault)}$	50	100	200	µs
Overload Threshold Current	$I_{D(lim)\ 1...8}$	500	700	1000	mA
Overtemperature Shutdown Threshold	$T_{th(sd)}$	170	--	200	°C
Hysteresis	T_{hys}	--	10	--	K

[1] Test conditions : No floating digital Inputs
[2] Measured on wafer level

Electrical Characteristics cont.

Parameter and Conditions	Symbol	Values			Unit
V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; Reset = H (unless otherwise specified)		min	typ	max	
6. SPI-Timing					
Serial Clock Frequency	f_{SCK}	DC	--	5	MHz
Serial Clock Period (1/fclk)	$t_{p(SCK)}$	200	--	--	ns
Serial Clock High Time	t_{SCKH}	80	--	--	ns
Serial Clock Low Time	t_{SCKL}	80	--	--	ns
Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of CLK)	t_{lead}	250	--	--	ns
Enable Lag Time (falling edge of CLK to rising edge of $\overline{CS}$)	t_{lag}	250	---	--	ns
Data Setup Time (required time SI to falling of CLK)	t_{SU}	--	25	--	ns
Data Hold Time (falling edge of CLK to SI)	t_H	--	25	--	ns
Enable Time	t_{EN}	250	--	--	ns
Disable Time	t_{DIS}	250	--	--	ns
Data Valid Time C_L = 50 pF[1]	t_{valid}	--	110	160	ns
C_L = 100 pF[1]		--	120	170	
C_L = 220 pF[1]		--	150	200	

[1] This parameter will not be tested but guaranteed by design

Functional Description

The TLE 6236 G is an octal-low-side power switch which provides a serial peripheral interface (SPI) to control the 8 power DMOS switches, as well as diagnostic feedback. The power transistors are protected against short to V_{BB}, overload, overtemperature and against overvoltage by an active zener clamp.
The diagnostic logic recognizes a fault condition which can be read out via the serial diagnostic output (SO).

Circuit Description

Output Stage Control

Each output is independently controlled by an output latch and a common reset line, which disables all eight outputs. Serial data input (SI) is read on the falling edge of the serial clock. A logic high input data bit turns the respective output channel ON, a logic low data bit turns it OFF. $\overline{CS}$ must be low whilst shifting all the serial data into the device. A low-to-high transition of $\overline{CS}$ transfers the serial data input bits to the output buffer.

Special conditions for Channel 1 to 4:
In addition to the serial control of the outputs it is possible to control channel 1 to channel 4 directly in parallel for PWM applications. These inputs are high active and **ORed** with the SPI control bit. The parallel inputs are provided with internal pull down sources, to guarantee that the channels are switched off when the inputs are not connected.

The table shows the OR-operation of the parallel inputs 1 ..4 and the corresponding SPI bits.

IN 1 - 4	SPI-Bit 0 - 3	OUT 1 - 4
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

The outputs 5 .. 8 can be controlled in serial via SPI Interface

SPI-Bit 4 - 7	OUT 5 - 8
0	OFF
1	ON

Serial Control Bits (SI)

Ch. 8	Ch. 7	Ch. 6	Ch. 5	Ch. 4	Ch. 3	Ch. 2	Ch. 1
7	6	5	4	3	2	1	0

MSB LSB

Serial Diagnostic Bits (SO)

DIAG7	DIAG6	DIAG5	DIAG4	DIAG3	DIAG2	DIAG1	DIAG0
7	6	5	4	3	2	1	0

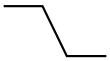
MSB LSB

Power Transistor Protection Functions[1)]

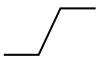
Each of the eight output stages has its own zener clamp, which causes a voltage limitation at the power transistor when solenoid loads are switched off. The outputs are provided with a current limitation set to a minimum of 500 mA. The continuous current for each channel is 200 mA (all channels ON).
Each output is protected by embedded protection functions. In the event of an overload or short to supply, the current is internally limited and a fault bit is generated for each output individually (early warning). If this operation leads to an overtemperature condition, a second protection level (about 170 °C) will change the output into a low duty cycle PWM (channel selective thermal shutdown with restart) to prevent critical chip temperatures.

SPI Signal Description

$\overline{CS}$ - Chip Select. The system microcontroller selects the TLE 6236 G by means of the $\overline{CS}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.



$\overline{CS}$ High to Low transition: - diagnostic status information is transferred from the power outputs into the shift register.
- serial input data can be clocked in from then on
- SO changes from high impedance state to logic high or low state corresponding to the SO bits



$\overline{CS}$ Low to High transition: - transfer of SI bits from shift register into output buffers
- reset of diagnosis register

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of $\overline{CS}$. When $\overline{CS}$ is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.
The device will react to the CS  only if one correct SCLK signal has been sent.

SCLK - Serial Clock. The system clock pin clocks the internal shift register of the TLE 6236 G. The serial input (SI) accepts data into the input shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out of the shift register on the rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the falling edge of SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.
A logic high bit at this pin (within the data byte) will switch the corresponding output on.

[1)] The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently

SO - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge of SCLK.

$\overline{RESET}$ - Reset pin. If the reset pin is in a logic low state, it clears the SPI shift register and switches all outputs OFF. An internal pull-up structure is provided on chip.

Diagnostics

$\overline{FAULT}$ - Fault pin. There is a general fault pin (open drain) which shows a high to low transition as soon as an error occurs for any one of the eight channels. This fault indication can be used to generate a µC interrupt. Therefore a 'diagnosis' interrupt routine need only be called after this fault indication. This saves processor time compared to a cyclic reading of the SO information.

As soon as a fault occurs, the fault information is latched into the diagnosis register. Serial data out pin (SO) is in a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ receives a LOW signal, all diagnosis bits can be shifted out serially. The rising edge of $\overline{CS}$ will reset all error registers.

Logic table

	Parallel Input	SI Bits 0-7	SO DIAG-Bits 0-7	Output State	Output voltage V_{OUT}	Operating Mode
1	L	L	L	OFF	>Vref	normal function
2	L	H	H	ON	< Vref	normal function
3	H	L	L	ON	< Vref	normal function
4	H	H	H	ON	< Vref	normal function
5	L	L	H	OFF	< Vref	open load/short to gnd
6	L	H	L	ON	>Vref	overload
7	H	L	H	ON	>Vref	overload
8	H	H	L	ON	>Vref	overload

Table 1: Definition of diagnostic bits under parallel and serial control

Basic principle of fault detection:

SO Bit = SI Bit: **Normal Function**
SO Bit inverse to SI Bit : **Fault Condition**

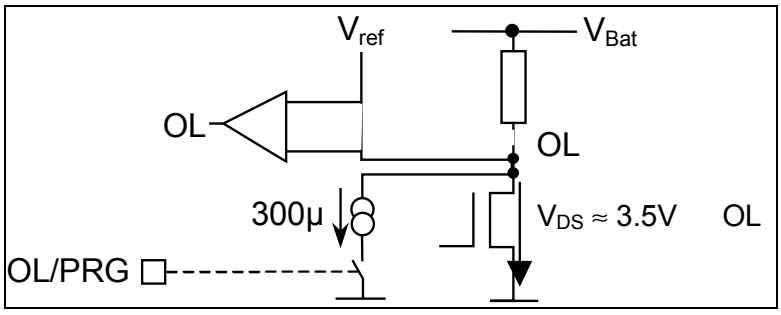
The diagnostic bits DIAG0 to DIAG3 for channel 1 to 4 indicate a fault when the DIAG bit is high during parallel control (IN1 .. IN4 = H; serial data bits 0 .. 3 = L). Note that the SPI serial input (SI) bit overrides the ON state control from IN1 to IN4 regarding diagnostic information.
Compare DIAG Bit in line 3 (parallel ON only) with DIAG Bit in line 4 (serial and parallel ON) under normal function.
Compare DIAG Bit in line 7 (parallel ON only) with DIAG Bit in line 8 (serial and parallel ON) under fault condition.

SPI serial input (SI) bit overrides the parallel ON state control from IN1 to IN4

Vref is the threshold reference level for detecting an Open Load/Overload
The standard way of obtaining diagnostic information is as follows:
Clock in serial information into SI pin and wait approximately 200 µs to allow the outputs to settle. Clock in the identical serial information once again - during this process the data coming out at SO contains the bit combinations representing the diagnosis conditions as described in figure 1.
Based on the needs of the application, a software routine should be programmed into the micro controller to set the corrective action of each fault condition.

Open Load Program Pin (OL/PRG)

To detect open load/short to ground each channel has an internal pull down source (300 µA typ.) which pulls the drain voltage under the detection threshold in case of an open load or short to ground condition.
If the TLE 6236 G is used to drive LEDs this pull down current could causes a slight glowing of the LED. To avoid this, the device is provided with a program pin, which enables or disables this open load detection. The OL/PRG pin is internally pulled up, i.e. the open load detection is enabled if the OL/PRG pin is not connected. To disable the open load detection this pin must be pulled to GND, e.g with a micro controller port.
In this way the open load detection can be enabled (e.g during start up of the system or in a diagnosis routine) and disabled (e.g. during normal operation to avoid LED glowing) by the µC.
If the open load detection is disabled, the leakage current is reduced to a maximum of 1µA.



Timing Diagrams

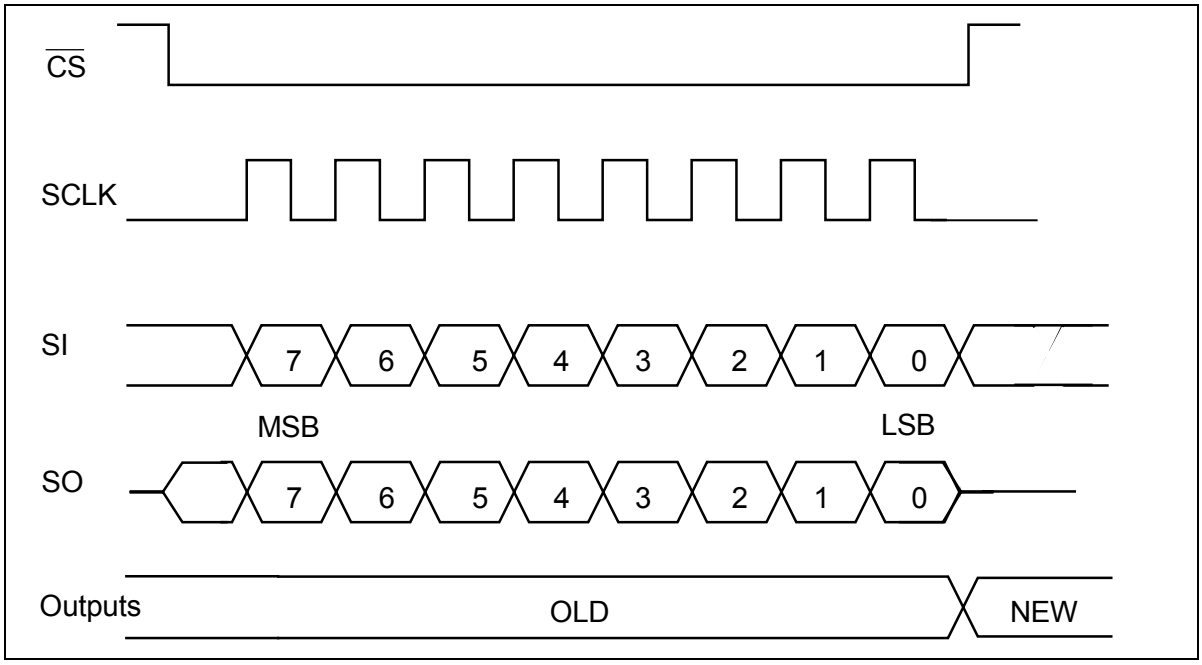


Figure 2: Serial Interface

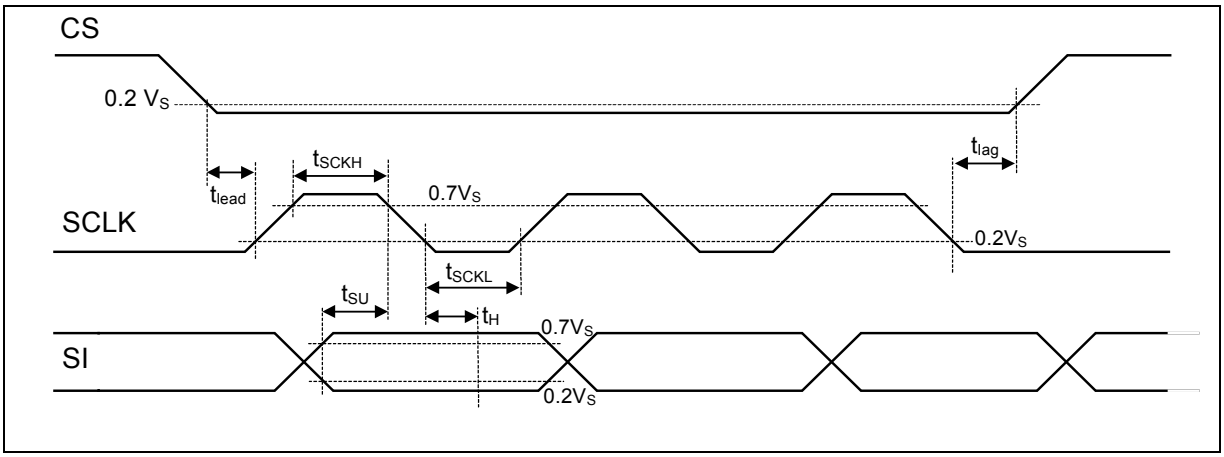


Figure 3: Input Timing Diagram

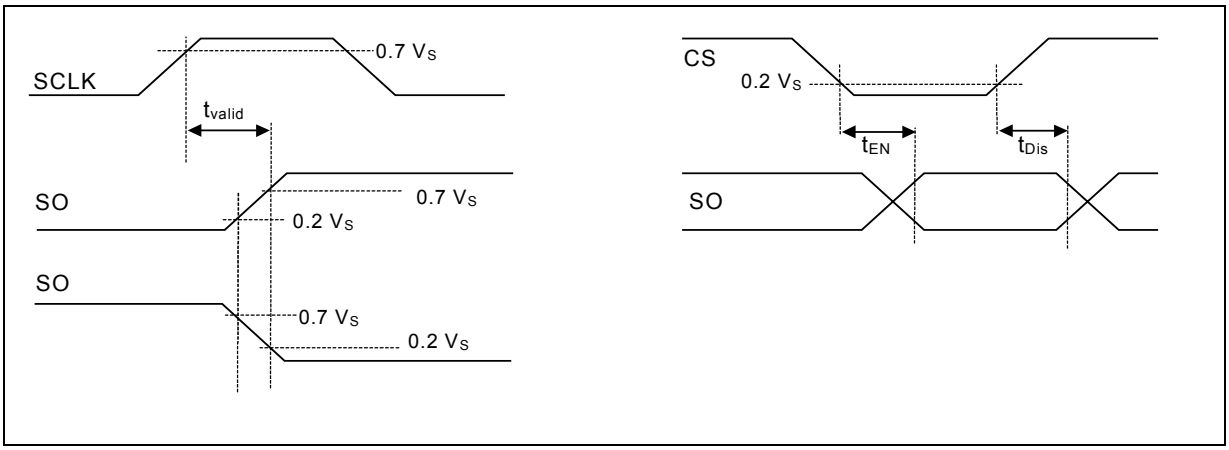


Figure 4:
SO Valid Time Waveforms **Enable and Disable Time Waveforms**

Application Circuits

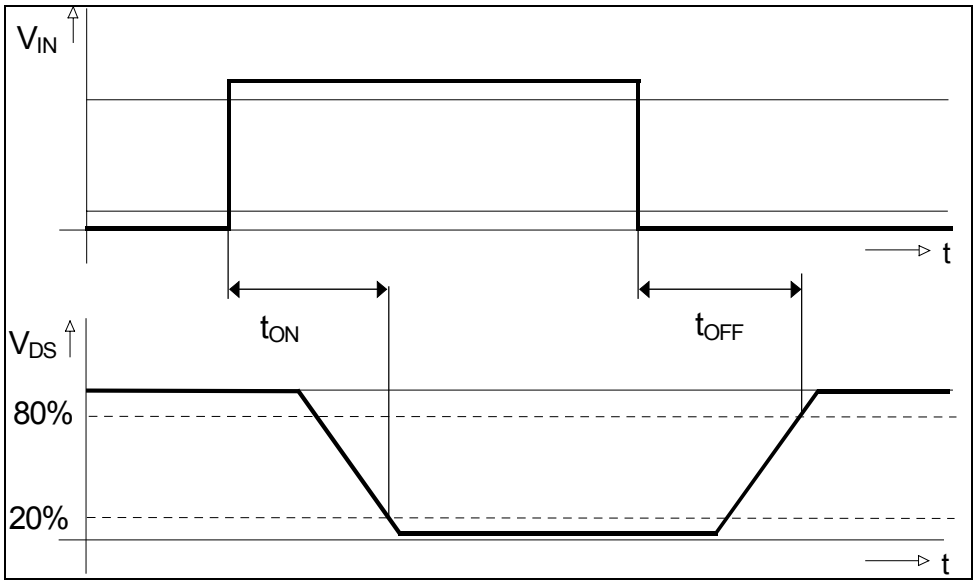
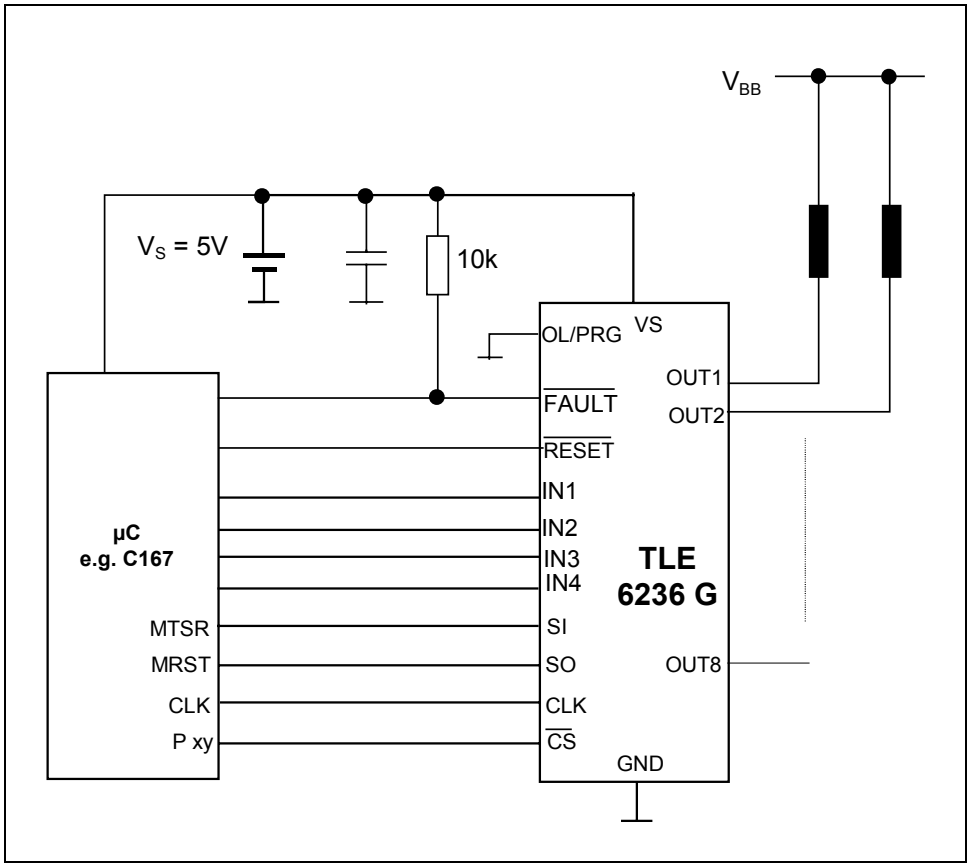


Figure 5: Power Outputs



Typical electrical Characteristics

Drain-Source on-resistance

$R_{DS(ON)} = f(T_j)$; $V_s = 5V$

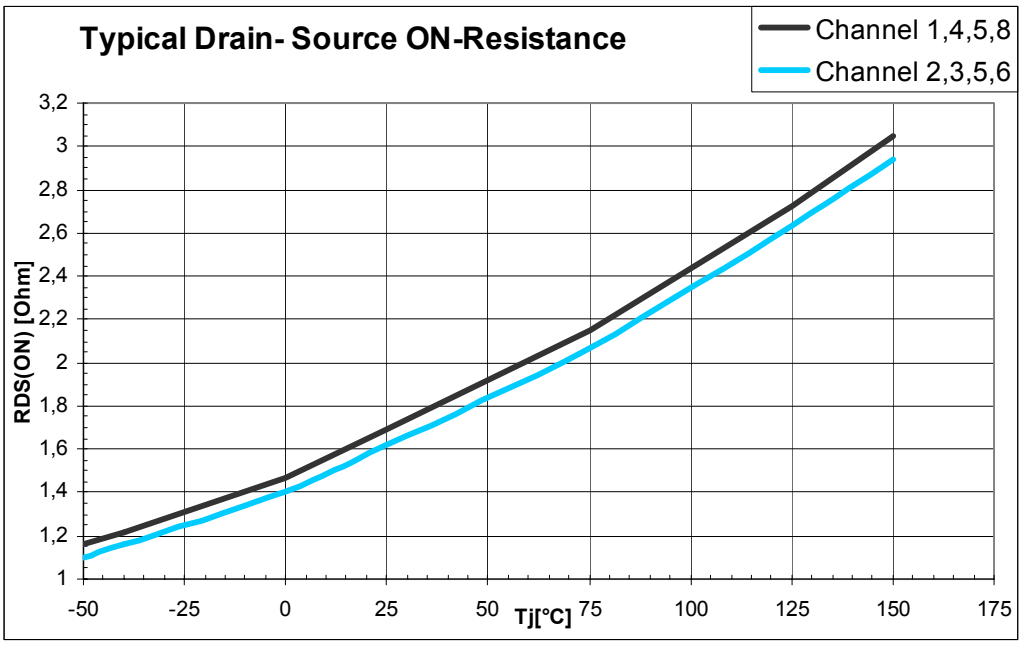


Figure 6 : Typical ON Resistance versus Junction-Temperature
Channel 1-8

Output Clamping Voltage

$V_{DS(AZ)} = f(T_j)$; $V_s = 5V$

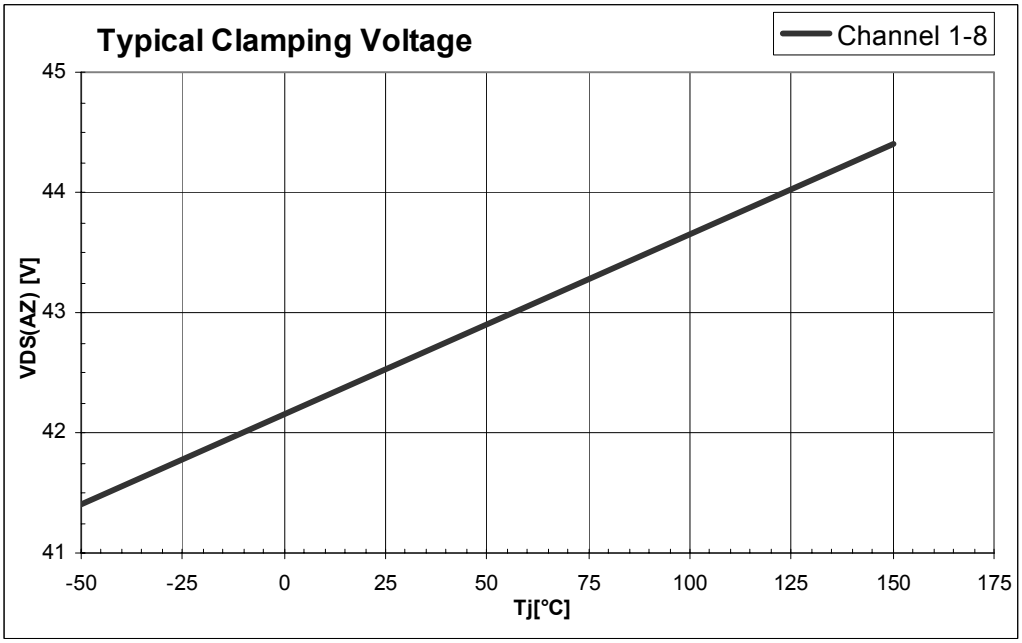
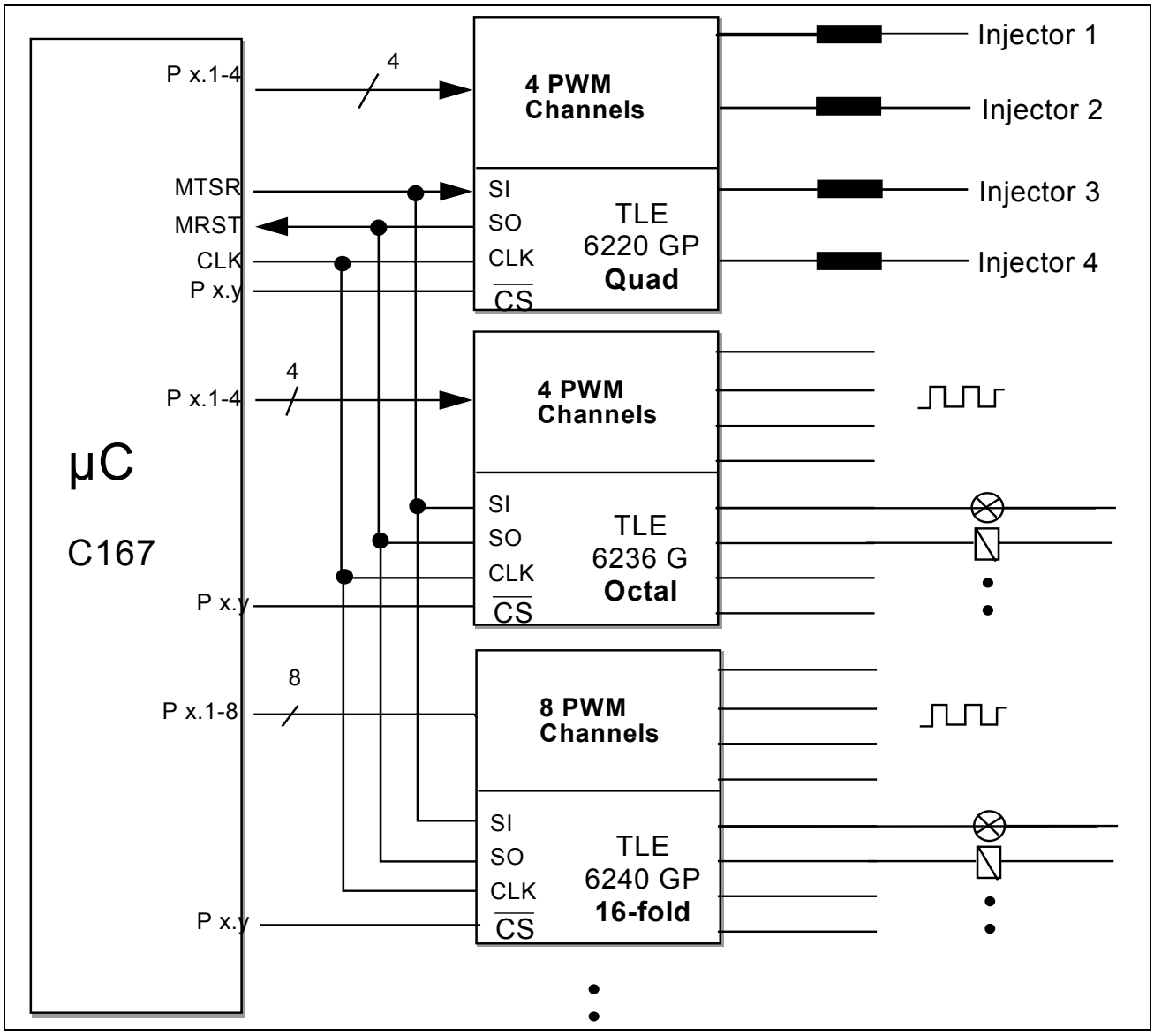


Figure 7 : Typical Clamp Voltage versus Junction-Temperature
Channel 1-8

Parallel SPI Configuration

Engine Management Application

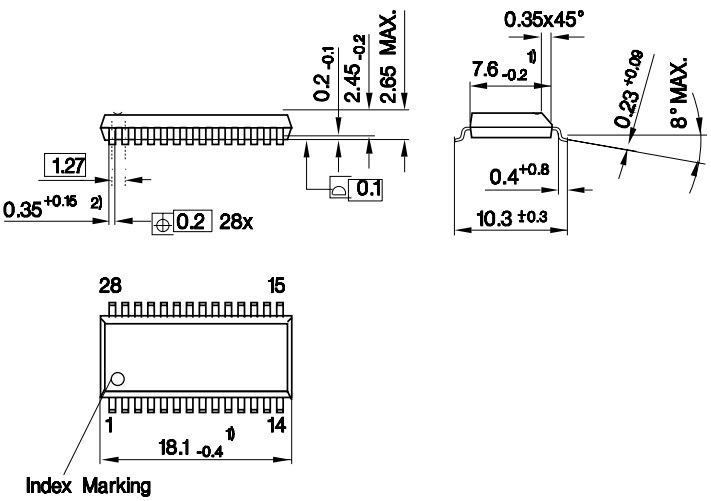
TLE 6236 G in combination with TLE 6240 GP (16-fold switch) for relays and general purpose loads and TLE 6220 GP (quad switch) to drive the injector valves. This arrangement covers the numerous loads to be driven in a modern Engine Management/Powertrain system. From 28 channels in sum 16 can be controlled direct in parallel for PWM applications.



Package and Ordering Code

(all dimensions in mm)

P-DSO 28	Ordering Code
TLE 6236 G	Q67007-A9413-A705



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

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