SIEMENS

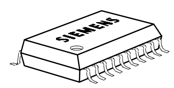
Intelligent Double Low-Side Switch 2 x 0.5 A

TLE 4214 G

Bipolar IC

Features

- Double low-side switch, 2 x 0.5 A
- Power limitation
- Overtemperature shutdown
- Overvoltage shutdown
- Status monitoring
- Shorted-load protection
- Integrated clamp diodes
- Temperature range – 40 to 125 °C



P-DSO-20-7

Type	Ordering Code	Package
TLE 4214 G	Q67000-A9094	P-DSO-20-7 (SMD)

Application

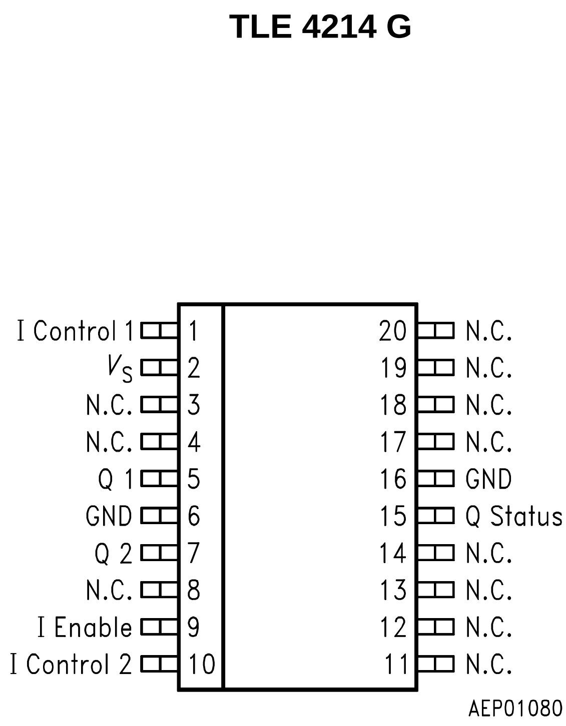
Applications in automotive electronics require intelligent power switches activated by logic signals, which are shorted-load protected and provide error feedback.

This IC contains two of these power switches (low-side switches). In case of inductive loads the integrated clamp diodes clamp the discharging voltage. If a “high” signal is applied to the enable input both switches can be activated independently of one another with TTL signals at the control inputs (active high). The high impedance inputs should always be connected to a fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions with high potential:

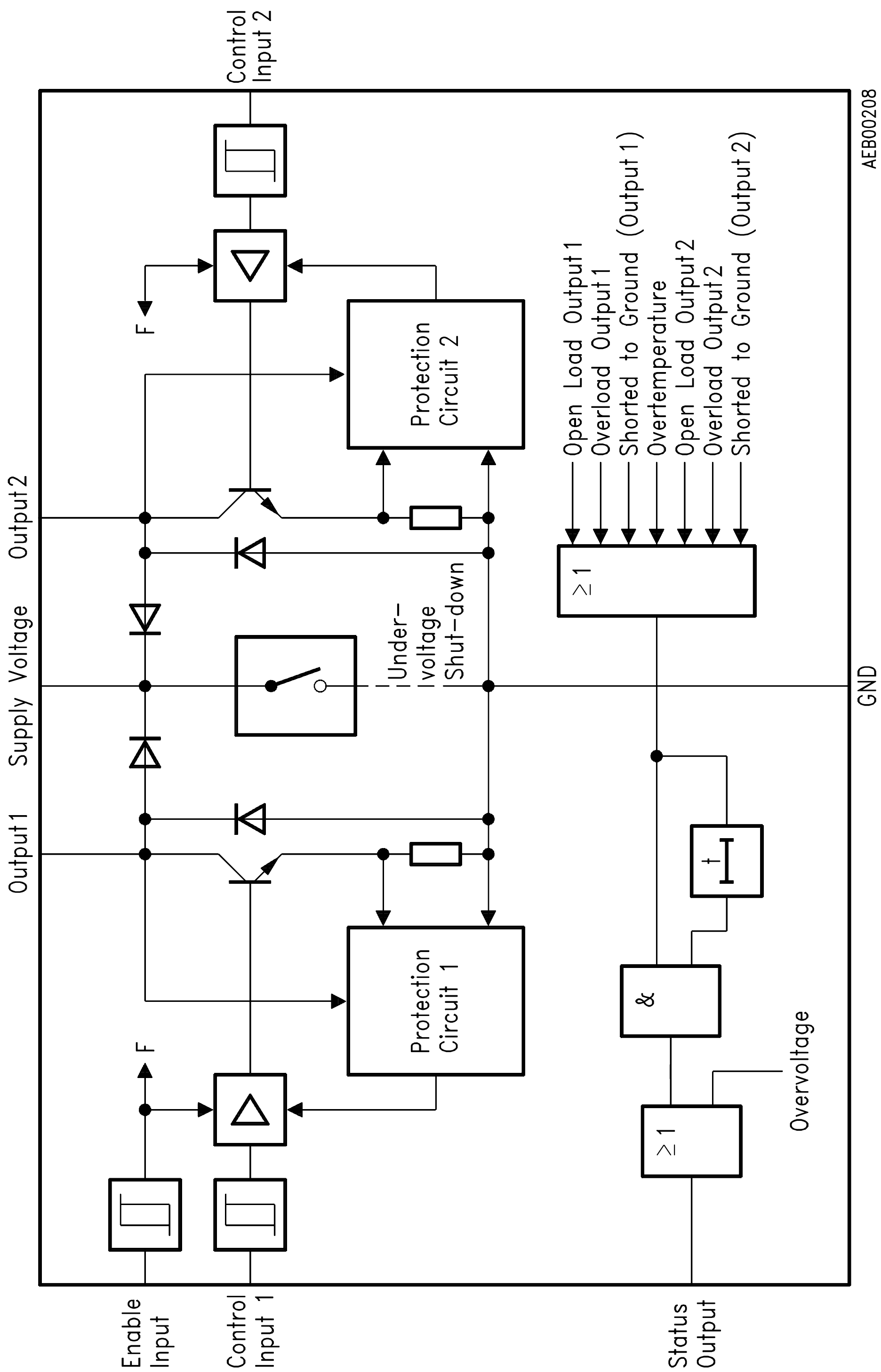
- Overload,
- Open load,
- Shorted load to ground,
- Overvoltage,
- Overtemperature.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
6, 16	GND	**Ground** Design wiring for the max. short-circuit current (2 x 1 A)
10	IN2	**Control input 2** (TTL compatible) activates the output transistor 2 in case of high potential
2	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are deactivated. The status output indicates this malfunction without delay time.
7	Q2	**Output 2** Shorted load protected, open collector output for currents up to 0.5 A, with clamping diodes to supply voltage.
5	Q1	**Output 1** Shorted load protected, open collector output for currents up to 0.5 A, with clamping diodes to supply voltage.
9	ENA	**Enable input**, active high
1	IN1	**Control input 1** (TTL-compatible) activates output transistor 1 in case of high potential
15	STA	**Status output** (open collector) for both outputs; indicates overtemperature, overload, open load and shorted load to ground as well as overvoltage at pin 3. It is switched to high after a defined delay time in case of malfunction (except: overvoltage)
3, 4, 8, 11 … 14, 17 … 20	N. C.	Not connected



Block Diagram

Circuit Description

Input Circuits

The control inputs and the enable input consist of TTL-compatible Schmitt triggers with hysteresis. Controlled by these stages the buffer amplifiers drive the NPN power transistors.

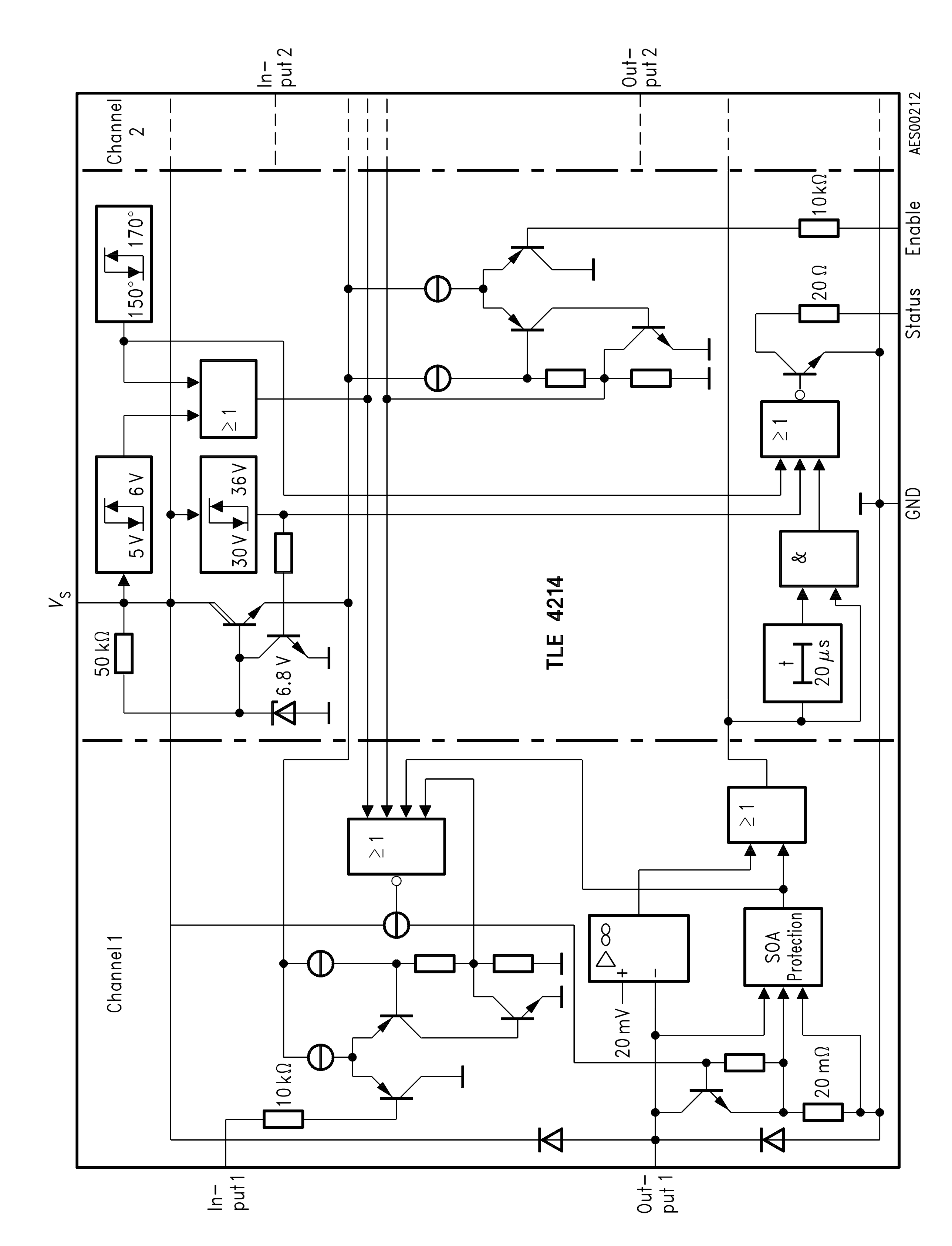
Switching Stages

The output stages consist of NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are shorted-load protected to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated clamp diodes.

Monitoring and Protective Functions

During the activated status the outputs are monitored for open load, overload, and shorted load to ground (see table below). In addition, large sections of the circuit are shut down in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active high). An internally determined delay time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal overload. If overload occurs, the outputs are protected according to the safe operating area (SOA) mode (**see diagram**). If voltage and current are outside the SOA, the outputs oscillate to reduce the power dissipation. The switching frequency depends on the internal delay time and the external load (inductances and capacitances). If the frequency is low, the status output may follow the oscillation. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no shorted load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated. At supply voltages below the operating range the output stages are de-activated.

Status Output (H = Error)				
	Undervoltage > 3.5 V	**Operating Range**		**Overvoltage**
		V_I = L (passive)	V_I = H (active)	
Normal function	L	L	L	H
Overload	L	L	H	H
Open load	L	L	H	H
Shorted output to ground	L	H	H	H
Overtemperature	L	H	H	H



Circuit Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage, $t < 0.2$ s	V_S	–	70	V
Supply voltage	V_S	– 1.3	40	V
Input voltage	V_I	– 13	40	V
Output voltage (status output)	V_O	– 0.3	40	V
Output voltage (switching stages)	V_Q	– 0.3	+ V_S	V
Currents				
Output current (switching stages)	I_Q	internally limited	–	–
Current with reverse polarity, $t < 0.1$ s	I_Q	– 0.7	–	A
Output current positive clamp	I_Q	–	0.7	A
Ground current	I_{GND}	– 1.4	2.0	A
Output current (status output)	I_O	–	10	mA
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 50	150	°C

Operating Range

Parameter	Symbol	min.	max.	Unit
Supply voltage	V_S	6 [1)]	25	V
Supply voltage slew rate	dV_S/dt	– 1	1	V/µs
Output current (switching stages)	I_Q	– 0.5	0.5	A
Input voltage	V_I, V_F	– 5	32	V
Output current (status output)	I_O	0	5	mA
Ambient temperature	T_A	– 40	125	°C

1) Lower limit = 5 V, if previously V_S greater than 6 V (turn-on hysteresis)

Absolute Maximum Ratings (cont'd)

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage while shorted load	V_S	–	15	V
Thermal resistance junction to ambient	$R_{th\,JA}$	–	77	K/W

Characteristics

V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Characteristics						
Quiescent current Supply voltage	I_S I_S	– –	2 35	4 50	mA mA	$V_F < V_{FL}$ $V_I = V_I > V_{IH}$, $V_F > V_{FH}$
Supply overvoltage shutdown threshold	V_{SO}	30	37	42	V	$V_L = 5$ V; $V_O > 4.5$ V
Hysteresis of supply overvoltage shutdown threshold	ΔV_{SO}	4	6	9	V	$V_L = 5$ V; $V_O > 4.5$ V
Open load error threshold voltage	V_Q	5	20	50	mV	$V_L = 5$ V; $V_O > 4.5$ V
Open load error threshold current	I_{QU}	1	–	40	mA	$V_Q = V_{QU}$
Open load error threshold current for both channels active	I_{QU}	–	–	80	mA	$V_{Q1} = V_{Q2} = V_{QU}$

Characteristics (cont'd)

V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Logic

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Control inputs						
H-input voltage threshold	V_{IH}	1.3	1.8	2.1	V	–
L-input voltage threshold	V_{IL}	0.9	1.2	1.5	V	–
Hysteresis of control input voltage	ΔV_I	0.2	0.6	1.0	V	–
Enable input						
H-input voltage threshold	V_{FH}	1.6	2.1	2.7	V	–
L-input voltage threshold	V_{FL}	1.4	1.8	2.3	V	–
Hysteresis of enable input voltage	ΔV_F	0.1	0.3	0.7	V	–
H-input current	I_{IH}	0	–	10	µA	V_I = 5 V
L-input current	$-I_{IL}$	0	–	10	µA	V_I = 0.5 V

Status Output (open collector)

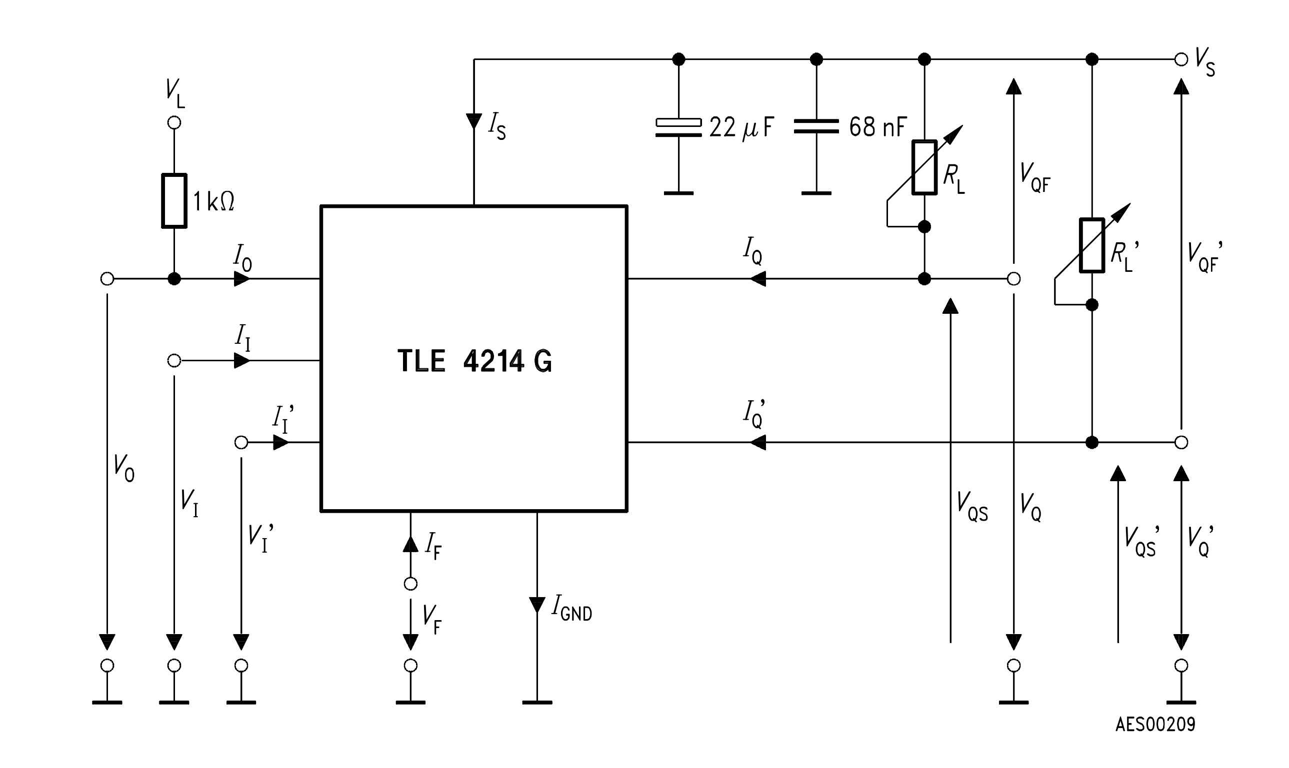
Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
L-saturation voltage	V_{osat}	0.1	0.2	0.4	V	I_O = 5 mA
Status delay time	t_{dS}	8	20	32	µs	[1]

[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50 % value of the status switching edge is reached.

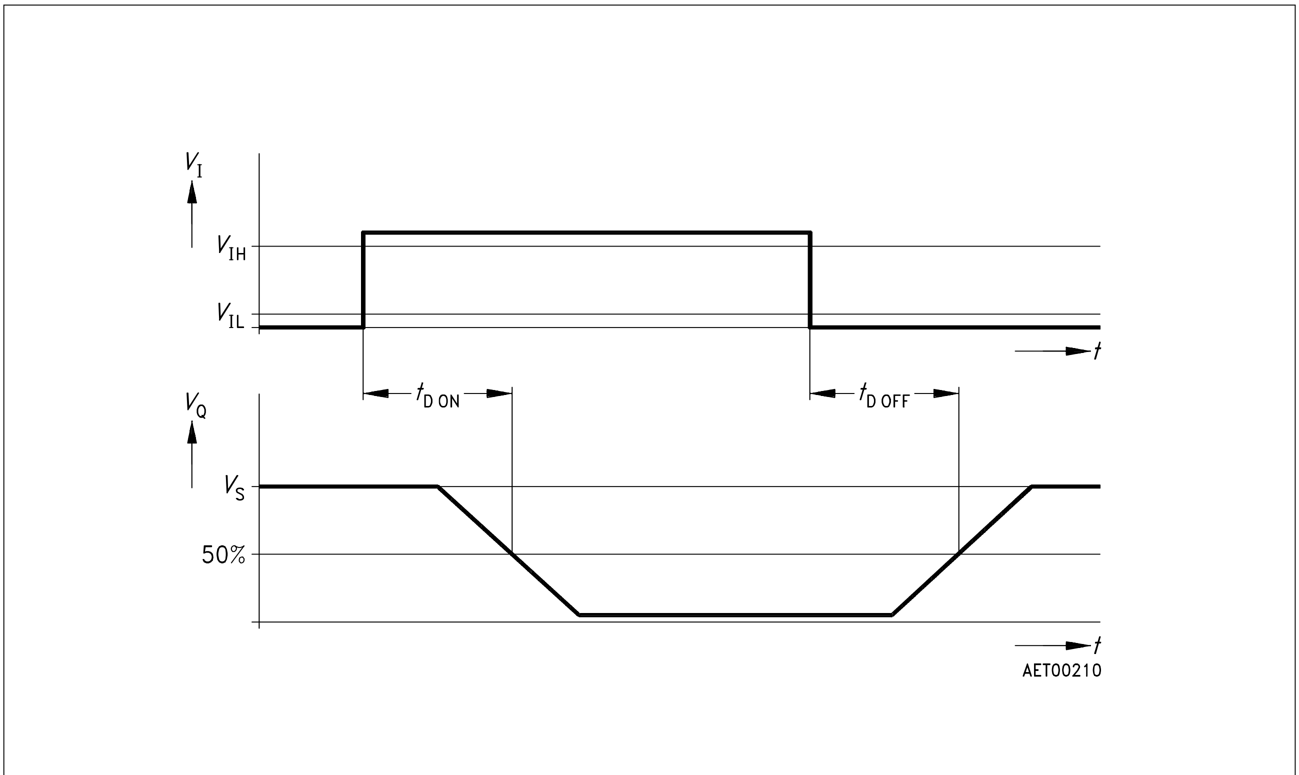
Characteristics (cont'd)

V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

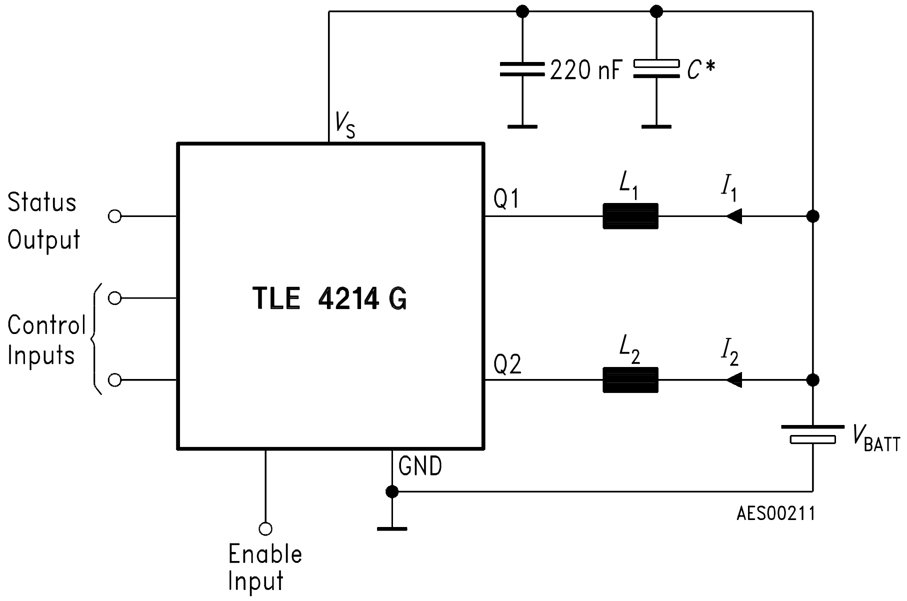
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching Stages						
Saturation voltage	V_{QSat}	–	0.6	0.8	V	I_Q = 0.5 A; $V_I > V_{IH}$; $V_F > V_{FH}$
Saturation voltage	V_{QSat}	–	45	100	mV	I_Q = 50 mA; $V_I > V_{IH}$; $V_F > V_{FH}$
Output current	I_Q	0.5	–		A	V_{QSat} = 0.8 V; $V_I > V_{IH}$
Leakage current	I_Q	– 5	–	50	µA	V_Q = 6 V; $V_I < V_{IL}$
Switch-ON time	$t_{D\ ON}$	0.2	0.5	5	µs	I_Q = 0.5 A **see Timing**
Switch-OFF time	$t_{D\ OFF}$	0.2	2	5	µs	I_Q = 0.5 A **Diagram**
Forward voltage of substrate diode	V_{QS}	–	1.3	1.7	V	I_Q = – 0.5 A; t < 0.1 s
Forward voltage of clamp diode	V_{QF}	–	1.3	1.7	V	I_Q = 0.5 A; t < 0.1 s
Leakage current of clamp diode	$-I_{QF}$	–	–	5	µA	V_Q = 0 V; $V_I < V_{IL}$



Test Circuit



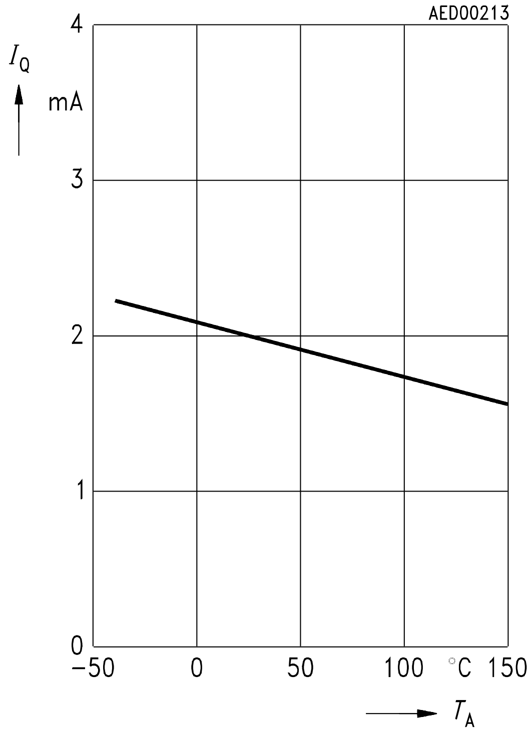
Timing Diagram



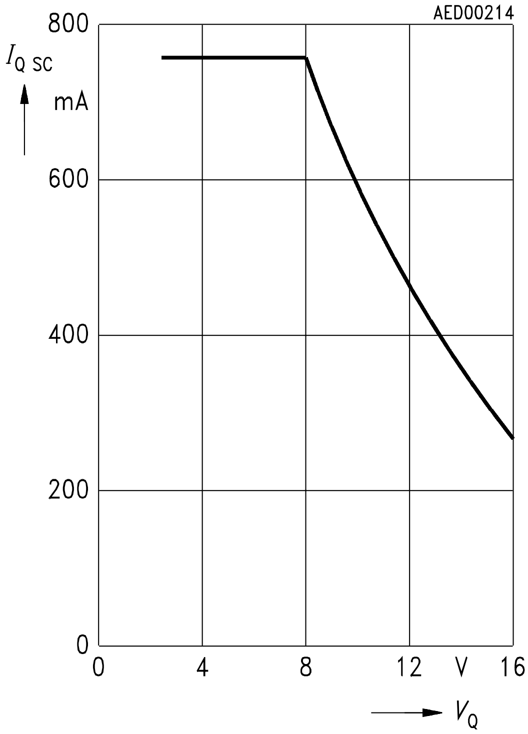
$$C* \geqq (L_1 I_1^2 + L_2 I_2^2) / (70\,\mathrm{V} - V_{BATT})^2$$

Application Circuit

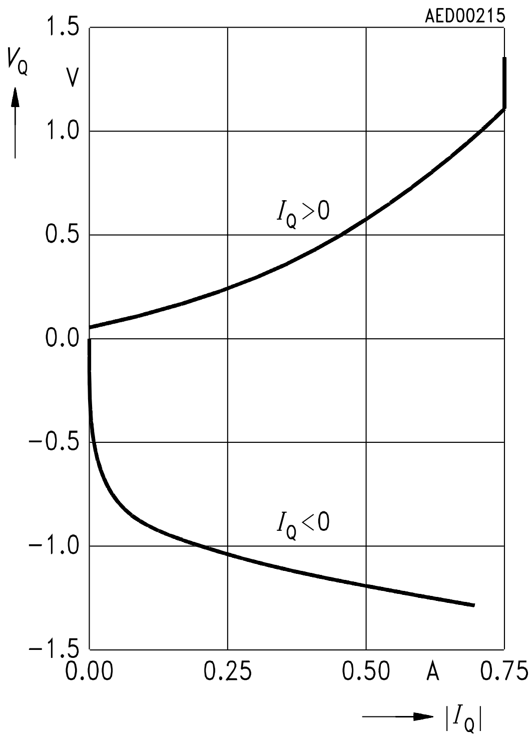
Quiescent Current I_S versus Ambient Temperature T_A in the OFF-Status
V_S = 12 V; V_F < V_{FL}



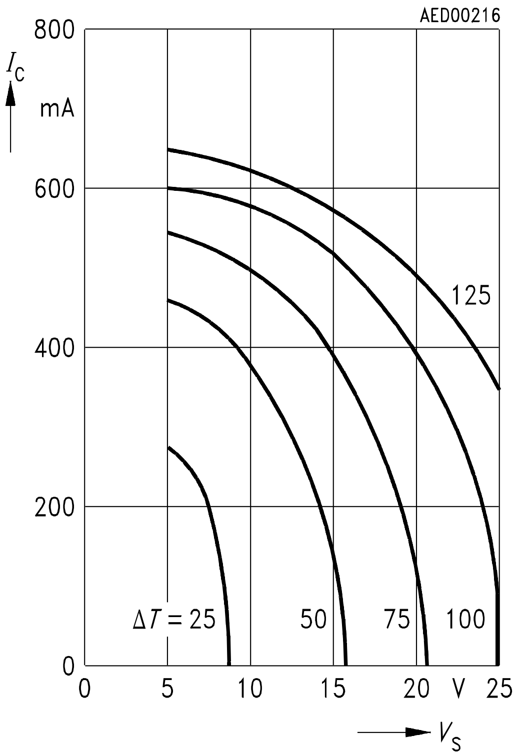
Shorted Load Current I_{Q0} versus Output Voltage V_Q



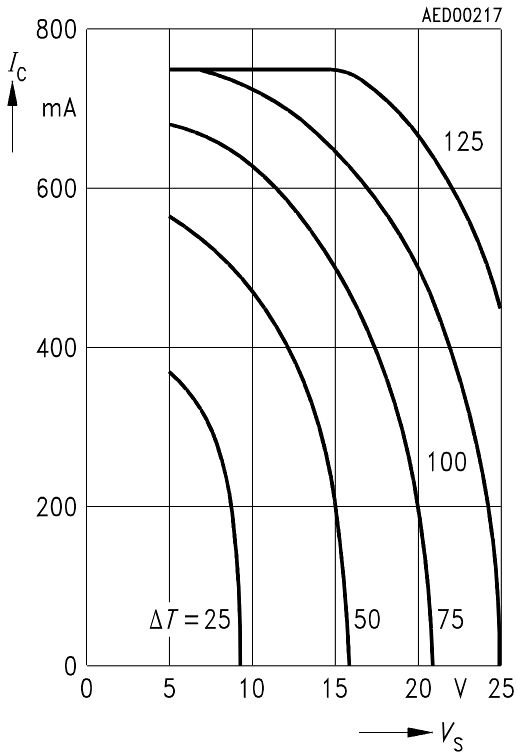
Output Voltage V_Q versus Output Current V_S = 12 V; V_I > V_{IH}



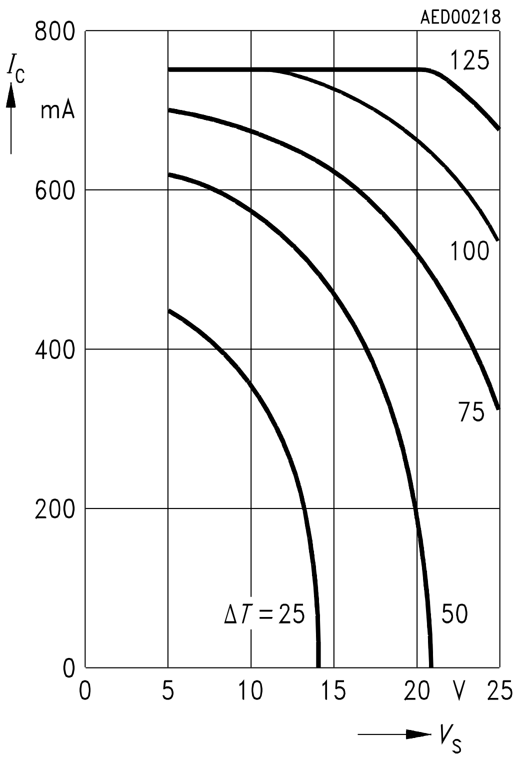
Equal current at both channels



First channel 50 mA, second channel I_Q

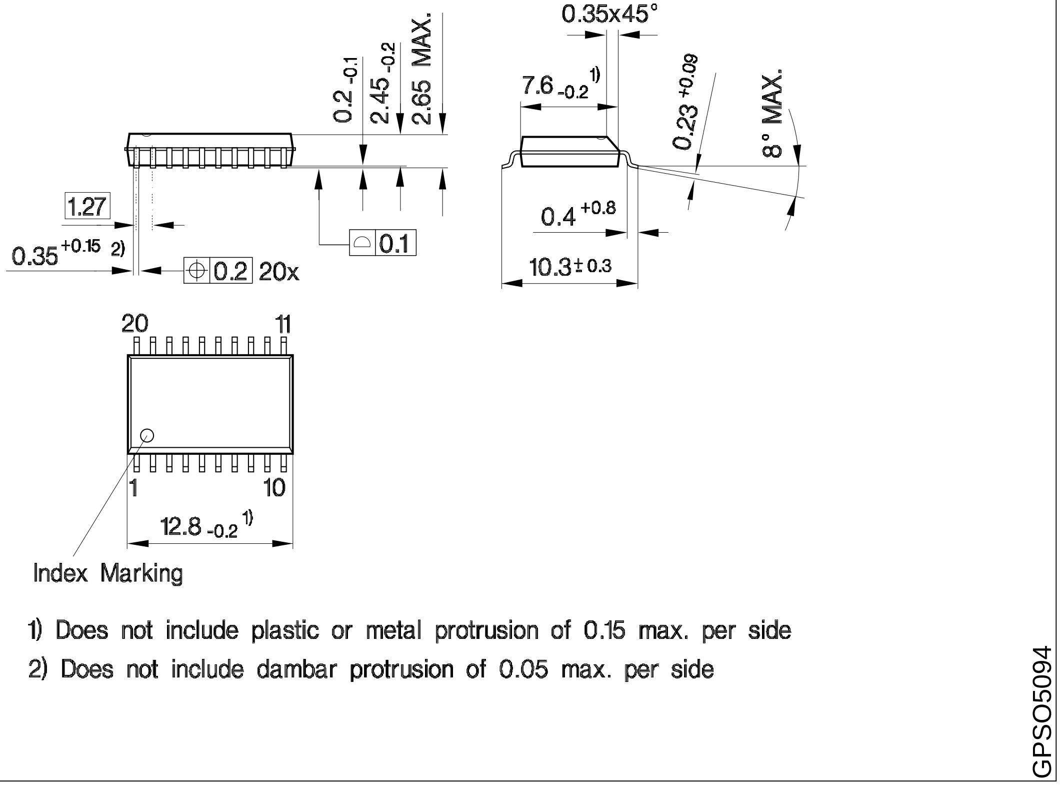


Only one channel in operation



Package Outlines

P-DSO-20-7
(Plastic Dual Small Outline Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm