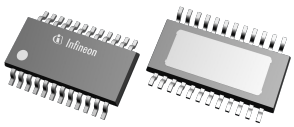
Features

- Dual channel device
- Wide input voltage (up to 58 V) and output voltage range (up to 70 V)
- Switching frequency range from 100 kHz to 500 kHz and 2.2 MHz
- EMC optimized device
- Analog output adjustment (analog dimming)
- Overvoltage, Short to ground, open feedback and overtemperature diagnostic output
- NMOS gate driver for adaptive output discharge
- LED current accuracy ±3.5% (no analog dimming applied)



AEC Qualified

RoHS

RoHS

AEC Qualified

ISO 26262 compliant

Potential applications

- LED driver for: front light module, animated light functions, pixelated adaptive driving beam

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

TLD6099-2ES is a dual channel multi-topology DC-DC controller designed for LED applications with built-in protection features to implement a compact LED driver.

The output current generated by the two channels are independent and they are regulated by means of a peak current control loop. An internal slope compensation is used to avoid sub-harmonic oscillation at high duty cycle (e.g. higher than 50%).

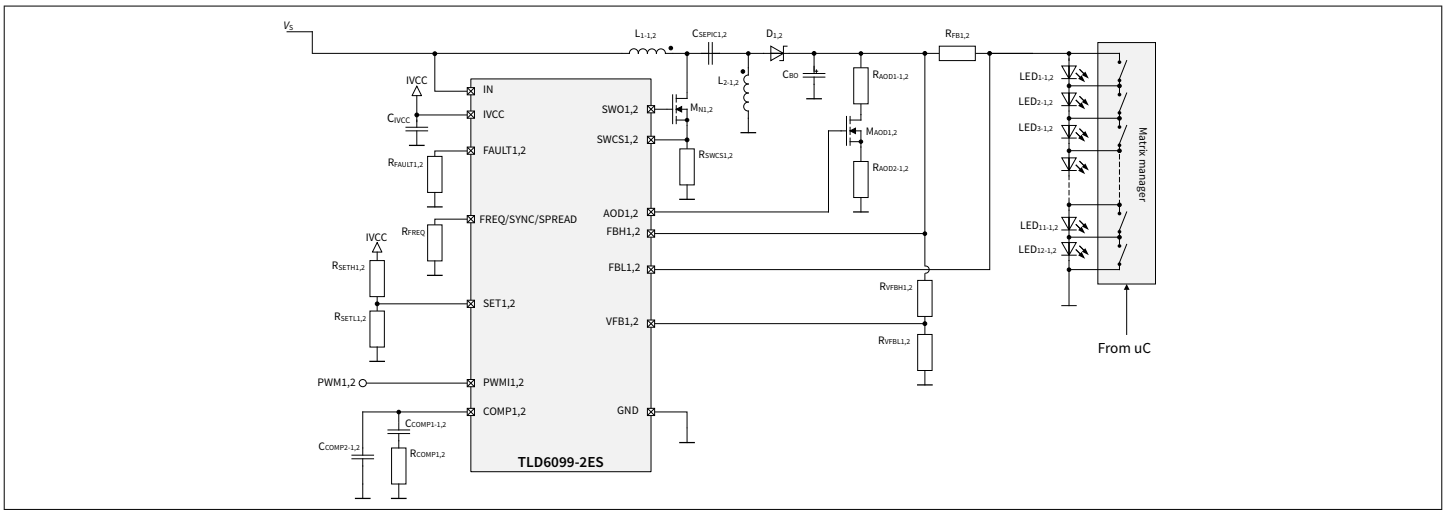
The current accuracy is better than 3.5% (with no analog dimming applied) over the operating temperature range. The current sense amplifiers provide flexibility on the topology choice needed to supply LED strings with more than 20 white LEDs (up to 70 V at output).

The switching frequency can be adjusted from 100 kHz to 500 kHz or fixed to 2.2 MHz by using an external resistor. A synchronization with an external clock is also possible. The device incorporates even a spread spectrum modulator to achieve easy fulfilment of electromagnetic emission standards.

Each channel of TLD6099-2ES can drive an external NMOS to discharge the output capacitance fast. This feature helps to manage fast load variations due to light function exchange scenario. Typical user cases are switching from low beam to high beam or driving adaptive driving beam with matrix manager.

Each channel features two dimming sources:

- The analog output adjustment reduces the output current by adjusting the reference voltage
- The digital dimming reduces the LED brightness by modulating the output current



Product type	Package	Marking
TLD6099-2ES	TSDSO-24	TLD6099

Table of contents

1 Block diagram

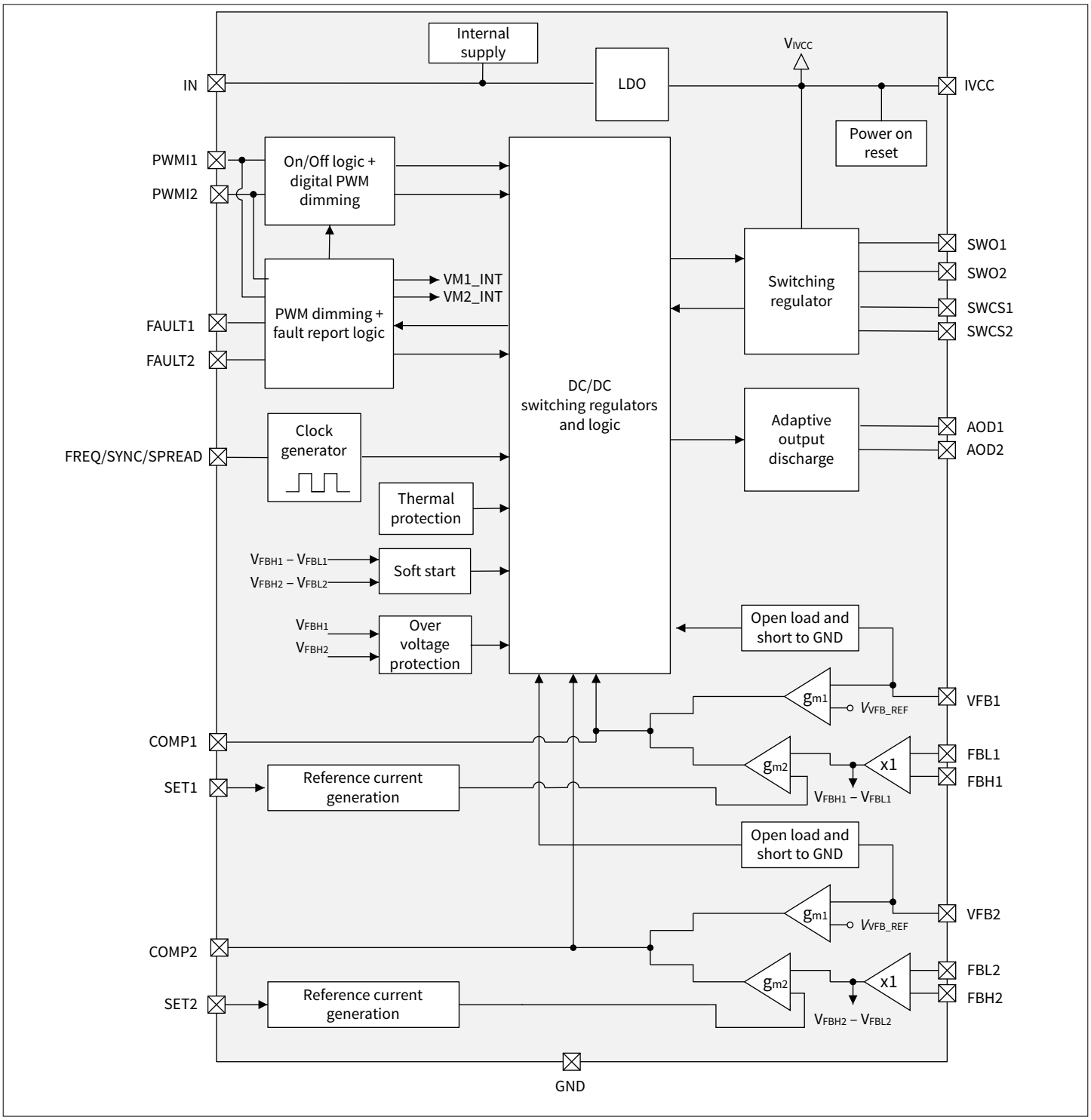


Figure 1 Block diagram

2 Pin configuration

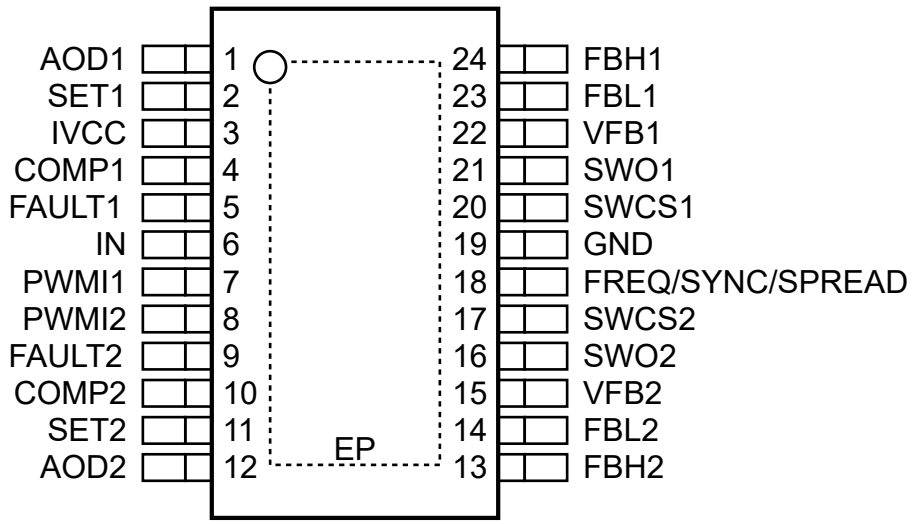


Figure 2 PG-TSDSO-24

Table 1 Pin configuration of PG-TSDSO-24

Name	Pos.	Description	Direction
AOD1	1	**NMOS driver for adaptive output discharge** *Channel 1* Connect to gate of external MOSFET Pin must be left open if external MOSFET is not used	Output
SET1	2	**Analog output adjustment** *Channel 1* Load current adjustment pin Pin must not be left open If analog adjustment is not used, connect to IVCC pin	Input
IVCC	3	**Internal linear voltage regulator** Used for internal biasing and gate drive Bypass with external capacitor Pin must not be left open	Output
COMP1	4	**Compensation** *Channel 1* Connect R and C network for stability	Input

(table continues...)

Table 1 (continued) Pin configuration of PG-TSDSO-24

Name	Pos.	Description	Direction
FAULT1	5	**Fault** *Channel 1* Faults are reported by raising the voltage on this pin Pin must not be left open Connect a pull-down resistor	Output
IN	6	**Supply** Supply for internal biasing	Input
PWMI1	7	**PWM adjustment** *Channel 1* Digital input for PWM dimming Pin must not be left open Connect a pull-down resistor or to IVCC	Input
PWMI2	8	**PWM adjustment** *Channel 2* Digital input for PWM dimming Pin must not be left open Connect a pull-down resistor or to IVCC	Input
FAULT2	9	**Fault** *Channel 2* Faults are reported by raising the voltage on this pin Pin must not be left open Connect a pull-down resistor	Output
COMP2	10	**Compensation** *Channel 2* Connect R and C network for stability	Input
SET2	11	**Analog output adjustment** *Channel 2* Load current adjustment pin Pin must not be left open If analog adjustment is not used, connect to IVCC pin	Input
AOD2	12	**NMOS driver for adaptive output discharge** *Channel 2* Connect to gate of external MOSFET Pin must be left open if external MOSFET is not used	Output
FBH2	13	**Voltage feedback positive** *Channel 2* Non inverting input (+)	Input

(table continues...)

Table 1 (continued) Pin configuration of PG-TSDSO-24

Name	Pos.	Description	Direction
FBL2	14	**Voltage feedback negative** *Channel 2* Inverting input (-)	Input
VFB2	15	**Voltage loop reference** *Channel 2* Connect to resistive voltage divider to set the maximum voltage at output and the short to ground threshold	Input
SWO2	16	**Switch gate driver** *Channel 2* Connect to gate of external switching power n-channel MOSFET	Output
SWCS2	17	**Current sense/Power ground** *Channel 2* Detects peak current through power switch Power ground for gate driver of SWO2	Input
FREQ/SYNC/ SPREAD	18	**Frequency select or synchronization** Connect external resistor to GND to set switching frequency Apply square waveform for synchronization	Input
GND	19	**Ground**	–
SWCS1	20	**Current sense/Power ground** *Channel 1* Detects peak current through power switch Power ground for gate driver of SWO1	Input
SWO1	21	**Switch gate driver** *Channel 1* Connect to gate of external switching power n-channel MOSFET	Output
VFB1	22	**Voltage loop reference** *Channel 1* Connect to resistive voltage divider to set the maximum voltage at output and the short to ground threshold	Input
FBL1	23	**Voltage feedback negative** *Channel 1* Inverting input (-)	Input
FBH1	24	**Voltage feedback positive** *Channel 1* Non inverting input (+)	Input
Exposed pad	EP	**Exposed pad** Used only for heat dissipation Connect to pin 19 (GND)	–

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply input voltage	V_{IN}	-0.3	–	60	V	1)	PRQ-89
Voltage at pin SET1, SET2	$V_{SET1,2}$	-0.3	–	5.5	V	1)	PRQ-92
Voltage at pin PWMI1, PWMI2	$V_{DC/PWMI1,2}$	-0.3	–	60	V	1)	PRQ-95
Voltage at pin FBH1, FBH2	$V_{FBH1,2}$	-1	–	75	V	1)	PRQ-97
Voltage at pin FBL1, FBL2	$V_{FBL1,2}$	-1	–	75	V	1)	PRQ-99
Differential input voltage	$V_{REF1,2(MAX)}$	-75	–	75	V	1) $V_{REF1,2(MAX)} = V_{FBH1,2} - V_{FBL1,2}$ Differential signal (not referred to ground)	PRQ-101
Current at pin FBH1, FBH2, FBL1, FBL2	$I_{FBH1,2}$ $I_{FBL1,2}$	-7.5	–	7.5	mA	1) $V_{REF1,2}$ =150 mV	PRQ-103
Voltage at pin VFB1, VFB2	$V_{FB1,2}$	-0.3	–	5.5	V	1)	PRQ-106
Voltage at pin SWCS1, SWCS2	$V_{SWCS1,2}$	-0.3	–	0.3	V	1)	PRQ-109
Voltage at pin SWO1, SWO2	$V_{SWO1,2}$	-0.3	–	5.5	V	1)	PRQ-111
Voltage at pin FAULT1	V_{FAULT1}	-0.3	–	5.5	V	1)	PRQ-113
Voltage at pin FAULT2	V_{FAULT2}	-0.3	–	5.5	V	1)	PRQ-115
Voltage at pin COMP1, COMP2	$V_{COMP1,2}$	-0.3	–	5.5	V	1)	PRQ-118
Voltage at pin FREQ/ SYNC/SPREAD	$V_{FREQ/SYNC}$	-0.3	–	5.5	V	1)	PRQ-119
Voltage at pin AOD1, AOD2	$V_{AOD1,2}$	-0.3	–	5.5	V	1)	PRQ-122

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltage at pin IVCC	V_{IVCC}	-0.3	–	5.5	V	1)	PRQ-125
Temperature							
Junction temperature	T_J	-40	–	150	°C	1)	PRQ-126
Storage temperature	T_{stg}	-40	–	150	°C	1)	PRQ-127
ESD susceptibility							
ESD susceptibility	V_{ESD_HBM}	-2	–	2	kV	1) HBM: ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-128
ESD susceptibility inner pins	V_{ESD_CDM}	-0.5	–	0.5	kV	1) CDM: ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011	PRQ-129
ESD susceptibility corner pins	$V_{ESD\_CDM\_CR}$	-0.75	–	0.75	kV	1) CDM: ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011	PRQ-130

1) Not subject to production test, specified by design

***Notes**:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for repetitive operation*

3.2 Functional range

Table 3 Functional range

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Extended power supply input voltage range	V_{IN_EXT}	4.5	–	58	V	1) Parameter deviations possible	PRQ-131
Power supply input voltage operating range	V_{IN_OP}	8	–	36	V	–	PRQ-132
Operating voltage at pin FBH1, FBH2	$V_{FBH1,2\_OP}$	2.7	-	70	V	–	PRQ-135
Operating voltage at pin FBL1, FBL2	$V_{FBL1,2\_OP}$	2.55	–	70	V	–	PRQ-136
Switching frequency adjustment range	f_{SWO}	100	–	500	kHz	–	PRQ-137
Synchronization low frequency capture range	$f_{FREQ/SYNC/SPREAD(LF)}$	100	–	500	kHz	–	PRQ-138
Synchronization high frequency capture range	$f_{FREQ/SYNC/SPREAD(HF)}$	2	–	2.4	MHz	–	PRQ-139

1) Not subject to production test, specified by design

***Note**: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table*

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	22.3	–	K/W	1) 2)	PRQ-143
Junction to ambient	R_{thJA}	–	52.7	–	K/W	1) 3) 2s2p	PRQ-145
Junction to ambient	R_{thJA}	–	71.2	–	K/W	1) 3) 1s0p + 600 mm^2	PRQ-147

(table continues...)

Table 4 (continued) Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to ambient	R_{thJA}	–	80.4	–	K/W	1) 3) 1s0p + 300 mm^2	PRQ-149

1) Not subject to production test, specified by design
2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and exposed pads are fixed to ambient temperature) T_A = 25°C dissipates 1 W
3) Specified R_{thJA} value is according JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board. The device was simulated on 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layer (2 x 35 µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the top layer and the inner layers to bottom layers of JEDEC PCB. T_A = 25°C; IC dissipates 1 W

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For further information visit* https://www.jedec.org

4 Switching regulator

The TLD6099-2ES implements a dual channel controller suitable for Boost-to-ground, Boost-to-battery, Buck-to-battery, SEPIC and Flyback configurations. The two channels work independently.

Each channel has two distinct control loops:

- A current control loop
- A voltage control loop

Each channel regulates the output current as long as the feedback voltage on VFB1,2 pin is below the VFB1,2 voltage mode ON threshold ($V_{VFB1,2\_VM(ON)}$). The voltage control loop takes over and regulates the output voltage once the VFB1,2 reference voltage ($V_{VFB1,2\_REF}$) is reached.

The controller generates two independent PWM signals by sensing the inductor peak currents and the output of the internal error amplifiers. The control signals are applied to the internal gate drivers connected to SWO1,2 pin to drive the external n-channel MOSFETs.

4.1 Soft start

The soft start routine has 2 functionalities:

- Limiting the input current and output overshoot
- Guaranteeing that the system output reaches the target value in a reasonable time even when being operated in PWM dimming with low duty cycles

Each channel performs its own soft start routine independently.

The first rising edge on PWMI1,2 pin enables the soft start routine.

It is then performed in the following cases:

- At start-up
- After an overvoltage on FBH1,2 pin
- After an overtemperature fault
- After an undervoltage on IVCC pin

The soft start is applied after a short to ground fault and retriggered every t_{FAULT} in case of continuous presence of the fault.

The operation of the soft start is conditioned by the analog output adjustment.

During the soft start, the switching regulator adjusts the PWM signal to make the voltage between FBH1,2 and FBL1,2 evolve from 0 to $V_{REF(100\%)}$ in t_{SS} time. The evolution is performed in 15 steps if the analog adjustment is not applied, otherwise the intended steady-state is reached before the soft start ends.

An ON time extension of the PWM dimming pulses is applied to ensure a reasonable power-up time when a low duty cycle dimming is applied.

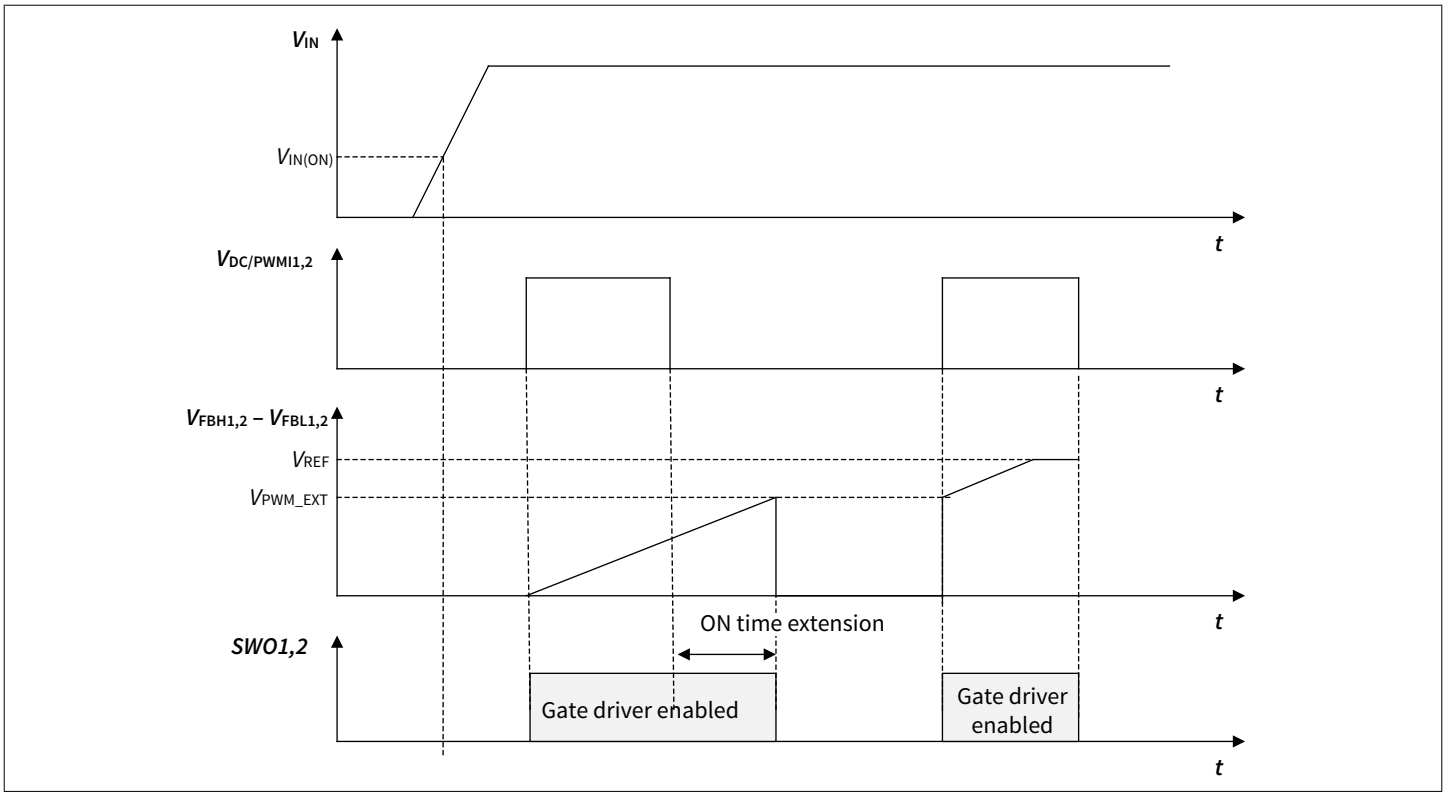


Figure 3 Soft start timing diagram (the linear waveform of V_{VFBH}-V_{VFBL} is an example of possible scenario)

The ON time extension is triggered if :

- The applied PWM dimming signal has an ON time shorter than t_{SS} during the soft start

and

- The voltage across FBH1,2 and FBL1,2 is lower than the reference voltage during PWM extension V_{PWM_EXT} at the end of the ON time of the PWM signal

The ON time extension persists as long as the voltage across FBH1,2 and FBL1,2 reaches V_{PWM_EXT}.

The V_{PWM_EXT} is limited by the analog output adjustment down to a minimum reference voltage during ON time extension V_{PWM_MIN}.

For the first 3 steps of the V_{REF} signal, the V_{PWM_EXT} is higher than V_{REF}.

If the reference voltage across FBH1,2 and FBL1,2 adjusted by analog adjustment feature is lower than the V_{PWM_MIN} the ON time extension ends after t_{SS}.

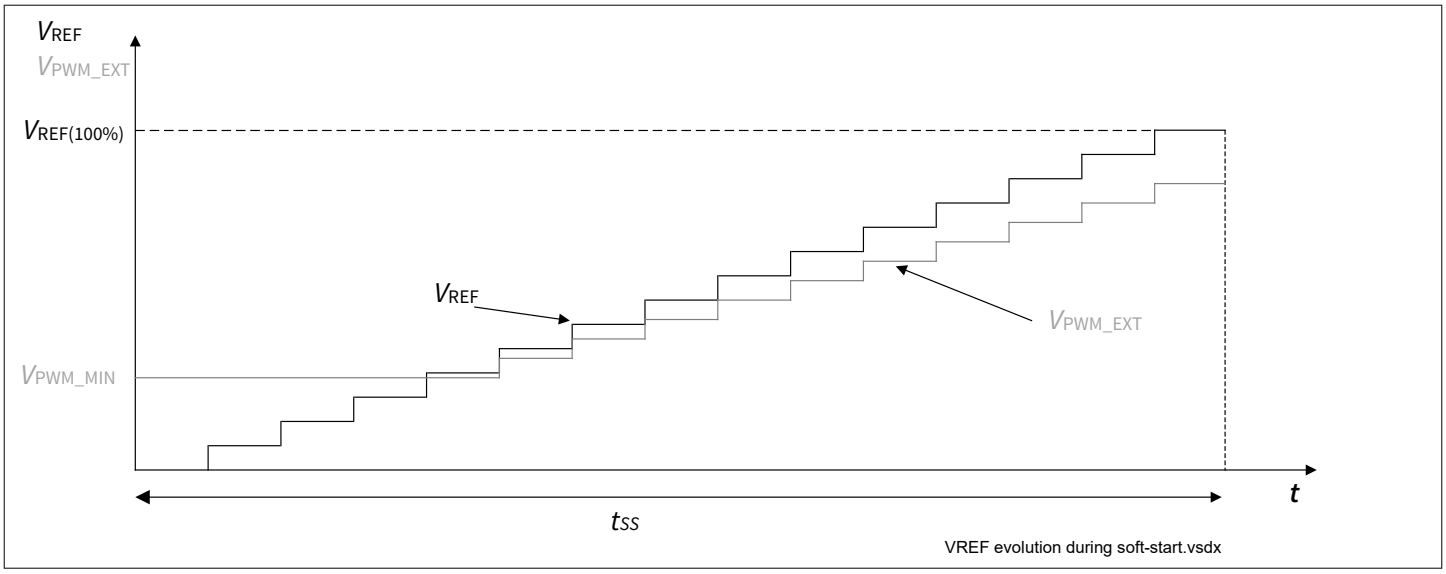


Figure 4 **V_{REF} and V_{PWM_EXT} waveforms during the soft start routine without analog output adjustment**

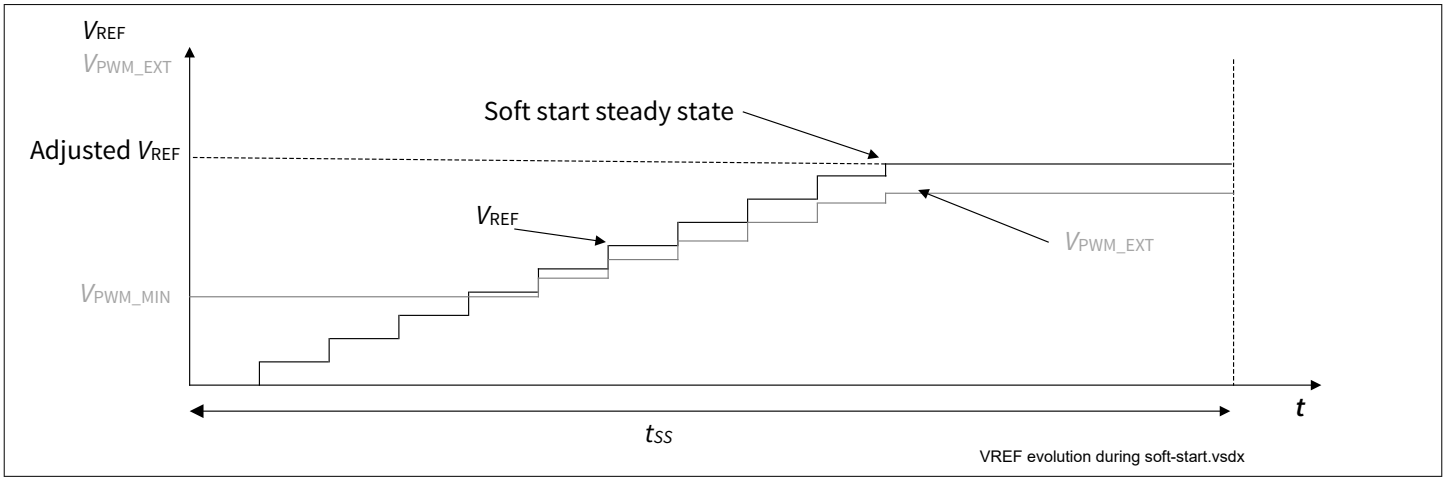


Figure 5 **V_{REF} and V_{PWM_EXT} waveforms during the soft start routine with analog output adjustment**

If the ON time extension ends before t_{SS} elapsed, the ON time extension is retriggered in the following PWM cycle, in case the voltage between FBH1,2 and FBL1,2 is once again lower than V_{PWM_EXT}.

When the ON time extension ends, the remaining part of the soft start is allowed to evolve during the following ON time of the PWM dimming signal. In this case the actual duration of soft start could be longer than t_{SS}.

4.2 Electrical characteristics

Table 5 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Regulator							
VFB1,2 reference voltages (voltage loop)	$V_{VFB1,2\_REF}$	1.568	1.6	1.632	V	–	PRQ-172
Current loop reference voltages	$V_{REF1,2(100\%)}$	144.75	150	155.25	mV	Differential signal (not referred to ground) $V_{REF1,2} = V_{FBH1,2} - V_{FBL1,2}$; $V_{SET1,2}$ = 5V	PRQ-174
Current loop reference voltages	$V_{REF1,2(40\%)}$	57	60	63	mV	Differential signal (not referred to ground) $V_{SET1,2}$ = 940 mV	PRQ-176
Current loop reference voltages	$V_{REF1,2(0\%)}$	–	–	10	mV	Differential signal (not referred to ground) $V_{SET1,2}$ = 100 mV	PRQ-178
Transconductance error amplifier voltage loop	g_{m1}	–	0.95	–	mS	1)	PRQ-179
Transconductance error amplifier current loop	g_{m2}	–	1.6	–	mS	1)	PRQ-180
Switch current limit thresholds	$V_{SWCS1,2\_TH}$	80	100	120	mV	–	PRQ-182
Maximum duty cycle in adjust. freq. mode	D_{MAX}	91	–	–	%	$R_{FREQ/SYNC/SPREAD}$ = 27 kΩ	PRQ-183
Maximum duty cycle in low frequency sync mode	$D_{MAX(LF)}$	88	–	–	%	f_{SW} = 500 kHz	PRQ-184
Maximum duty cycle in high frequency sync mode	$D_{MAX(HF)}$	85	–	–	%	f_{SW} = 2.2 MHz	PRQ-185
Soft start time	t_{SS}	1.8	2	2.2	ms	1)	PRQ-186
Reference voltage during PWM extension	V_{PWM_EXT}	–	0.8* $V_{REF1,2}$	–	V	1) $V_{PWM\_EXT} > V_{PWM\_MIN}$	PRQ-187
Minimum reference voltage during PWM extension	V_{PWM_MIN}	–	31.5	–	mV	1)	PRQ-188
Input current at pin FBH1, FBH2	$I_{FBH1,2}$	–	120	160	µA	$V_{FBH1,2} - V_{FBL1,2}$ = 0.15 V $V_{FBH1,2}$ = 60 V	PRQ-194

(table continues...)

Table 5 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Input current at FBL1, FBL2	$I_{FBL1,2}$	–	50	70	µA	$V_{FBH1,2}$ - $V_{FBL1,2}$ = 0.15 V $V_{FBL1,2}$ = 60 V	PRQ-196
Power supply undervoltage shutdown	$V_{IN(OFF)}$	2.5	–	4.5	V	V_{IN} decreasing	PRQ-201
Power supply minimum startup voltage	$V_{IN(ON)}$	–	–	5.5	V	V_{IN} increasing	PRQ-202
Power supply current consumption	I_{IN}	–	8	12	mA	$V_{PWMI1,2}$ = 0 V $V_{SET1,2}$ = V_{IVCC} $R_{FREQ/SYNC/SPREAD}$ = 33 kΩ $R_{FAULT1,2}$ = 57 kΩ no faults detected	PRQ-204
Gate driver for external switch							
Gate drivers peak output current	$I_{SWO1,2}$	1	–	–	A	1) $V_{SWO1,2}$ increasing 1 V to 4 V Current flows out of pin	PRQ-206
Gate drivers peak output current	$I_{SWO1,2}$	1	–	–	A	1) $V_{SWO1,2}$ decreasing 4 V to 1 V	PRQ-208
Gate drivers output rise time	$t_{R\_SWO1,2}$	–	–	20	ns	1) $C_{L\_SWO1,2}$ = 3.3 nF $V_{SWO1,2}$ increasing 1 V to 4 V	PRQ-210
Gate drivers output fall time	$t_{F\_SWO1,2}$	–	–	20	ns	1) $C_{L\_SWO1,2}$ = 3.3 nF $V_{SWO1,2}$ decreasing 4 V to 1 V	PRQ-212
Gate driver high side resistance	R_{SWO_HS}	–	1	3	Ω	1) I_{SWO} = -10 mA	PRQ-213
Gate driver low side resistance	R_{SWO_LS}	–	1	3	Ω	1) I_{SWO} = 10 mA	PRQ-214

1) Not subject to production test, specified by design

5 Linear regulator

The device incorporates a linear regulator to generate a 5 V output used to supply the internal gate drivers and, through IVCC pin, other auxiliary devices on the PCB (for example a microcontroller and resistor dividers).

The maximum output current of the linear regulator is limited to the IVCC output current limit I_{IVCC}.

If the load on IVCC (gate drivers plus connected devices on PCB) draws more than I_{IVCC} the linear regulator output voltage decreases.

The linear regulator starts to deliver current to IVCC pin when the input voltage V_{IN} goes above the power supply minimum start up voltage $V_{IN\ (ON)}$ for a time longer than IVCC start time t_{ST}.

A low ESR capacitor has to be connected from IVCC to ground (C_{IVCC} in the figure) to stabilize the output voltage of the linear regulator.

The ESR of the capacitor C_{IVCC} has to be lower than IVCC buffer capacitor ESR $R_{IVCC(ESR)}$.

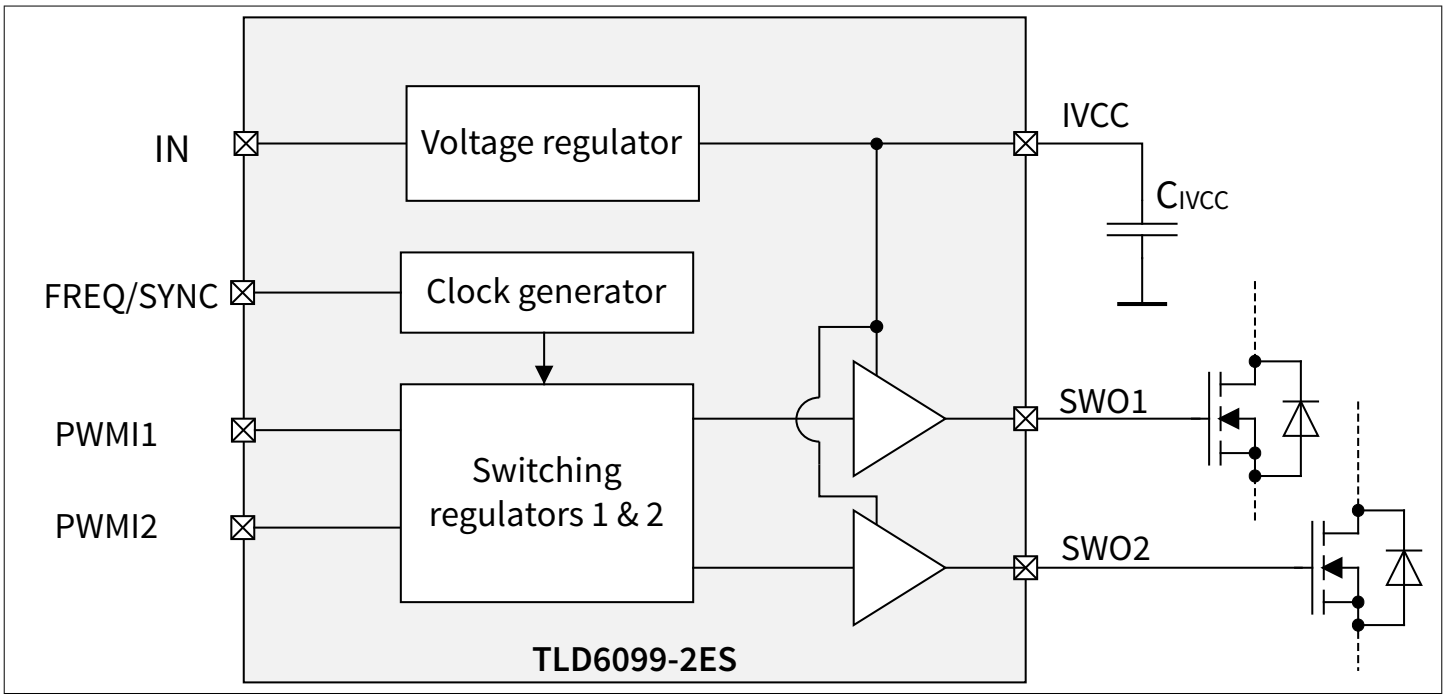


Figure 6 Block diagram of the linear regulator

5.1 Undervoltage protection for the external switching MOSFET

During the ON time of the switching PWM signal, the gate driver has to bias the switching NMOS in deep ohmic region to avoid the overheating of the MOSFET themselves. This is ensured by choosing a logic level MOSFET with a maximum threshold voltage lower than IVCC undervoltage switch-off threshold $V_{IVCC\_TH\_D}$.

TLD6099-2ES has an integrated undervoltage reset threshold circuit to disable the gate driver if the V_{IVCC} drops below the $V_{IVCC\_TH\_D}$. The gate driver are then enabled again when the V_{IVCC} goes above the IVCC undervoltage switch-on threshold $V_{IVCC\_TH\_I}$.

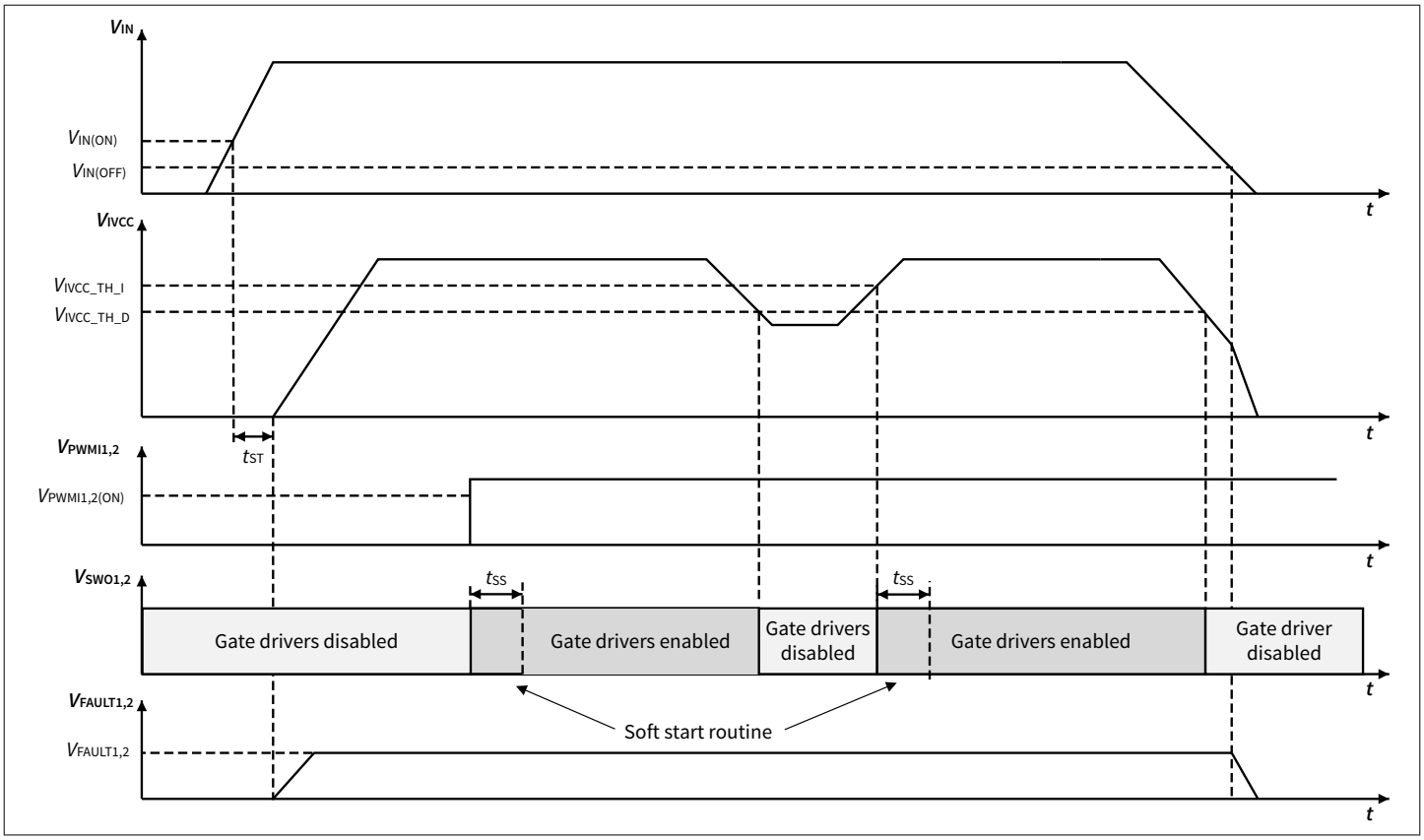


Figure 7 Thresholds and timing diagram related to the linear regulator

5.2 Electrical characteristics

Table 6 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IVCC output voltage	V_{IVCC}	4.85	5	5.15	V	8 V ≤ V_{IN} ≤ 36 V; 0.1 mA ≤ I_{IVCC} ≤ 40 mA	PRQ-222
IVCC output current limit	I_{IVCC}	51	–	100	mA	8 V < V_{IN} < 13.5 V; V_{IVCC} < 4.5 V; Current flows out of pin	PRQ-223
IVCC dropout voltage	V_{IVCC_DV}	–	–	0.5	V	V_{IN} = 5 V; I_{IVCC} < 20 mA	PRQ-224
IVCC start time	t_{ST}	–	–	300	µs	1) V_{IN} slew rate higher than 1 V/10 µs	PRQ-225
IVCC buffer capacitor	C_{IVCC}	1	4.7	10	µF	1)	PRQ-226
IVCC buffer capacitor ESR	$R_{IVCC(ESR)}$	–	–	0.2	Ω	1) Maximum value given for regulator stability	PRQ-227

(table continues...)

Table 6 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IVCC undervoltage switch-off threshold	$V_{IVCC\_TH\_D}$	3.6	–	4.0	V	V_{IVCC} decreasing	PRQ-228
IVCC undervoltage switch-on threshold	$V_{IVCC\_TH\_I}$	–	–	4.5	V	V_{IVCC} increasing	PRQ-229

1) Not subject to production test, specified by design

***Note**: Select external switching MOSFET with worst case threshold voltage $V_{GS(th)}$ lower than minimum $V_{IVCC\_TH\_D}$*

6 Switching frequency setup and synchronization

The DC-DC switching frequency is adjusted by a resistor placed from FREQ/SYNC/SPREAD pin to ground or by providing a digital clock to this pin. The device incorporates also a spread spectrum modulator to reduce the design effort to fulfill the EMI compliance.

If an external clock is provided, the device accepts a digital clock in these two working windows:

- Synchronization low frequency capture range $f_{FREQ/SYNC/SPREAD(LF)}$ (low frequency synchronization mode)
- Synchronization high frequency capture range $f_{FREQ/SYNC/SPREAD(HF)}$ (high frequency synchronization mode)

Outside these ranges, the device does not recognize a valid clock and then the behavior of the regulator can be out of specification.

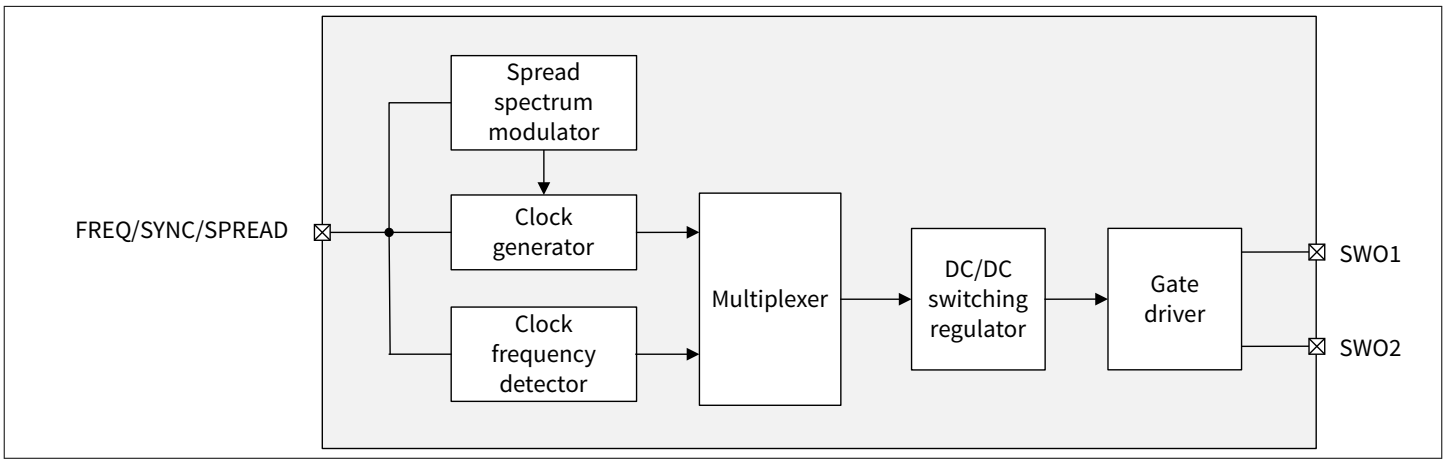


Figure 8 Diagram of switching frequency adjustment and synchronization blocks

To limit the input current spikes and then to relax the input filter requirements, SWO2 is in phase opposition to SWO1. This means SWO2 is activated with a $1/(2*f_{SWO})$ delay respect to SWO1.

6.1 Switching frequency setup with external resistor

The resistor placed on FREQ/SYNC/SPREAD pin adjusts the frequency of the DC-DC and enables or disables the spread spectrum modulator.

The resistor placed between FREQ/SYNC/SPREAD pin and ground adjusts switching frequency of the regulator as follows:

- If the bias resistor is in the $R_{FREQ\_SpreadSpectrum(ON)}$ range the spread spectrum is activated and the switching frequency is adjusted in f_{SWO} range
- If the bias resistor is in the $R_{FREQ\_SpreadSpectrum(OFF)}$ range the spread spectrum is deactivated and the switching frequency is adjusted in f_{SWO} range
- If the resistor is below $R_{FREQ\_HF(ON)}$ the spread spectrum is deactivated and the switching frequency is fixed at f_{SWO_HS}

Values out of these resistor sets are not allowed.

The relationship between the biasing resistor and switching frequency with spread spectrum activated is

$$f_{SW} = \frac{1}{\left(1.11 \cdot 10^{-9} \cdot R_{FREQ/SYNC/SPREAD}\right)} \quad (1)$$

The relationship between the biasing resistor and the switching frequency with the spread spectrum not active is

$$f_{SW} = \frac{1}{\left(1.11 \cdot 10^{-10} \cdot R_{FREQ/SYNC/SPREAD}\right)} \quad (2)$$

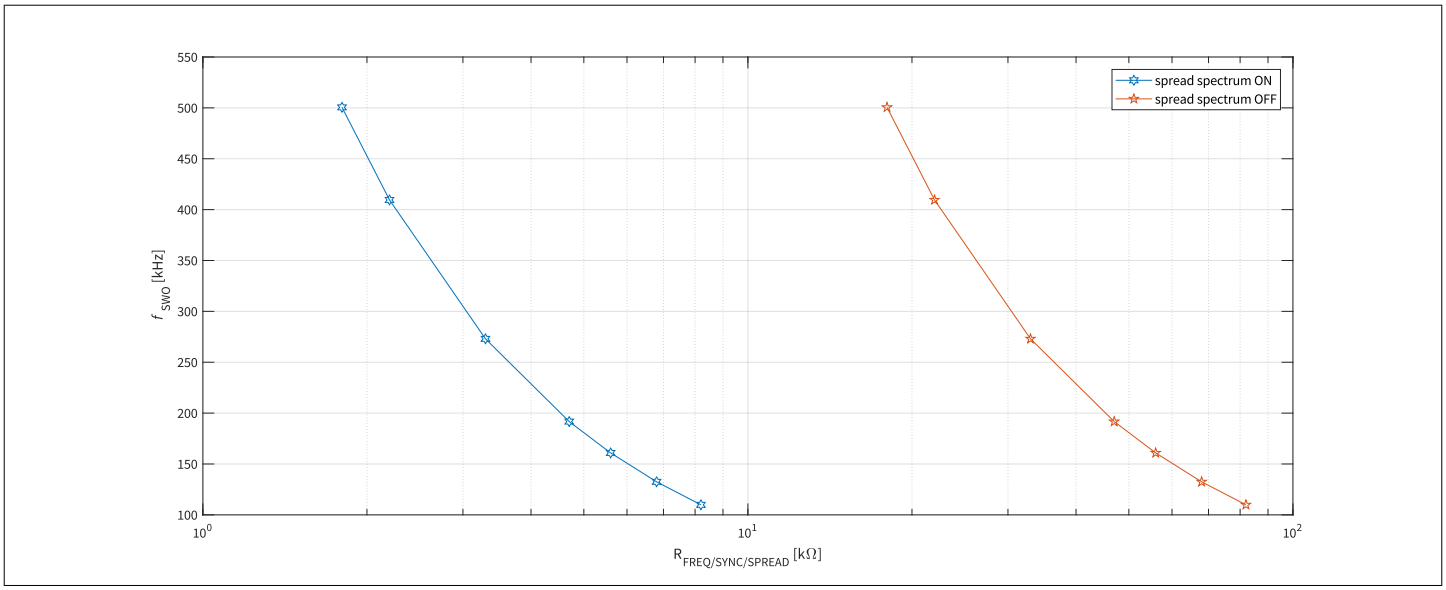


Figure 9 Switching frequency versus $R_{FREQ/SYNC/SPREAD}$

6.1.1 Electrical characteristics

Table 7 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching frequency	$f_{SWO\_SSM(OFF)}$	288	333	378	kHz	$R_{FREQ/SYNC/SPREAD}$ = 27 kΩ	PRQ-238
Switching frequency	f_{SWO_HF}	2	2.2	2.4	MHz	$R_{FREQ/SYNC/SPREAD}$ = 100Ω	PRQ-446
FREQ/SYNC/SPREAD output current	$I_{FREQ/SYNC/SPREAD}$	–	–	3	mA	$V_{FREQ/SYNC/SPREAD}$ = 0 V Current flowing out of pin	PRQ-239
FREQ/SYNC/SPREAD output voltage	$V_{FREQ/SYNC/SPREAD\_SSM(OFF)}$	0.72	0.8	0.88	V	$R_{FREQ/SYNC/SPREAD}$ = 27 kΩ	PRQ-240
Biasing resistor FREQ/SYNC/SPREAD spread spectrum ON	$R_{FREQ\_SpreadSpectrum(ON)}$	1.8	–	9	kΩ	–	PRQ-443
Biasing resistor FREQ/SYNC/SPREAD spread spectrum OFF	$R_{FREQ\_SpreadSpectrum(OFF)}$	18	–	90	kΩ	–	PRQ-444
Biasing resistor FREQ/SYNC/SPREAD/ high frequency	$R_{FREQ\_HF(ON)}$	–	–	100	Ω	–	PRQ-445

6.1.2 Spread Spectrum

The spread spectrum modulation technique significantly reduces the electromagnetic harmonics emission at the lower frequency range of the spectrum (f < 30 MHz).

This technique is enabled by changing the switching frequency over the time. The final result is the movement over a broad band of the energy associated with the peaks of the electromagnetic harmonics emission.

The switching frequency is modulated with a triangular shape digitalized in 7 steps equally distributed over the entire frequency span (2 times the frequency deviation f_{DEV}).

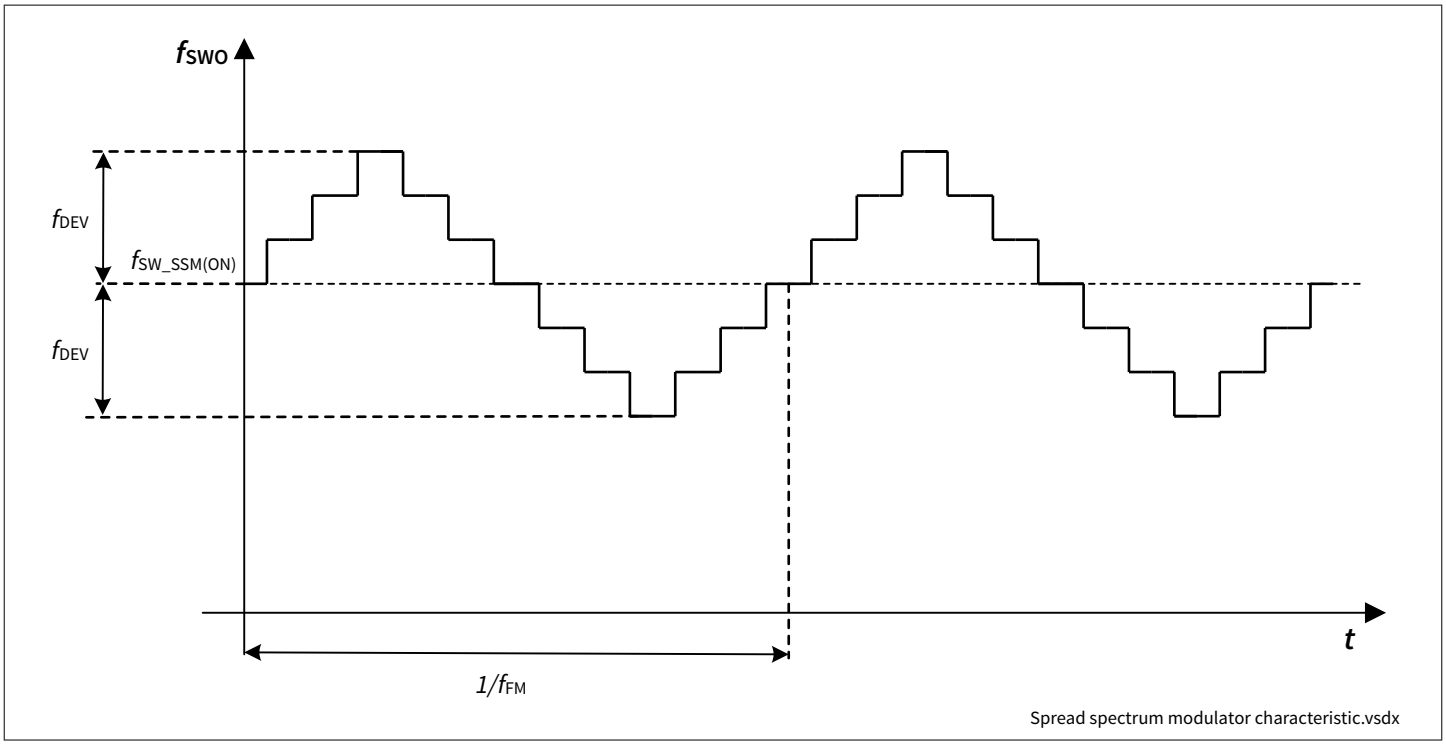


Figure 10 Spread spectrum modulator characteristic

6.1.2.1 Electrical characteristics

Table 8 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Average switching frequency	$f_{SWO\_SSM(ON)}$	288	333	378	kHz	1) $R_{FREQ/SYNC/SPREAD}$ = 2.7 kΩ	PRQ-243
Modulation frequency	f_{FM}	6.75	7.5	8.25	kHz	1) 1.8 kΩ ≤ $R_{FREQ/SYNC/SPREAD}$ ≤ 9 kΩ	PRQ-244
Frequency deviation	f_{DEV}	0.08* f_{SWO}	0.10* f_{SWO}	–	kHz	1) 1.8 kΩ ≤ $R_{FREQ/SYNC/SPREAD}$ ≤ 9 kΩ	PRQ-245

(table continues...)

Table 8 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
FREQ/SYNC/SPREAD output voltage	$V_{FREQ/SYNC/SPREAD\_SSM(ON)}$	0.72	0.8	0.88	V	$R_{FREQ/SYNC/SPREAD}$ = 2.7 kΩ	PRQ-246

1) Not subject to production test, specified by design

6.2 Synchronization with external clock (low frequency mode)

The switching frequency is synchronized with an external clock source applied on FREQ/SYNC/SPREAD pin if the frequency is in the synchronization low frequency capture range $f_{FREQ/SYNC/SPREAD(LF)}$ and the duty cycle is in the synchronization input duty cycle range $DC_{FREQ/SYNC/SPREAD}$.

The device detects the external clock source if the voltage on FREQ/SYNC/SPREAD exceeds the two thresholds:

- The synchronization input high voltage $V_{FREQ/SYNC/SPREAD(H)}$ during the positive pulse,
- The synchronization input low voltage $V_{FREQ/SYNC/SPREAD(L)}$ during the negative pulse.

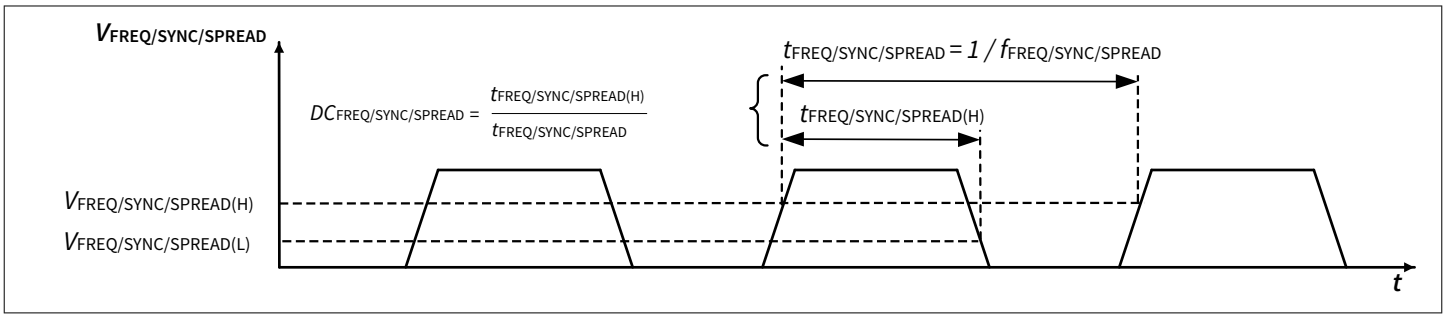


Figure 11 Timing diagram when synchronization mode is enabled

6.2.1 Electrical characteristics

Table 9 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Synchronization input high voltage	$V_{FREQ/SYNC/SPREAD(H)}$	3.0	–	–	V	–	PRQ-250
Synchronization input low voltage	$V_{FREQ/SYNC/SPREAD(L)}$	–	–	0.8	V	–	PRQ-251
Synchronization input duty cycle range	$DC_{FREQ/SYNC/SPREAD}$	40	–	60	%	*1)*	PRQ-252

1) Not subject to production test, specified by design

6.3 Synchronization with external clock (high frequency range)

High switching frequency enables a system cost down due to reduced value for the reactive components.

The high frequency synchronization is enabled if the input clock is in the synchronization high frequency capture range $f_{FREQ/SYNC/SPREAD(HF)}$.

Voltage threshold levels on FREQ/SYNC/SPREAD pin are the same as in the low frequency synchronization mode.

7 Analog output adjustment

Each channel can adjust the reference voltage $V_{REF1,2}$ across FBH1,2 and FBL1,2 pins (thus adjusting the output currents) by monitoring the analog voltage on the respective SET1,2 pin ($V_{SET1,2}$).

The analog output adjustment acts independently channel by channel without any relations between the channels.

The SWO1,2 NMOS gate driver is disabled if the voltage applied on the SET1,2 pin is lower than $V_{SET1,2(NOSW)}$.

The SET1,2 pin is connected to a voltage higher than $V_{SET1,2(100\%)}$ (e.g. connecting SET1,2 pin to IVCC pin) to exclude the output current adjustment feature.

The voltage on SET1,2 pins influences the voltage reference of the corresponding channel following the behavior depicted in the diagram below.

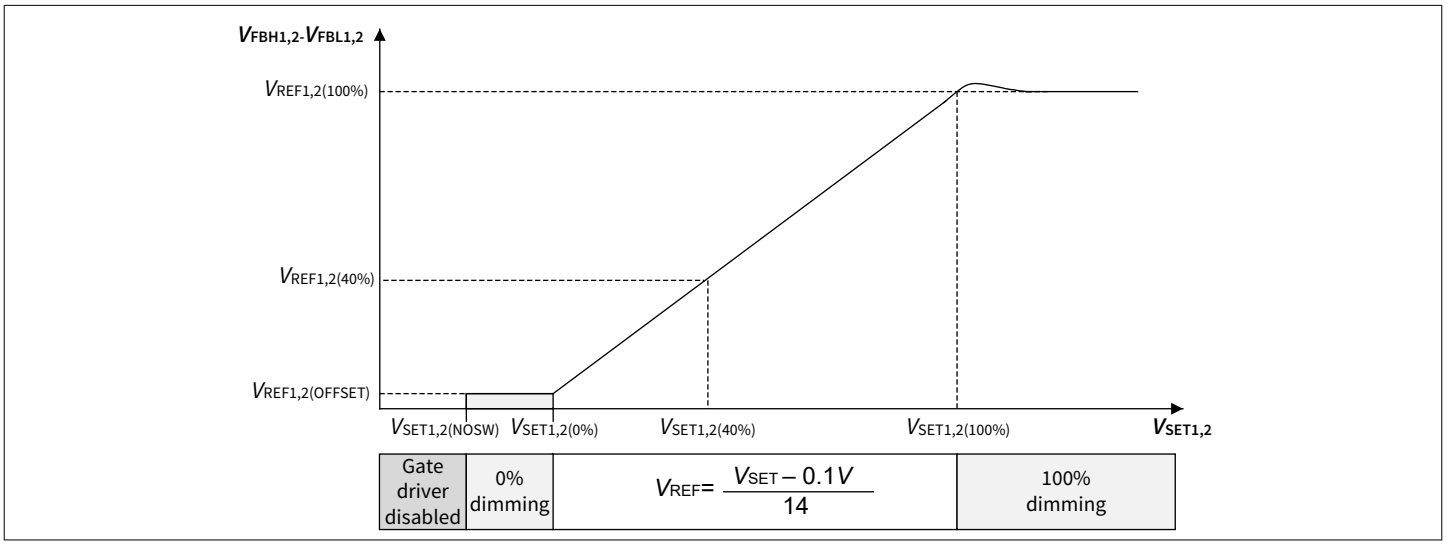


Figure 12 Relationship between $V_{SET1,2}$ and the respective voltage $V_{REF1,2}$

The SET pin can also be wired to an external thermistor (usually mounted on the LED module) to perform a thermal protection.

7.1 Electrical characteristics

Table 10 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SET1 SET2 input voltage 100%	$V_{SET1,2(100\%)}$	–	2.2	–	V	1)	PRQ-260
SET1 SET2 input voltage 40%	$V_{SET1,2(40\%)}$	–	940	–	mV	1)	PRQ-262
SET1 SET2 input voltage 0%	$V_{SET1,2(0\%)}$	–	100	–	mV	1)	PRQ-265
SET1 SET2 input voltage no switching activity	$V_{SET1,2(NOSW)}$	–	–	50	mV	–	PRQ-266

1) Not subject to production test, specified by design

8 Dimming functions

The TLD6099-2ES offers two dimming inputs (one for each channel) for pulse width modulating (PWM) the output current.

This modulation is beneficial to reduce the average current at output (and then the brightness of the LEDs), without showing color shift on the light produced by the LEDs.

This feature is implemented on both channels and it acts independently channel by channel without any relation between channels.

8.1 Digital PWM dimming

Each channel of the TLD6099-2ES has a dedicated input pin to modulate the average current in a LED string with a digital pattern.

Each channel recognizes a digital PWM dimming signal on PWMI1,2 pin if:

- The minimum voltage on PWMI1,2 pin is lower than $V_{PWMI1,2(OFF)}$
- The maximum voltage on PWMI1,2 pin is higher than $V_{PWMI1,2(ON)}$
- The maximum frequency on PWMI1,2 is less than 1 kHz
- No faults are detected

If a valid pattern is recognized and the V_{PWMI} is higher than $V_{PWMI1,2(ON)}$ the NMOS gate driver is enabled, else the NMOS gate driver is disabled. When the NMOS gate driver is disabled the voltage at COMP pin is kept stable.

8.1.1 Electrical characteristics

Table 11 Electrical Characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWMI1, PWMI2 input voltage high threshold	$V_{PWMI1,2(ON)}$	2.0	–	–	V	–	PRQ-290
PWMI1, PWMI2 input voltage low threshold	$V_{PWMI1,2(OFF)}$	–	–	0.8	V	–	PRQ-292
PWMI1 PWMI2 input current	$I_{PWMI1,2}$	–	–	200	µA	$V_{PWMI1,2} = V_{IN}$	PRQ-294
PWMI1 PWMI2 input current	$I_{PWMI1,2}$	–	–	1	µA	$V_{PWMI1,2}$ = 0.8 V	PRQ-296
PWMI1, PWMI2 minimum ON time	$t_{PWMI1,2(ON)}$	6	–	–	µs	–	PRQ-298

9 Adaptive output discharge

Load variation could generate current spikes that reduce the LED reliability. TLD6099-2ES protects the load by enabling the adaptive output discharge (AOD) feature.

The AOD drives a NMOS in parallel to the output capacitance to quickly adjust the output voltage when the load has a reduced number of LEDs in series.

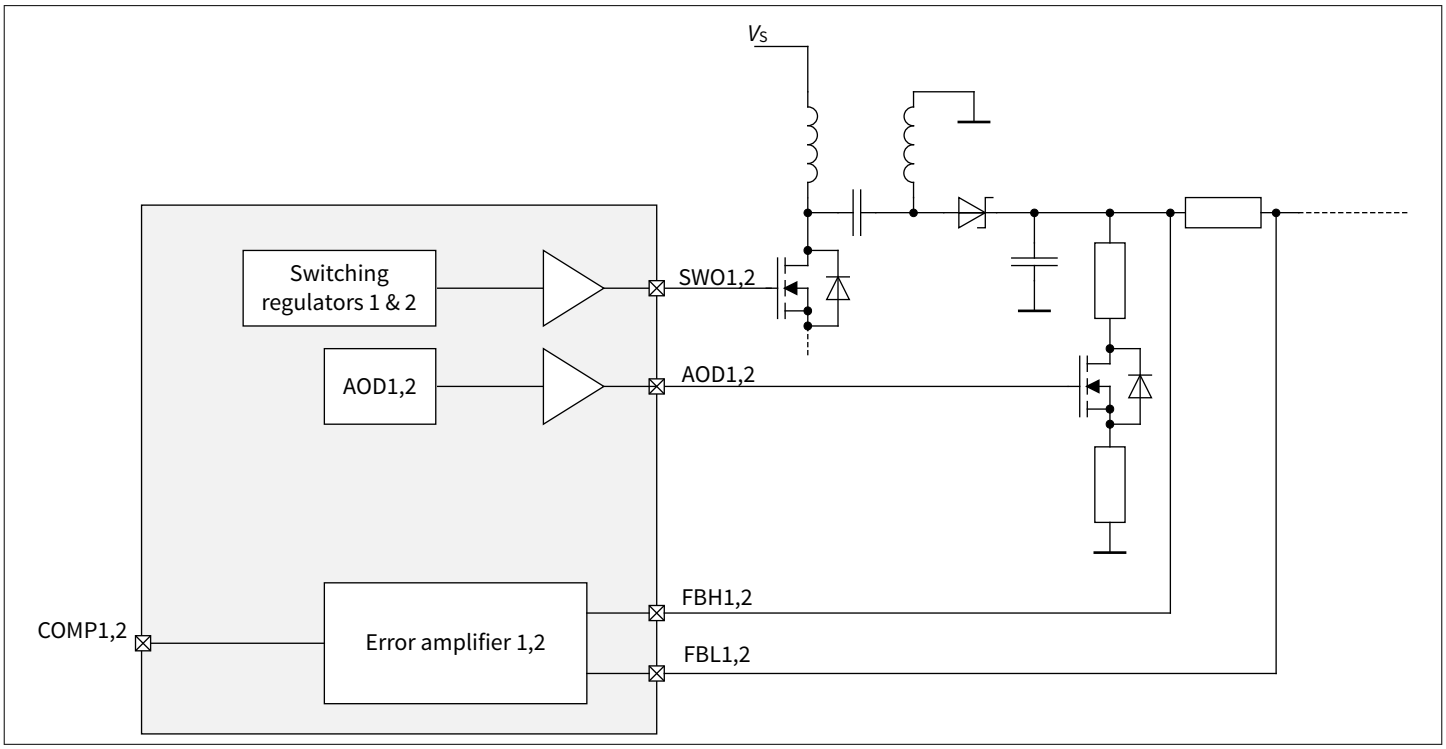


Figure 13 Adaptive output discharge

The adaptive output discharge feature turns ON the external AOD NMOS when the voltage across FBH1,2 and FBL1,2 exceeds $V_{REF1,2}$ by V_{AOD_ON} for a time longer than t_{AOD_ON}.

The external AOD NMOS is turned off when the voltage across FBH1,2 and FBL1,2 goes lower than ($V_{REF1,2}$ + V_{AOD_ON} - V_{AOD_HYS}).

The adaptive output discharge activation threshold is modulated by the analog output adjustment (analog dimming) down to a minimum reference voltage $V_{AOD\_ON(MIN)}$.

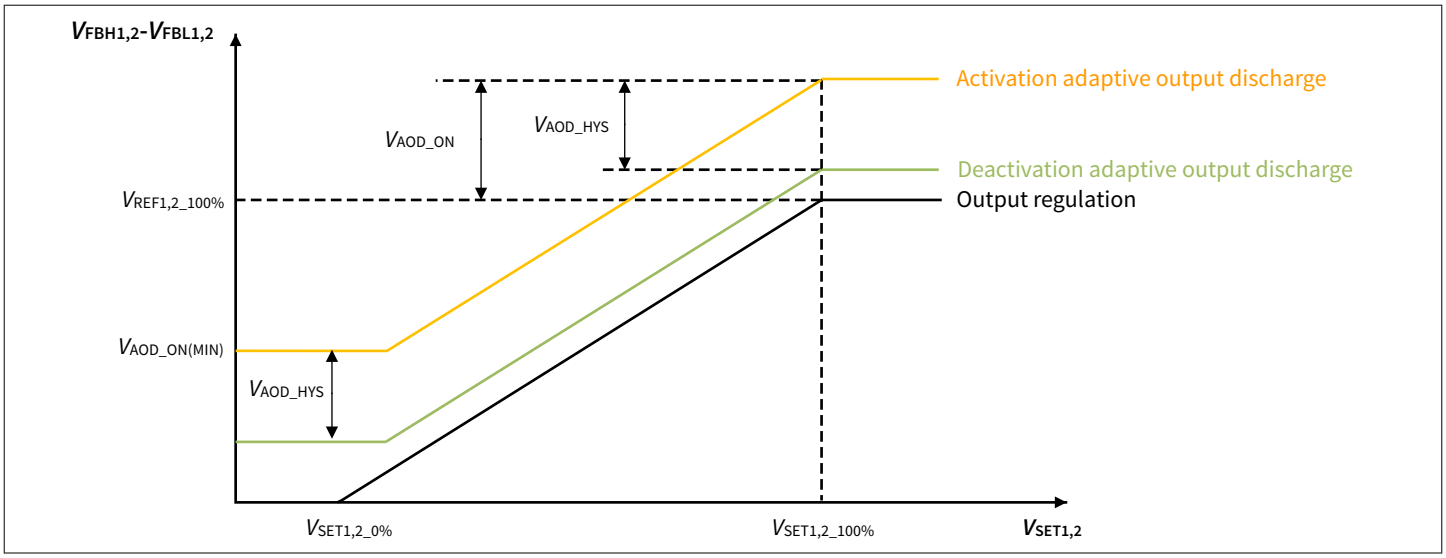


Figure 14 AOD activation as function of V_{SET}

During the soft-start routine the adaptive output discharge feature is enabled.

9.1 Electrical characteristics

Table 12 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Activation adaptive output discharge	V_{AOD_ON}	15	22.5	30	mV	$V_{FBH1,2}$ = 60 V Voltage $V_{FBH1,2}$ - $V_{FBL1,2}$ increasing	PRQ-430
Hysteresis adaptive output discharge	V_{AOD_HYS}	10	15	–	mV	$V_{FBH1,2}$ = 60 V Voltage $V_{FBH1,2}$ - $V_{FBL1,2}$ decreasing	PRQ-431
Activation time	t_{AOD_ON}		–	200	ns	1)	PRQ-432
Minimum activation adaptive output discharge	$V_{AOD\_ON(MIN)}$	50	62.5		mV	1) $V_{FBH1,2}$ = 60 V Voltage $V_{FBH1,2}$ - $V_{FBL1,2}$ increasing	PRQ-436
Gate driver for external switch							
Gate drivers peak output current	$I_{AOD1,2}$	150	–	–	mA	1) *VAOD1,2* increasing 1 V to 4 V Current flows out of pin	PRQ-440
Gate drivers peak output current	$I_{AOD1,2}$	150			mA	1) $V_{AOD1,2}$ decreasing 4 V to 1 V	PRQ-449

(table continues...)

Table 12 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate drivers output rise time	$t_{R\_AOD1,2}$	–	–	100	ns	1) $C_{L\_AOD1,2}$ = 3.3 nF *VAOD1,2* increasing 1 V to 4 V	PRQ-441
Gate drivers output fall time	$t_{F\_AOD1,2}$	–	–	100	ns	1) $C_{L\_AOD1,2}$ = 3.3 nF $V_{AOD1,2}$ decreasing 4 V to 1 V	PRQ-442

1) Not subject to production test, specified by design

10 Protections and fault management

The fault conditions are identified by checking the status of IVCC and FAULT1,2 pins. The faults on the two channels are independently managed and reported.

Each channel of the device disables the gate drivers and reports a fault on its FAULT1,2 pin if it detects:

- Short to ground
- Overtemperature
- Overvoltage on FBH1,2 pin

The faults are reported by raising the voltage on the respective FAULT1,2 pin to $V_{FAULT1,2(FAULT)}$.

The status of FAULT pin can be monitored by a microcontroller. In this case a series resistor $R_{FAULT-uC}$ has to be used between FAULT and the input pin of the microcontroller.

The fault pin is driven by an open drain structure. The maximum output current is $I_{FAULT1,2(HIGH)}$.

10.1 Electrical characteristics

Table 13 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
FAULT1,2 output voltage with fault	$V_{FAULT1,2(HIGH)}$	4	–	–	V	1)	PRQ-336
FAULT1,2 output current with fault	$I_{FAULT1,2(HIGH)}$	–	–	6.5	mA	V_{FAULT} = 0 V Fault detected	PRQ-448
Fault period	t_{FAULT}	9	10	11	ms	1)	PRQ-337
Series resistance on FAULT pin	$R_{FAULT-uC}$	10	—	—	kΩ	1)	PRQ-451

1) Not subject to production test, specify by design

10.2 Short to ground

The short to ground detection feature protects each channel from an excess of current during a short circuit.

Each channel detects this fault if the voltage of VFB1,2 pin is lower than short to ground voltage threshold $V_{FB1,2\_S2G}$ for a time longer than short to ground reaction time t_{S2G_RT}. After a fault time with short to ground t_{S2G} a soft start routine is triggered. The fault is released if the voltage on VFB1,2 pin is higher than ($V_{FB1,2\_S2G}$+$V_{FB1,2\_S2G\_HYST}$) at the end of the soft start.

During soft-start routine, the short to ground detection is disabled and no faults are reported on FAULT1,2 pin.

The reaction to short to ground is:

1. The voltage on FAULT1,2 pin is raised to $V_{FAULT1,2(HIGH)}$ for t_{S2G} time
2. After a t_{S2G} time the soft-start routine is performed
3. At the end of soft-start routine, the check on the voltage $V_{VFB1,2}$ is redone

If the fault is still present, the procedure is repeated, otherwise the channel restarts.

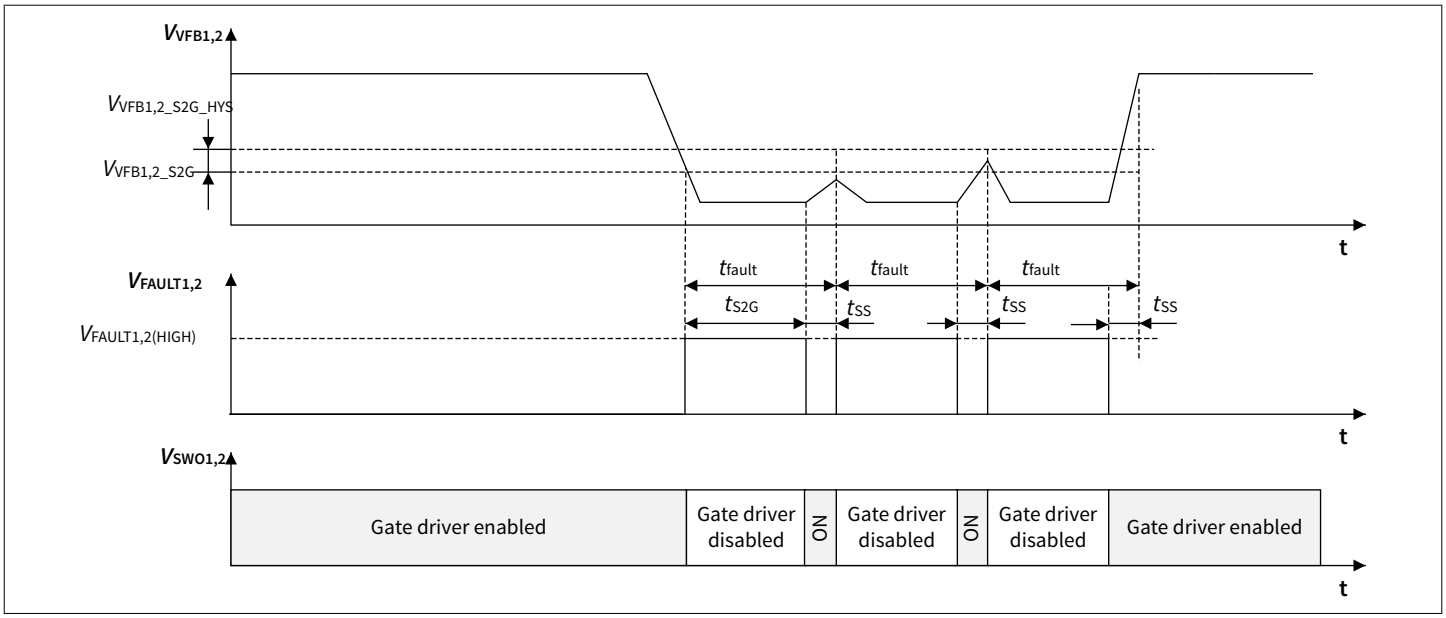


Figure 15 Timing diagram during short to ground detection

The faults are not detected when the voltage on PWMI1,2 pin is lower than $V_{PWMI1,2(OFF)}$.

10.2.1 Electrical characteristics

Table 14 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Fault time with short to ground	t_{S2G}	7.2	8	8.8	ms	1)	PRQ-348
Short to ground reaction time	t_{S2G_RT}	4	–	20	µs	–	PRQ-349
Short to ground voltage threshold	$V_{FB1,2\_S2G}$	93	100	107	mV	Voltage decreasing	PRQ-350
Short to ground voltage hysteresis	$V_{FB1,2\_S2G\_HYST}$	–	5	10	mV	1)	PRQ-351

1) Not subject to production test, specified by design

10.3 Output voltage regulation

Each channel implements an overvoltage protection by regulating the output voltage using the internal voltage loop.

The voltage loop is taking over the regulation when the voltage on VFB1,2 pin goes higher than $V_{FB1,2\_VM(ON)}$. At this time the voltage on FAULT1,2 pin is raised to $V_{FAULT1,2(HIGH)}$.

The channel also reports no faults at FAULT1,2 pin when the voltage on VFB1,2 pin goes below $V_{FB1,2\_VM(OFF)}$ to highlight the voltage loop is ineffective.

The reporting on FAULT1,2 pin is not active if the voltage on PWMI1,2 pin is lower than $V_{PWMI1,2(OFF)}$.

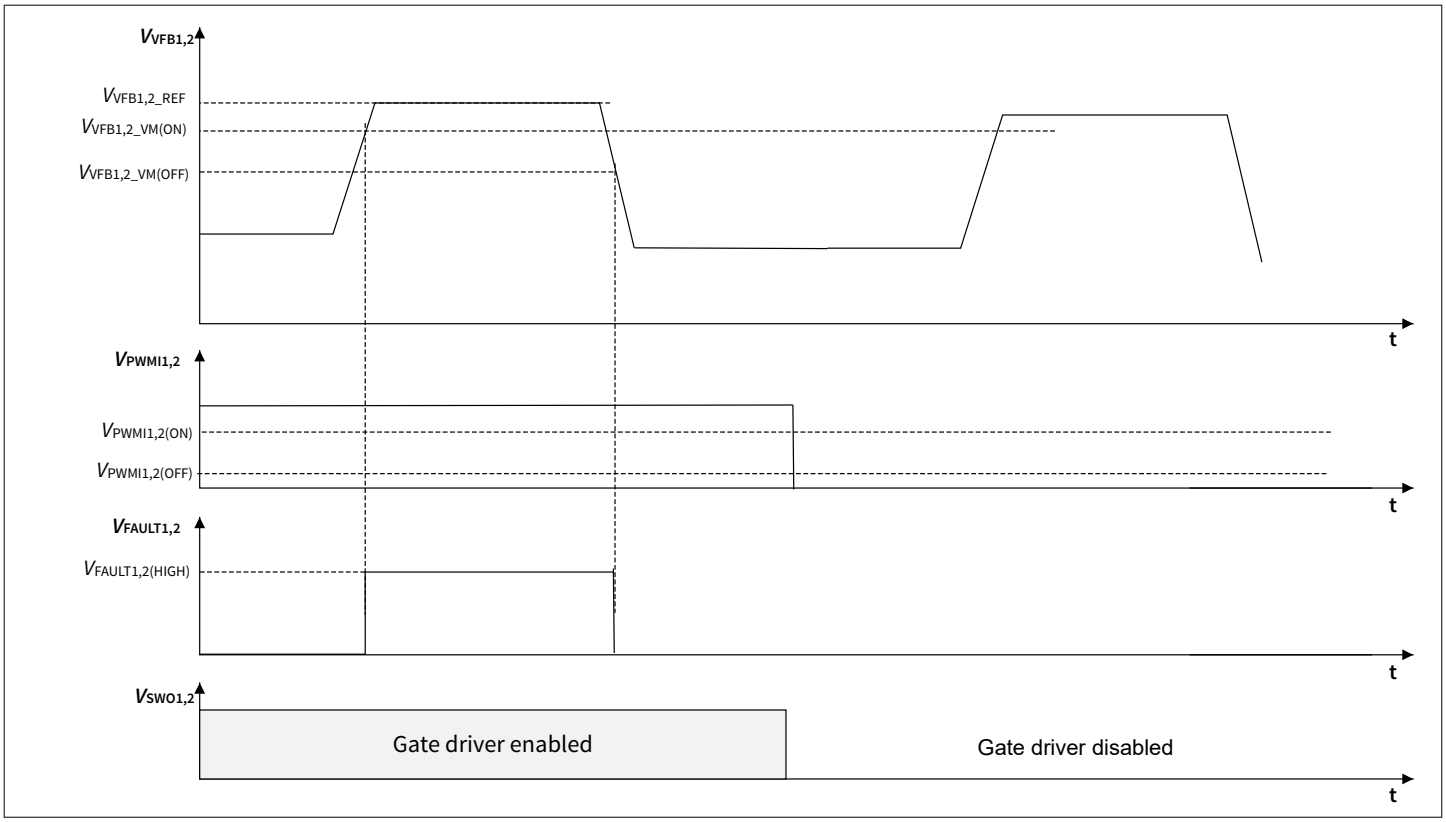


Figure 16 Timing diagram in voltage regulation

10.3.1 Electrical characteristics

Table 15 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VFB1, VFB2 overvoltage threshold	$V_{VFB1,2\_OV}$	1.568	1.6	1.632	V	Voltage increasing	PRQ-361
VFB1, VFB2 input current	$I_{VFB1,2}$	-1	-0.1	1	µA	$V_{FB1,2}$ = 1.6 V	PRQ-363
VFB1, VFB2 voltage mode ON thresholds	$V_{VFB1,2\_VM(ON)}$	1.45	1.5	1.55	V	Voltage increasing	PRQ-366
VFB1, VFB2 voltage mode OFF threshold	$V_{VFB1,2\_VM(OFF)}$	1.3	1.35	1.4	V	Voltage decreasing	PRQ-368

10.4 Overvoltage on FBH pin

The channels have a feature to protect FBH1,2 pin from a voltage higher than the maximum absolute rating.

Each channel reacts to the fault by:

- Disabling the respective SWO NMOS gate driver

- Raising the voltage of respective FAULTn pin to $V_{FAULT1,2(HIGH)}$
- After t_{FAULT} period, the device checks if the voltage on FBH pin is still higher than $V_{FBH1,2(L)}$

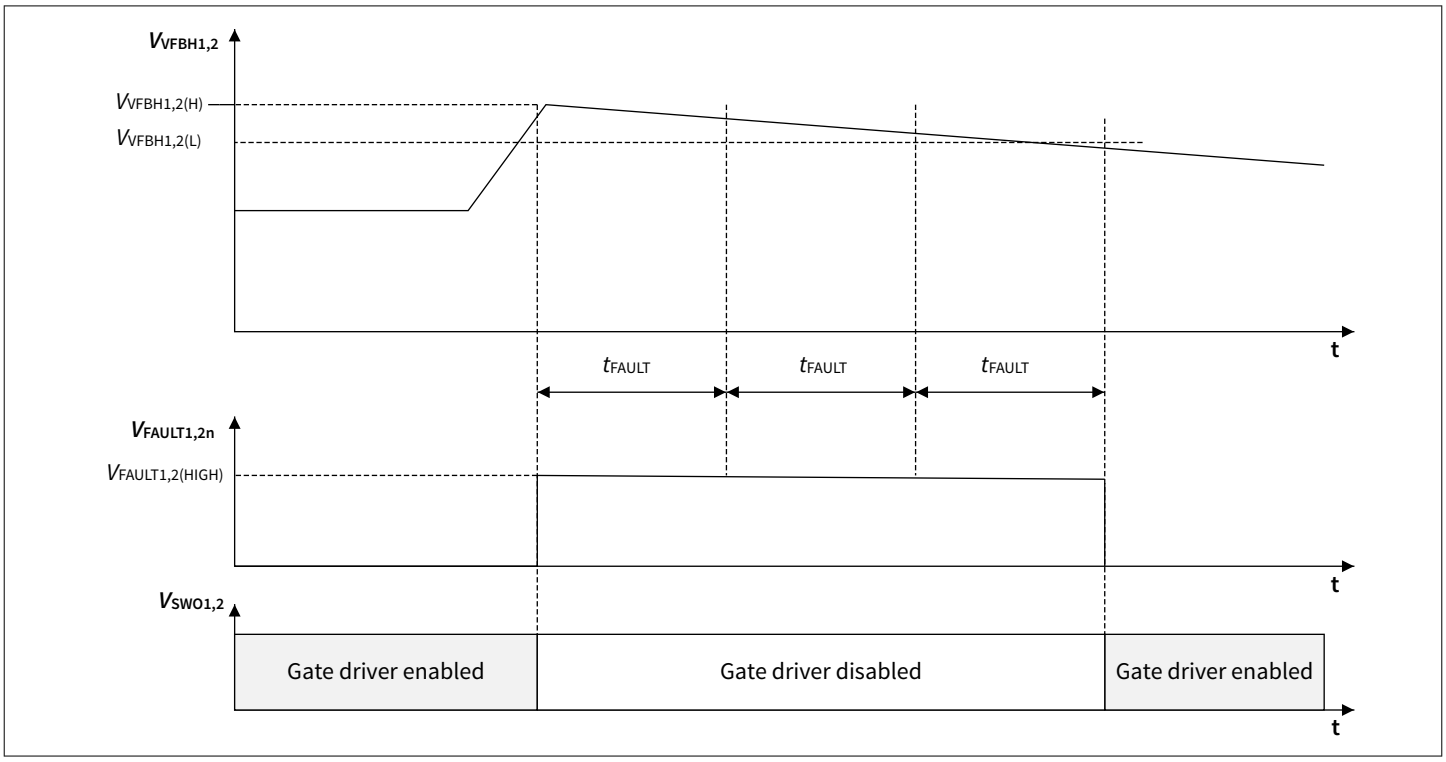


Figure 17 Timing diagram during overvoltage on FBH pin

When the fault disappears, the channel restarts with soft-start routine and no fault reported on FAULT1,2 pin.

If the fault appears during the soft-start routine, it interrupts the soft-start for a t_{FAULT} time and then the routine restarts.

The fault is detected even when the voltage on PWMI1,2 pin is lower than $V_{PWMI1,2(OFF)}$.

10.4.1 Electrical characteristics

Table 16 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
FBH1 FBH2 overvoltage upper threshold	$V_{FBH1,2(H)}$	72	–	75	V	$V_{FBH1,2}$ increasing	PRQ-381
FBH1 FBH2 overvoltage lower threshold	$V_{FBH1,2(L)}$	65	–	–	V	$V_{FBH1,2}$ decreasing	PRQ-383

10.5 Overtemperature

Thermal shutdown is an internal feature designed to prevent the device destruction and it is not intended for continuous use in normal operation.

If the junction temperature reaches the overtemperature shutdown $T_{J(SD)}$, the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator.

The junction temperature is checked each t_{FAULT} period, and when it is cooled down to ($T_{J(SD)}$-$T_{J(SD\_HYS)}$) the device will automatically restart with a soft-start.

The thermal shutdown operates on both the channels.

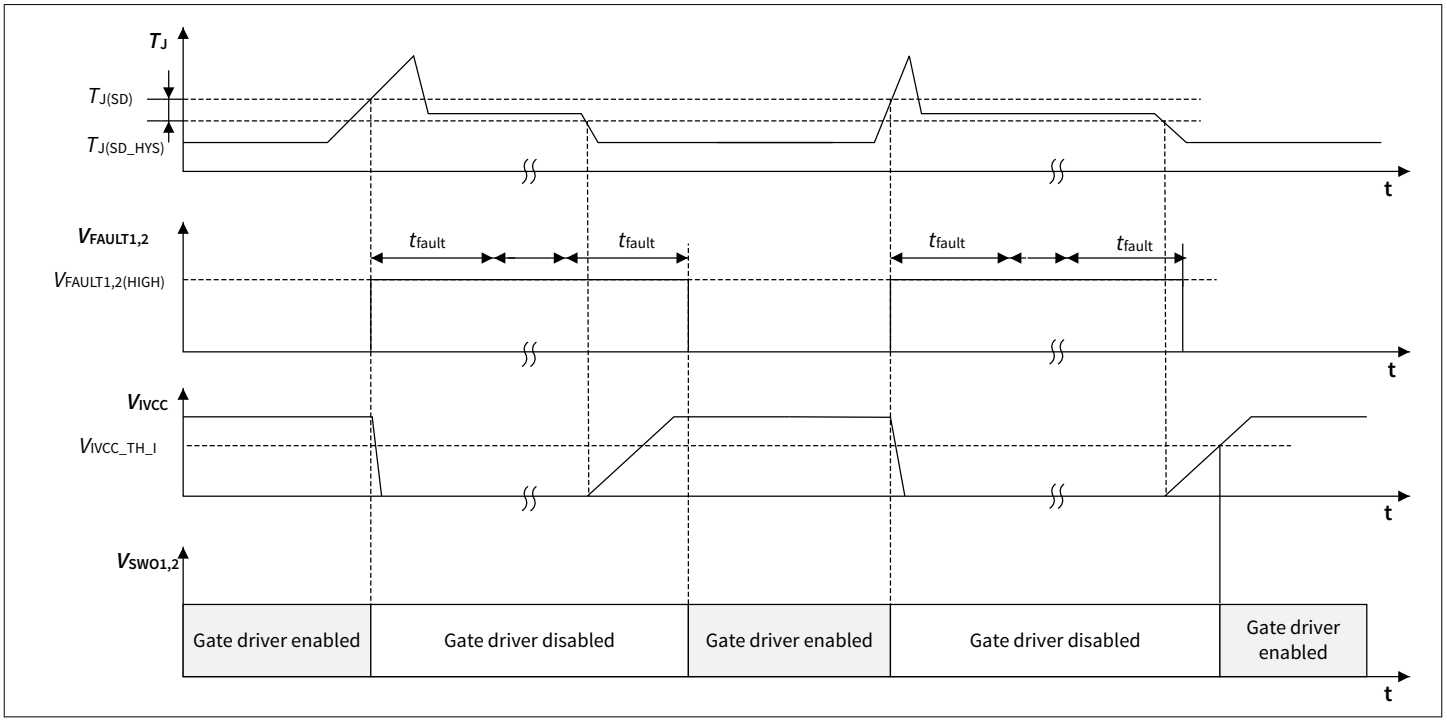


Figure 18 Timing diagram during overtemperature protection

10.5.1 Electrical characteristics

Table 17 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overtemperature shutdown	$T_{J(SD)}$	160	175	190	°C	1)	PRQ-408
Overtemperature shutdown hysteresis	$T_{J(SD\_HYS)}$	–	10	–	°C	1)	PRQ-409

1) Not subject to production test, specified by design

11 Application information

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

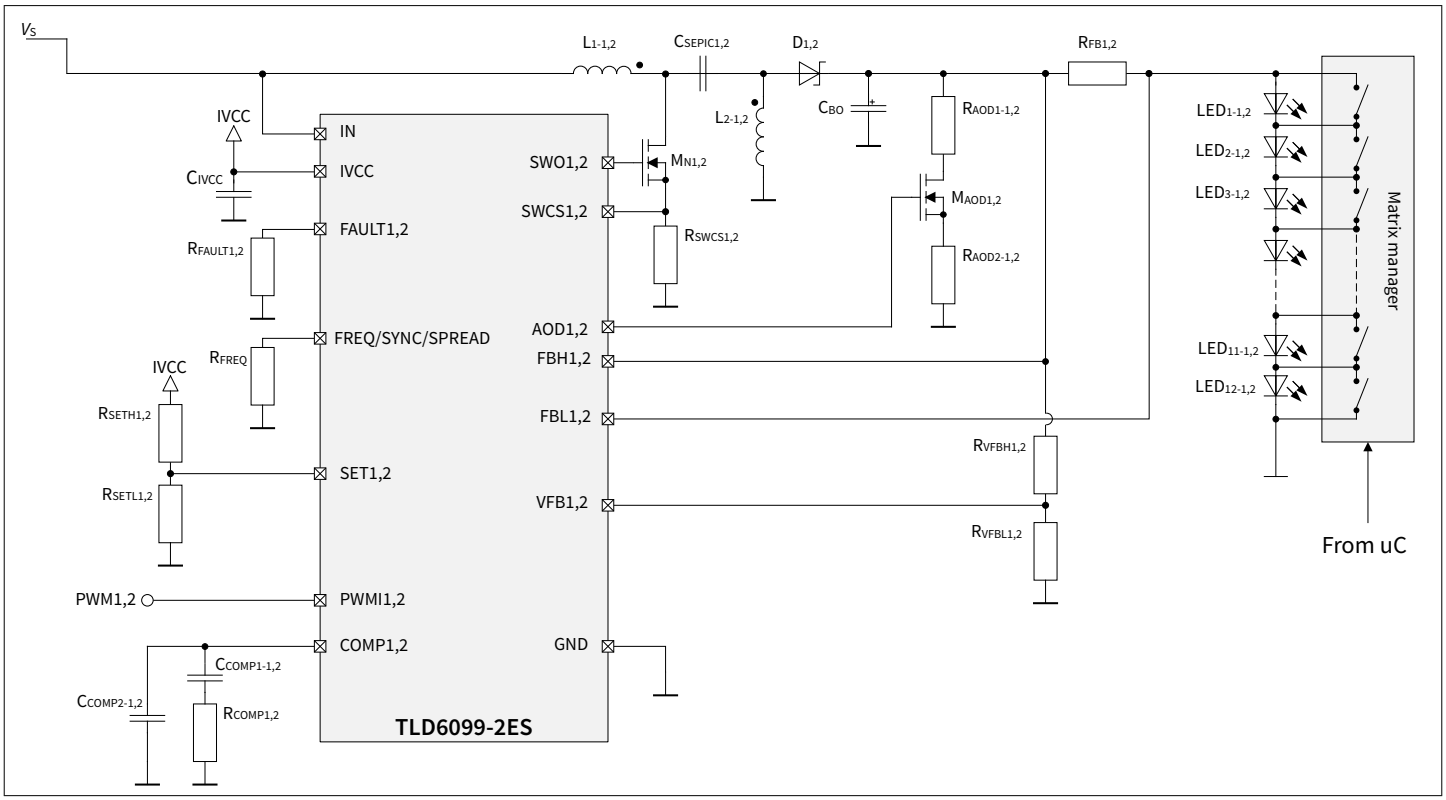


Figure 19 Application diagram

12 Package information

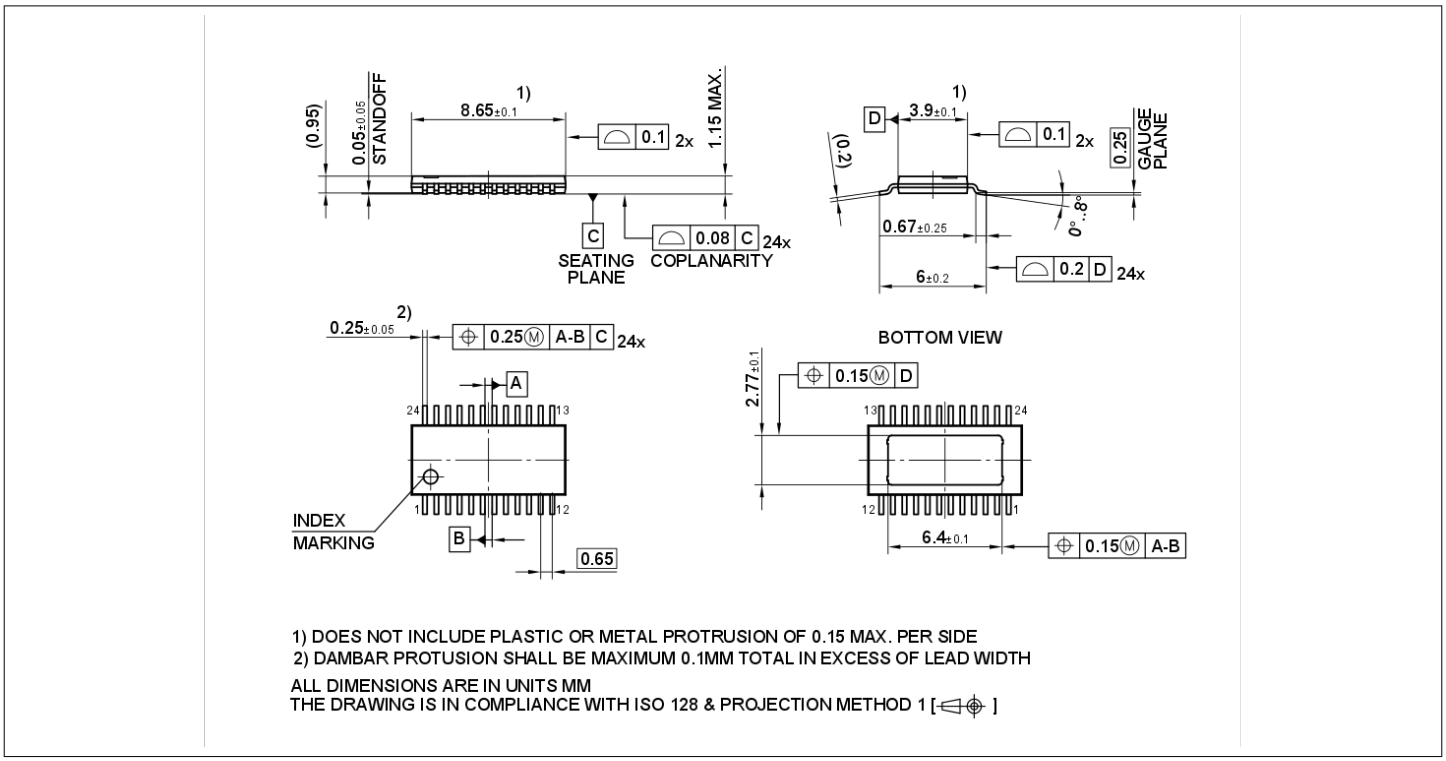


Figure 20 Package dimensions PG-TSDSO-24

***Note**: **Green product (RoHS compliant)** To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).*

Further information on packages www.infineon.com/packages

13 Revision history

13.1 Revision history

Document version	Date of release	Description of changes
Rev. 1.11	2024-09-17	• Changed severity level
Rev. 1.10	2024-07-22	• Parameter update in PRQ-135 and PRQ-136
Rev. 1.00	2024-07-10	• Initial document release

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Edition 2024-09-17

Published by

Infineon Technologies AG

81726 Munich, Germany

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Email: erratum@infineon.com

Document reference
IFX-yke1709888981843

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