

75 Ω VIDEO LINE DRIVER

FEATURES

- Superimpose Circuit for Character (140 IRE) and Border (70 IRE) Generation
- Fixed Gain (6 dB)
- Internal 75 Ω Driver with Clamp Circuit
- Very Small Output Capacitor Using SAG Function Pin
- Active High ON/OFF Control
- Very Low Standby Current (typ. $I_{\text{STBY}} \leq 25 \mu\text{A}$)
- Single +5 V Power Supply Operation

APPLICATIONS

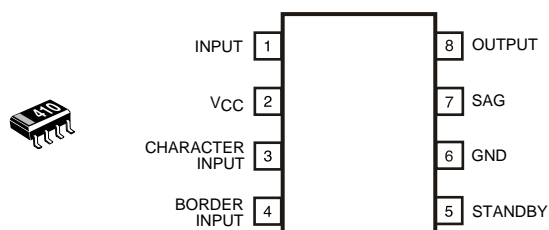
- Video Equipment
- Digital Cameras
- CCD Cameras
- TV Monitors
- Video Tape Recorders
- LCD Projectors

DESCRIPTION

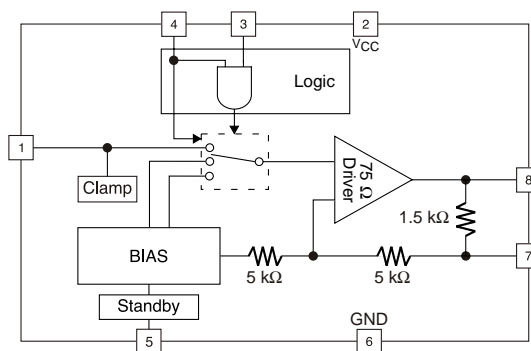
Operating from a single +5 V supply, the TK15410 is a single-channel video line driver IC that takes a standard video analog input and provides a buffered analog output for driving a 150 Ω load. The standard video input signal (1 $V_{\text{P-P}}$ typical) is internally clamped to 1.25 V and amplified 6 dB to produce 2 $V_{\text{P-P}}$ (typical) into a series 75 Ω resistor and 75 Ω cable load. The internal 1.5 k Ω SAG function resistor provides gain compensation for low frequency signals. The built-in superimpose circuit provides the addition of character (140 IRE) and border (70 IRE) generation to the video signal. During standby (Pin 5 grounded), the TK15410 consumes only 125 μW of power. Nominal power dissipation (no input) is typically 73 mW.

The TK15410M is available in the SOT23L-8 surface mount package.

TK15410



BLOCK DIAGRAM



ORDERING INFORMATION

TK15410M □□

Tape/Reel Code

TAPE/REEL CODE
TL: Tape Left

TK15410

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6 V
Operating Voltage Range 4.5 to 5.5 V
Power Dissipation (Note 1) 200 mW

Storage Temperature Range -55 to +150 °C
Operating Temperature Range -25 to +85 °C

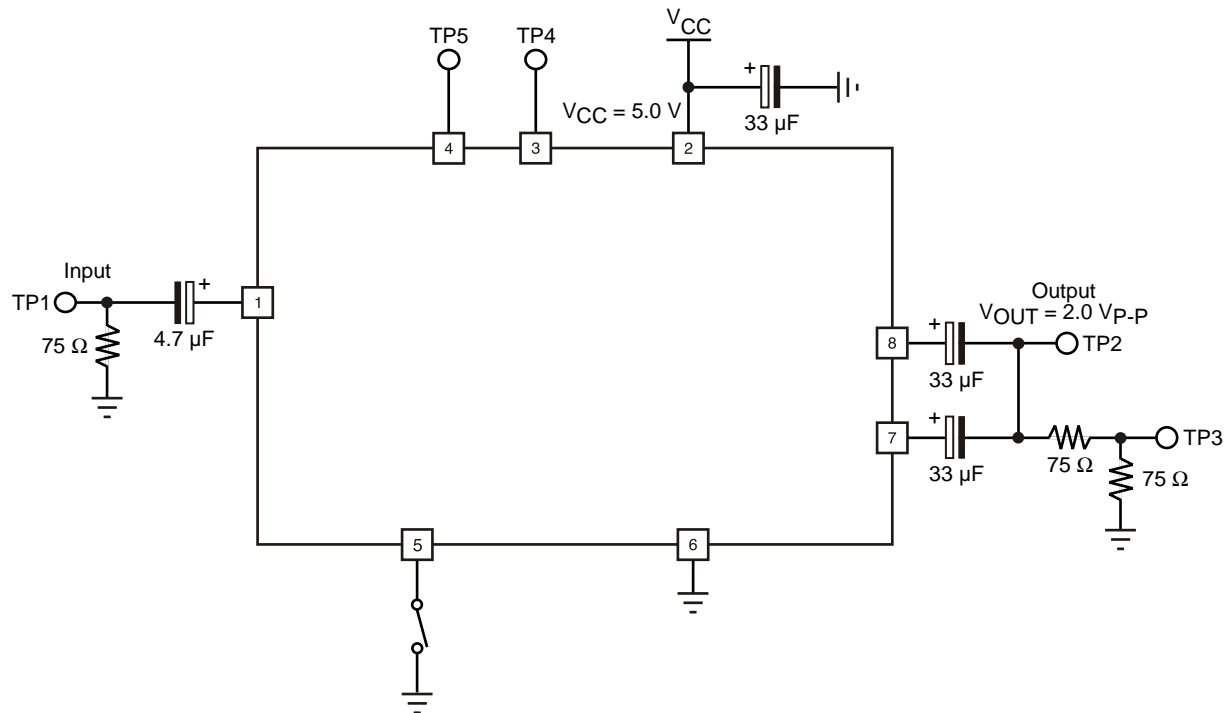
TK15410M ELECTRICAL CHARACTERISTICS

Test conditions: $V_{CC} = 5.0$ V, $V_{IN} = 1.0$ V_{P-P}, $R_L = 150$ Ω , $T_A = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current	No input		14.5	20.0	mA
I_{STBY}	Standby Supply Current	Pin 5 Grounded		25.0	50.0	μ A
I_{OS}	Standby Terminal Current	Pin 5 in Standby mode		25.0	50.0	μ A
$V_{THL(SUPER)}$	Superimpose Threshold Voltage (High to Low)	Pin 3, Pin 4	GND		0.80	V
$V_{TLH(SUPER)}$	Superimpose Threshold Voltage (Low to High)	Pin 3, Pin 4	2.00		V_{CC}	V
$V_{THL(STBY)}$	Standby Threshold Voltage (High to Low)	Pin 5 Operating to Standby mode	GND		0.60	V
$V_{TLH*STBY)}$	Standby Threshold Voltage (Low to High)	Pin 5 Standby to Operating mode	2.00		V_{CC}	V
V_{CMP}	Clamp Voltage	Pin 1 Input terminal	1.05	1.25	1.45	V
V_{CHA}	Character Level	Pin 7 SAG terminal	130	140	150	IRE
V_{BOR}	Border Level	Pin 7 SAG terminal	60	70	80	IRE
GVA	Voltage Gain	$f_{in} = 1$ MHz	5.45	5.95	6.45	dB
DG	Differential Gain	Staircase signal input	-3.0	+1.3	+3.0	%
DP	Differential Phase	Staircase signal input	-3.0	+0.2	+3.0	deg
fr	Frequency Response	$f_{in} = 1$ MHz / 5 MHz		-0.4		dB

Note 1: Power dissipation is 200 mW in free air. Derate at 1.6 mW/°C for operation above 25°C.

TEST CIRCUIT



Output Truth Table

Pin 3	Pin 4	Output
L	L	Pin 1
L	H	V_{BOR}
H	L	Pin 1
H	H	V_{CHA}

MEASUREMENT METHOD

1. Supply Current (I_{CC})

The Pin 2 current is measured with no input signal and the Standby Pin (Pin 5) open.

2. Standby Supply Current (I_{STBY})

The Pin 2 current is measured when the Standby Pin (Pin 5) is connected to ground.

3. Standby Terminal Current (I_{OS})

The Pin 5 current is measured when the Standby Pin (Pin 5) is connected to ground.

4. Standby Threshold Voltage (High to Low) ($V_{THL(STBY)}$)

The Pin 5 voltage is measured at the point which changes the device from operating mode into standby mode.

MEASUREMENT METHOD (CONT.)

5. Standby Threshold Voltage (Low to High) ($V_{TLH(STBY)}$)

The Pin 5 voltage is measured at the point which changes the device from standby mode into operating mode.

6. Superimpose Threshold Voltage (High to Low) ($V_{THL(SUPER)}$)

The voltage at TP4 and/or TP5 is slowly decreased. The TP4 and TP5 voltage level is measured at the point at which the video signal is applied to TP2.

7. Superimpose Threshold Voltage (Low to High) ($V_{TLH(SUPER)}$)

The voltage at TP5 and/or TP4 is slowly increased. The TP4 and TP5 voltage level is measured at the point at which the character signal or the border signal (in accordance with the Output Truth Table) is applied to TP2.

8. Clamp Voltage (V_{CMP})

The DC voltage at Pin 1 is measured with no input signal.

9. Character Level (V_{CHA})

The character level equation is as follows:

$$V_{CHA} = (V2 - V1)/(1/140)$$

Where V1 is the measured voltage at TP3 when TP4 and TP5 are at a low level and V2 is the measured voltage at TP3 when TP4 and TP5 are at a high level.

10. Border Level (V_{BOR})

The border level equation is as follows:

$$V_{BOR} = (V2 - V1)/(1/140)$$

Where V1 is the measured voltage at TP3 when TP4 and TP5 are at a low level and V2 is the measured voltage at TP3 when TP4 is at a low level and TP5 is at a high level.

11. Voltage Gain (GVA)

The voltage gain equation is as follows:

$$GVA = 20 \log_{10} V2/V1$$

Where V1 is the input voltage at TP1 and V2 is the measured voltage at TP2.

12. Differential Gain (DG)

The differential gain is measured at TP3 when a staircase waveform of 10 steps is applied to TP1.

13. Differential Phase (DP)

The differential phase is measured at TP3 when a staircase waveform of 10 steps is applied to TP1.

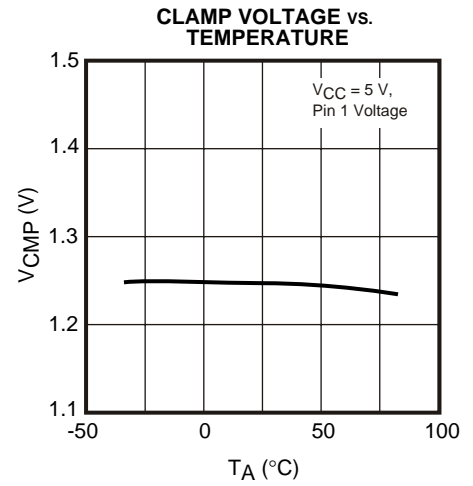
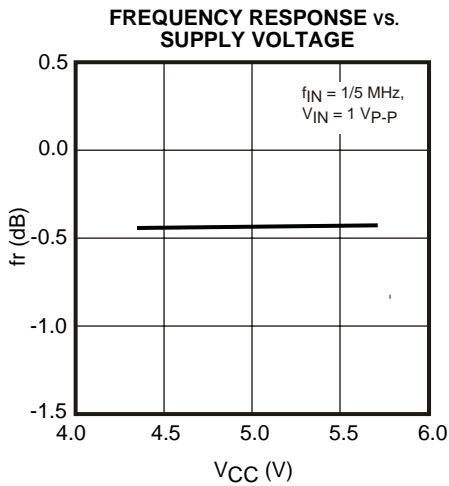
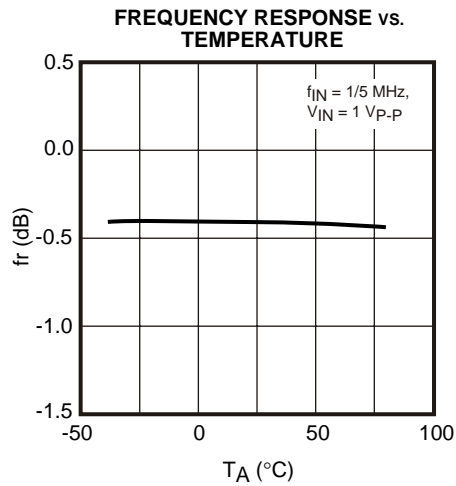
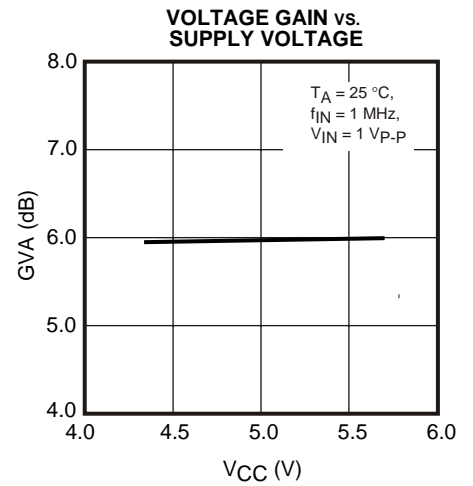
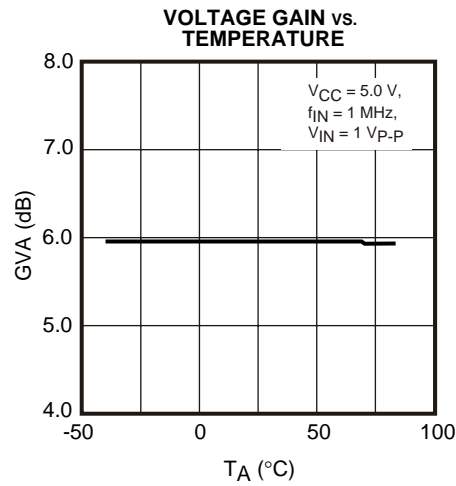
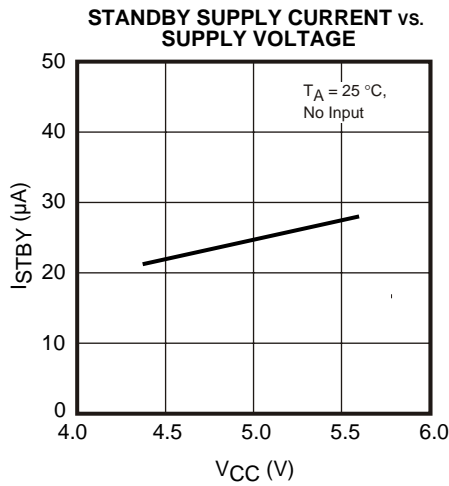
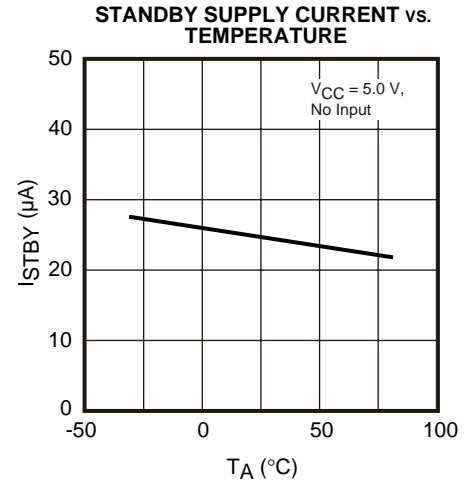
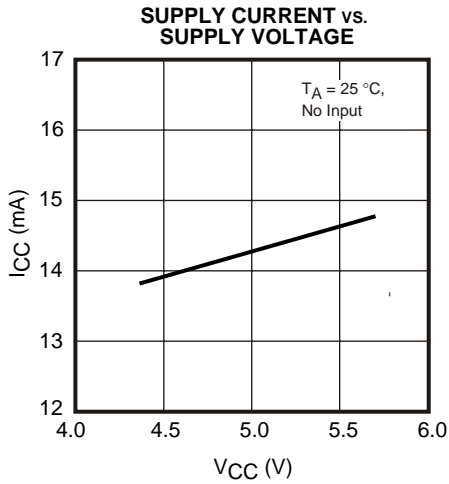
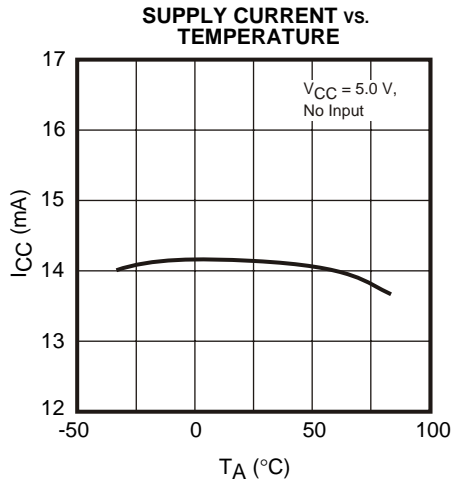
14. Frequency Response (fr)

The frequency response equation is as follows:

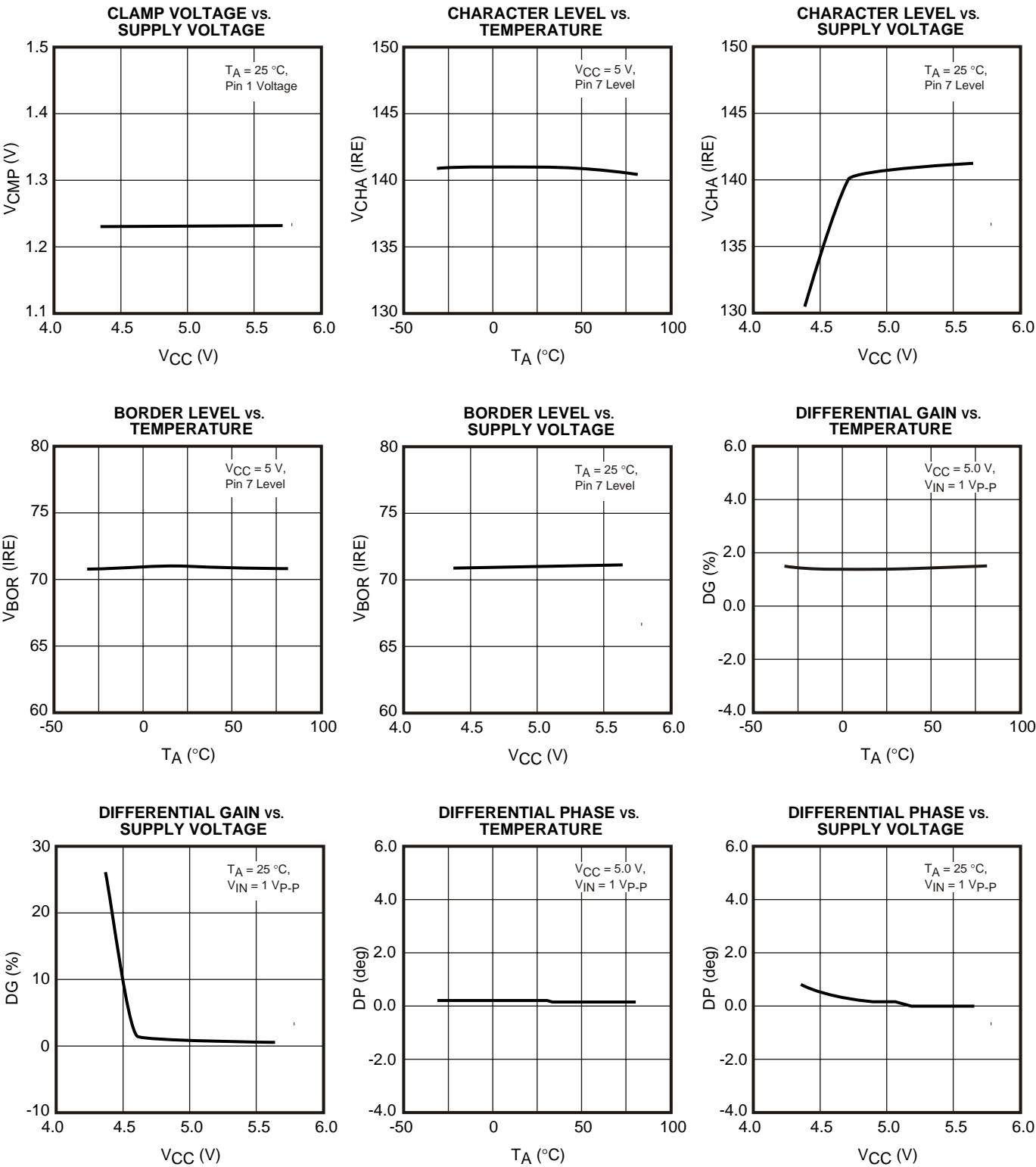
$$fr = 20 \log_{10} V2/V1$$

Where V1 is the measured TP3 voltage when the input frequency is set to 1 MHz and V2 is the measured TP3 voltage when the input frequency is set to 5 MHz.

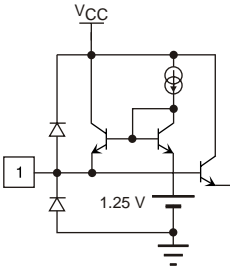
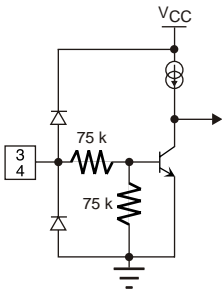
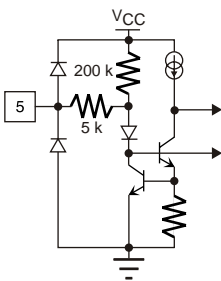
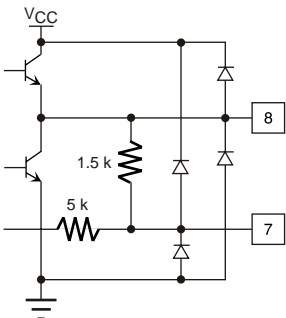
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

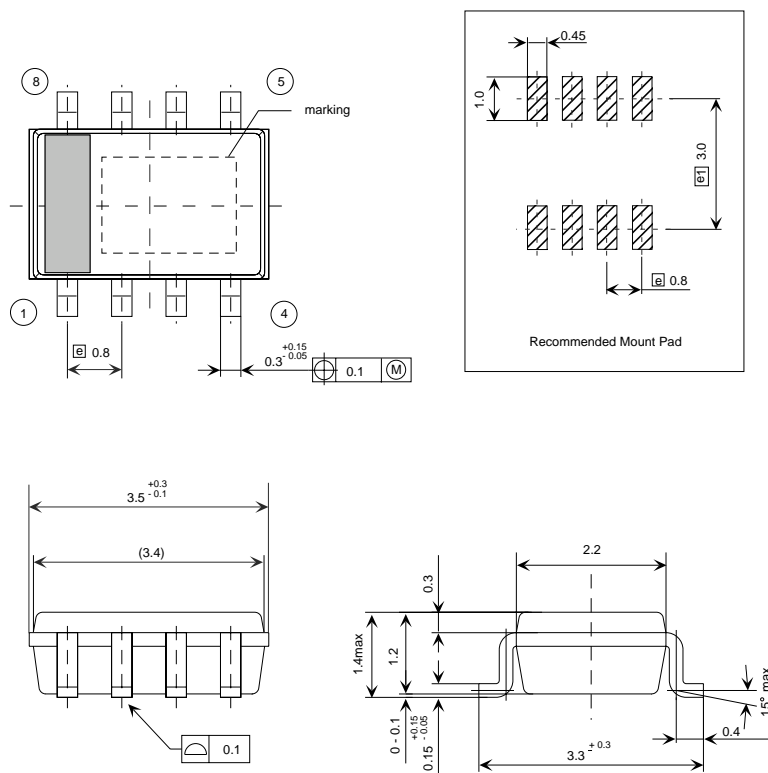


PIN FUNCTION DESCRIPTION

TERMINAL			INTERNAL EQUIVALENT CIRCUIT	DESCRIPTION
PIN NO.	SYMBOL	VOLTAGE		
1	INPUT	1.25 V		Luminance Input Terminal. The luminance input signal is clamped at 1.25 V.
2	V_{CC}	V_{CC}		Power Supply Terminal
3 4	CHARACTER INPUT BORDER INPUT			Pin 3: Character Signal Input Terminal. Pin 4: Border Signal Input Terminal. A video signal, a character signal, and a border signal can be selected by combining the logic levels of these two terminals.
5	STANDBY	2.1 V		Standby Logic Terminal. The device is in the standby mode when Pin 5 is connected to Low. The device is in the operating mode when Pin 5 is connected to High or Open.
6	GND	GND		GND Terminal
7 8	SAG OUTPUT	1.25 V 1.25 V		Pin 7: SAG Terminal. Pin 8: Output Terminal. The output is available to drive a $75\ \Omega + 75\ \Omega$ load.

PACKAGE OUTLINE

SOT23L-8



Dimensions are shown in millimeters
Tolerance: x.x = ± 0.2 mm (unless otherwise specified)

Marking Information

TK15410

Marking
410



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