3.0A Low Output Voltage Ultra LDO Regulator TJ47300

FEATURES

- Works with 1.25V ~ 5.5V V_{IN}
- Ultra Low Dropout Voltage
- Low Quiescent Current
- Excellent Line and Load Regulation
- Guaranteed Output Current of 3.0A
- Adjustable Output Voltage Down to 0.8V
- V_{OUT} Power OK Signal
- Logic Controlled Shutdown Option
- Over-Temperature/Over-Current Protection
- -40℃ to 125℃ Junction Temperature Range

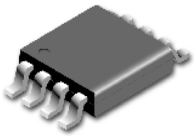
APPLICATION

- Motherboards and Graphic Cards
- Microprocessor and Chipset Power Supplies
- Peripheral Cards
- Low Voltage Digital ICs
- High Efficiency Linear Regulators

DESCRIPSION

The TJ47300 is a 3.0A high performance ultra low-dropout linear regulator ideal for powering core voltages of low-power microprocessors. The TJ47300 implements a dual supply configuration allowing for very low output impedance. The TJ47300 requires a bias input supply and a main input supply, allowing for ultra-low input voltages on the main supply rail. The input supply operates from 1.25V to 5.5V and the bias supply requires between 3V and 5.5V for proper operation. The TJ47300 delivers high current and ultra-low-dropout output voltage as low as 0.8V for applications where V_{OUT} is very close to V_{IN}. The TJ47300 is developed on a CMOS technology which allows low quiescent current operation independent of output current. This technology also allows the TJ47300 to operate under extremely low dropout conditions.

SOP-8-PP



ORDERING INFORMATION

Device	Package
TJ47300GDP	SOP8-PP

ABSOLUTE MAXIMUM RATINGS

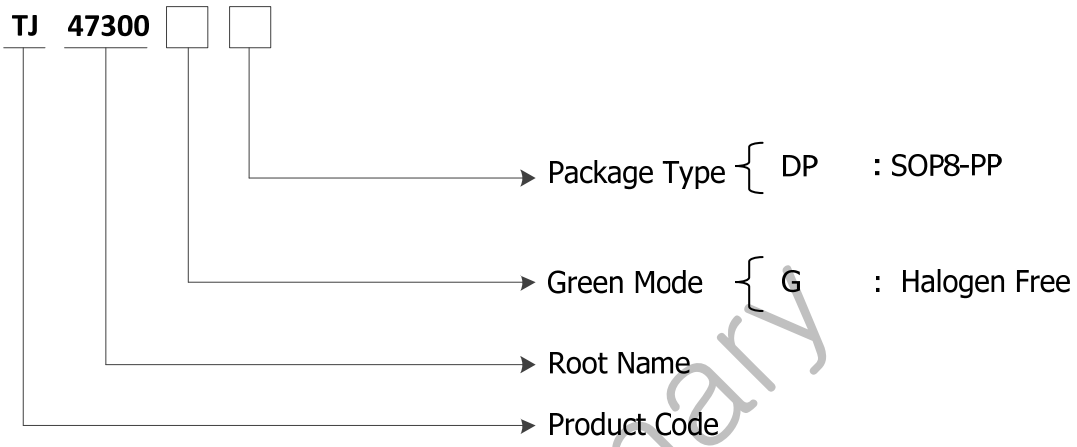
CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Input Supply Voltage (Survival)	V_{IN}	-0.3	6	V
Enable Input Voltage (Survival)	V_{EN}	-0.3	6	V
Bias Supply Voltage (Survival)	V_{BIAS}	-0.3	6	V
Output Voltage (Survival)	V_{OUT}	-0.3	V_{IN} +0.3	V
Lead Temperature (Soldering, 5 sec)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	-65	150	℃
Operating Junction Temperature Range	T_{JOPR}	-40	125	℃
Package Thermal Resistance *	$\Theta_{JA\text{-}SOP8\text{-}PP}$	68		ºC/W

* Calculated from package in still air, mounted to 2.6mm X 3.5mm(minimum foot print) 2 layer PCB without thermal vias per JESD51 standards.

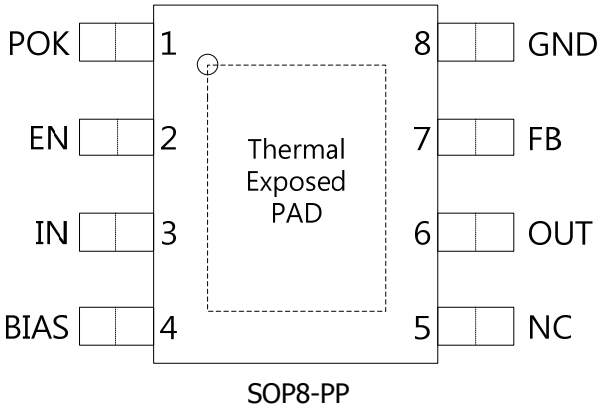
ORDERING INFORMATION

Package	Order No.	Description	Package Marking	Compliance	Supplied As
SOP8-PP	TJ47300GDP	3.0A, Enable, Adjustable, Power OK	TJ47300G	RoHS, Halogen Free	Reel

ORDERING INFORMATION (Continued)



PIN CONFIGURATION

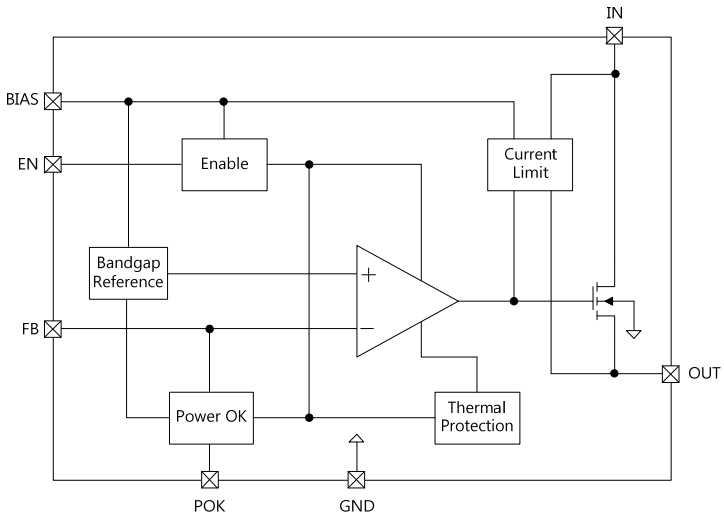


SOP8-PP

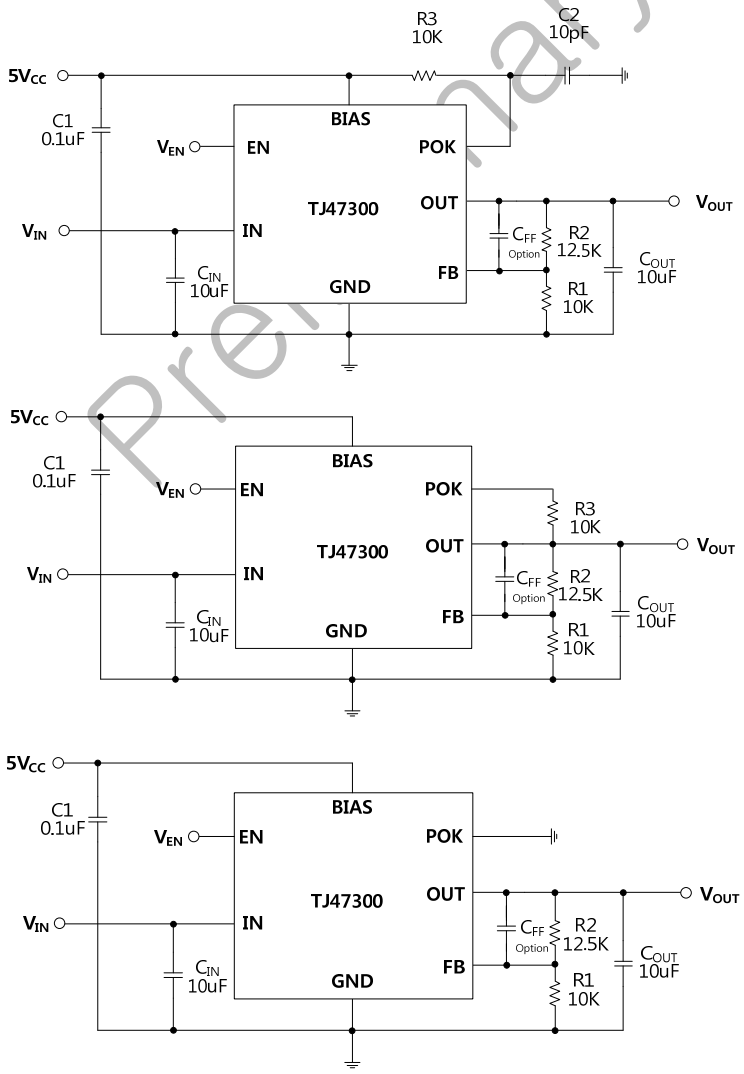
PIN DESCRIPTION

Pin No.	Pin Name	Pin Function
1	POK	Power OK Indication. This pin is an Open-drain output and is set high impedance once V_{OUT} reaches 92% of its rating voltage.
2	EN	Enable Input. Pulling this pin below 0.4V turns the regulator off. Do not float
3	IN	Power Input. This pin is the drain input to the power device that supply current to output pin.
4	BIAS	Supply Input for Internal Circuit. Input Bias Voltage for powering all circuitry on the regulator except the output power TR.
5	NC	No Connection.
6	OUT	Power Output. This pin is power output of the device.
7	FB	Feedback Voltage. A resistor divider from the output to GND is used to set the regulation voltage as V_{OUT}= 0.8V x (1+R2/R1)
8	GND	Ground
-	Thermal Exposed PAD	Connect to Ground.

BLOCK DIAGRAM



TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{BIAS} = 5V, V_{IN} = $V_{O(NOM)}$ + 1V, V_{EN}=V_{BIAS}, I_L = 10 mA, T_A=25℃.

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Input Voltage		V_{IN}	V_{OUT}=V_{REF}	1.25	-	5.5	V
Bias Input Voltage		V_{BIAS}	V_{OUT}=V_{REF}	3.0	-	5.5	V
Reference Voltage		V_{REF}	V_{BIAS}=V_{IN}=V_{EN}=5.0V, I_{OUT}=10mA, V_{OUT}=V_{REF}	0.784	0.8	0.816	V
V_{IN} Line Regulation(Note 1)		$\Delta V_{LINE(IN)}$	V_{OUT}+1V<V_{IN}<5.5V, I_{OUT}=10mA	-	0.02	0.10	%/V
V_{BIAS} Line Regulation(Note 2)		$\Delta V_{LINE(BIAS)}$	V_{IN}=3.3V, I_{OUT}=10mA, V_{OUT}=V_{REF}	-	0.02	0.10	%/V
Load Regulation(Note 1, 3)		ΔV_{LOAD}	10mA < I_L <3A, V_{CNTL}=V_{IN}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	0.20	0.75	%
Dropout Voltage		V_{DROP}	I_L = 1.0A, V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	120	150	mV
			I_L = 2.0A, V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	240	300	
			I_L = 3.0A, V_{BIAS}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	380	450	
Ground Pin Current(Note 4)		I_{GND1}	I_L = 10mA	-	0.1	1.0	mA
			I_L = 3.0 A	-	0.1	1.0	mA
		I_{GND2}	V_{EN} < 0.4 V, POK=open (Note5)	-	-	150	uA
Enable Threshold	Logic High	V_{IH}	Output=High	2.0	-	-	V
	Logic Low	V_{IL}	Output=Low	-	-	0.4	V
EN Input Current		I_{EN}	V_{EN}=V_{CNTL}=5.0V	-	-	0.5	uA
FB Power OK Threshold		V_{POKTH}	I_{OUT}=0A, V_{CNTL}=V_{IN}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	90	-	%
Power OK Hysteresis		V_{POKHYS}	I_{OUT}=0A, V_{CNTL}=V_{IN}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	10	-	%
OCP Threshold Level		I_{OCP}	V_{CNTL}=V_{IN}=V_{EN}=5.0V, V_{OUT}=V_{REF}	-	4.5	-	A
Thermal Shutdown Temperature		T_{SD}		-	165	-	℃
Thermal Shutdown Hysteresis		ΔT_{SD}		-	10	-	℃

Note 1. Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current.

Note 2. Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the bias line voltage.

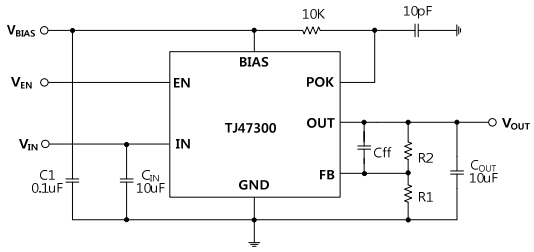
Note 3. Regulation is measured at constant junction temperature by using a 10ms current pulse. Devices are tested for load regulation in the load range from 10mA to 3.0A

Note 4. I_{GND} = I_{BIAS} + (I_{IN} – I_{OUT}). The total current drawn from the supply is the sum of the load current plus the ground current.

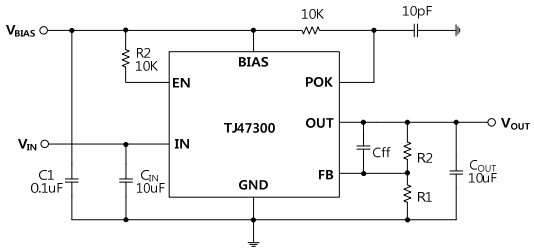
Note 5. When POK pin is applied to V_{BIAS} through the resistor R3, I_{GND2} should be added to the bias current (V_{BIAS} - V_{POK}) / R3.

TYPICAL OPERATING CHARACTERISTICS

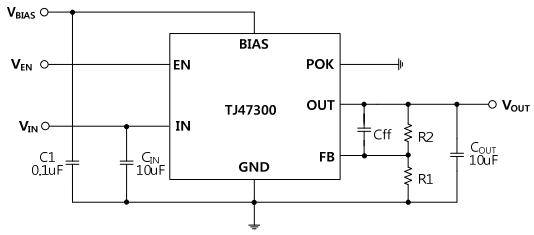
- TEST Circuit



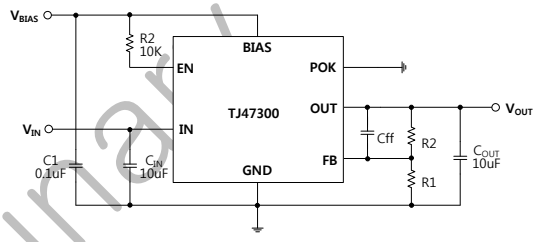
Circuit #1



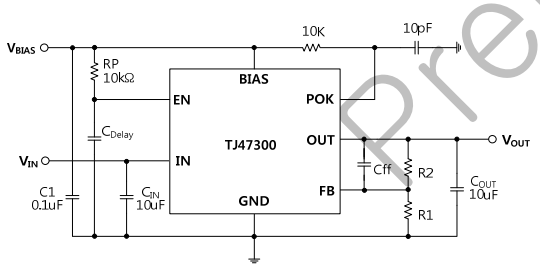
Circuit #2



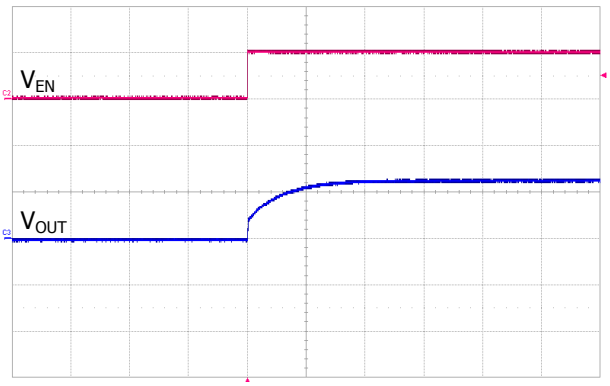
Circuit #3



Circuit #4



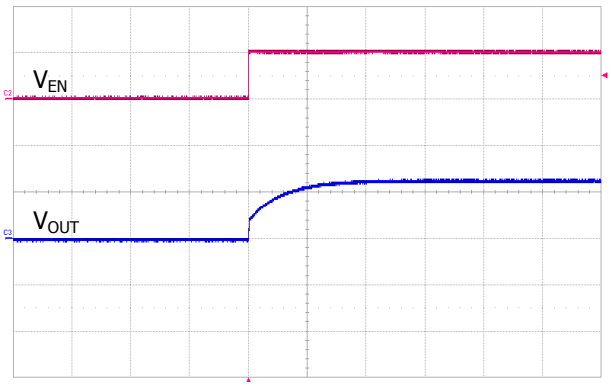
Circuit #5



VEN: 5V/div, VOUT: 2V/div, 200us/div

Start Up @ Iout=10mA, Circuit #1

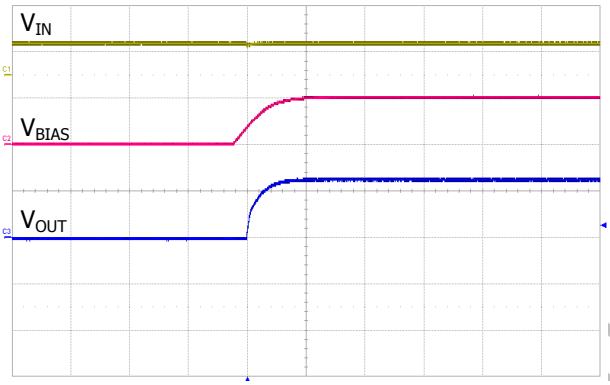
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V, V_{BIAS}=5.0V)



VEN: 5V/div, VOUT: 2V/div, 200us/div

Start Up @ Iout=3.0A, Circuit #1

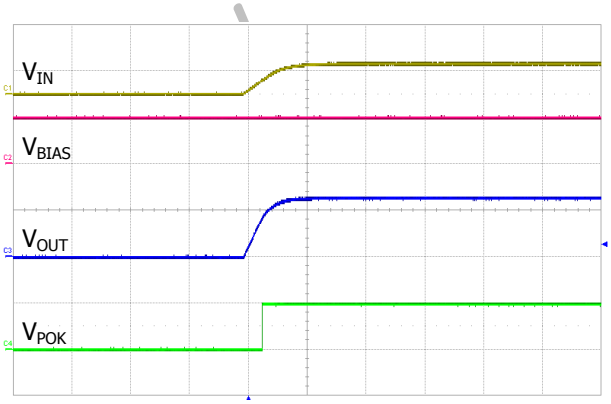
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V, V_{BIAS}=5.0V)



VIN: 5V/div, VBIAS: 5V/div, VOUT: 2V/div, 500us/div

Start Up with V_{BIAS} @ Iout=10mA, Circuit #2

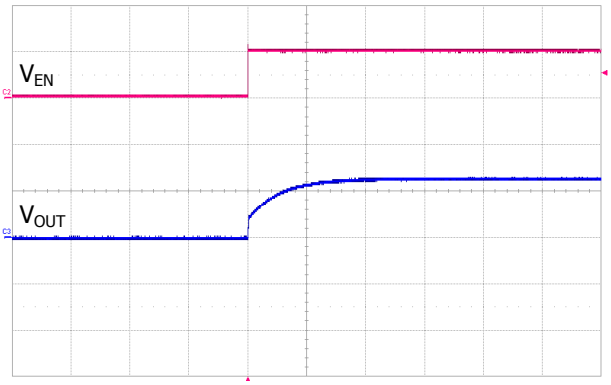
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V)



VIN: 5V/div, VBIAS: 5V/div, VOUT: 2V/div, VPOK: 5V/div, 500us/div

Start Up with V_{IN} @ Iout=10mA, Circuit #2

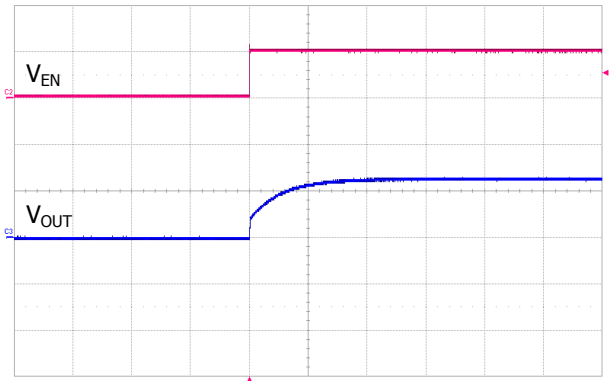
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{BIAS}=5.0V)



VEN: 5V/div, VOUT: 2V/div, 200us/div

Start Up @ Iout=10mA, Circuit #3

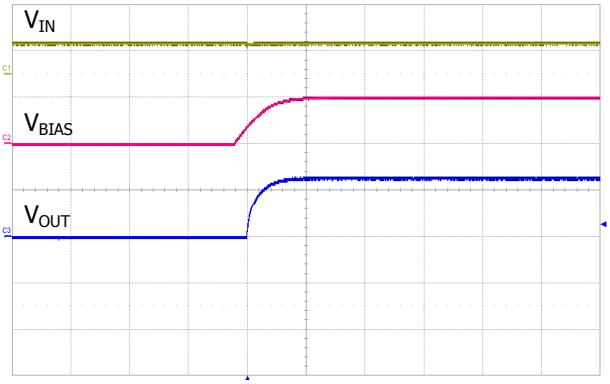
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V, V_{BIAS}=5.0V)



VEN: 5V/div, VOUT: 2V/div, 200us/div

Start Up @ Iout=3.0A, Circuit #3

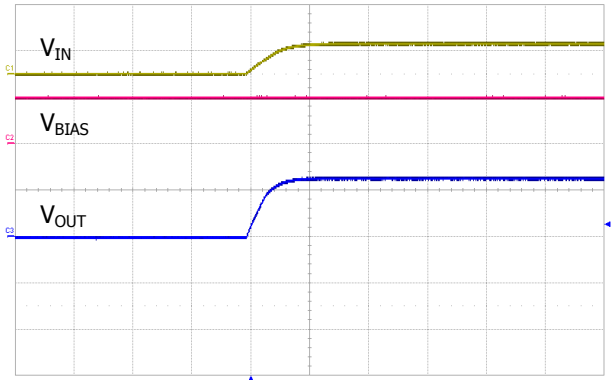
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V, V_{BIAS}=5.0V)



VIN: 5V/div, VBIAS: 5V/div, VOUT: 2V/div, 500us/div

Start Up with V_{BIAS} @ Iout=10mA, Circuit #4

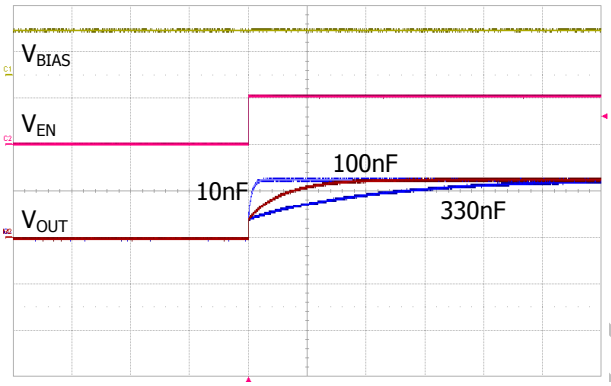
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V)



VIN: 5V/div, VBIAS: 5V/div, VOUT: 2V/div, 500us/div

Start Up with V_{IN} @ Iout=10mA, Circuit #4

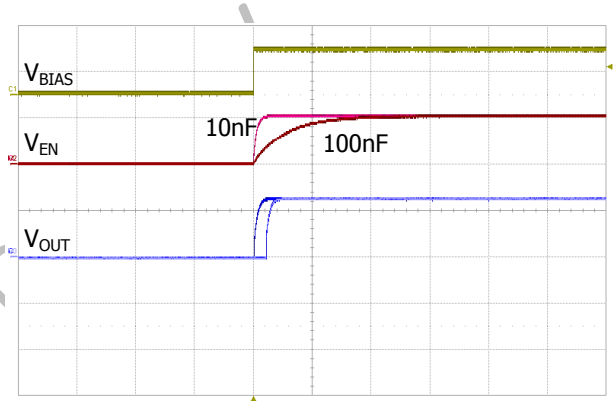
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{BIAS}=5.0V)



VBIAS: 5V/div, VEN: 5V/div, OUT: 2V/div, 2ms/div

Start Up @ Iout=10mA, Circuit #1

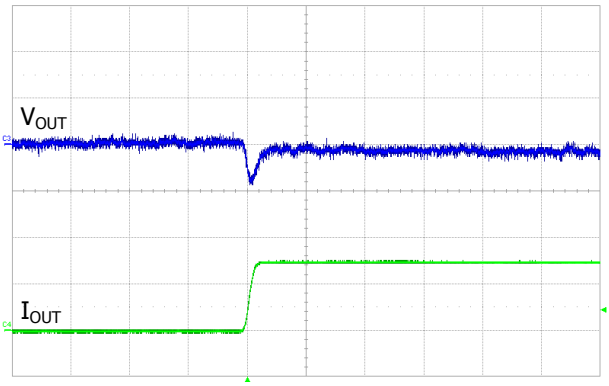
(Cff is varied, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V, V_{BIAS}=5.0V)



VBIAS: 5V/div, VEN: 5V/div, OUT: 2V/div, 2ms/div

Start Up @ Iout=10mA, Circuit #5

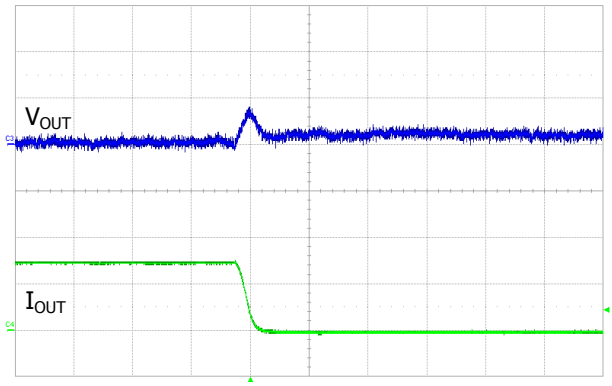
(Cdelay is varied, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V)



VOUT: 20mV/div, IOUT: 2A/div, 100us/div

Load Transient Response

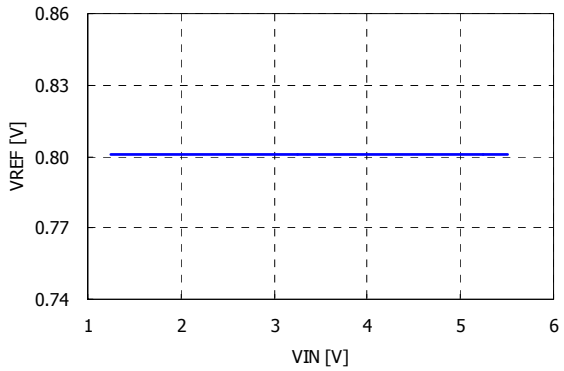
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V, V_{BIAS}=5.0V)



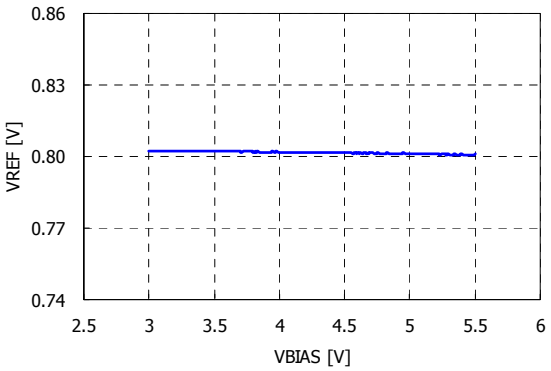
VOUT: 20mV/div, IOUT: 2A/div, 100us/div

Load Transient Response

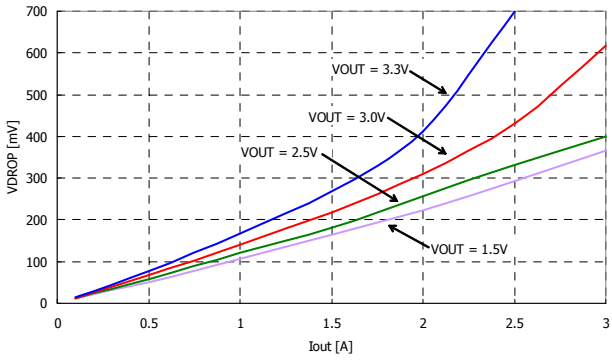
(Cff=10nF, R2=10kΩ, R1=4.7kΩ, V_{IN}=3.5V, V_{BIAS}=5.0V)



V_{REF} vs. V_{IN} @ V_{BIAS}=5.5V



V_{REF} vs. V_{BIAS} @ V_{IN}=5.5V



Dropout Voltage

APPLICATION INFORMATION

The TJ47300 is a high performance, low dropout linear regulator, designed for high current application that requires fast transient response. The TJ47300 operates from two input supply voltages, significantly reducing dropout voltage. The TJ47300 is designed so that a minimum of external component are necessary.

Bias Supply Voltage

The TJ47300 control circuitry is supplied by the BIAS pin which requires a very low bias current even at the maximum output current level. A bypass capacitor on the bias pin is recommended to improve the performance of the TJ47300 during line and load transient. A small ceramic capacitor from BIAS pin to ground reduces high frequency noise that could be injected into the control circuitry from the bias rail. In practical applications, a 1uF capacitor and smaller valued capacitors such as 0.01uF or 0.001uF in parallel with that larger capacitor may be used to decouple the bias supply. The BIAS input voltage must be 2.1V above the output voltage, with a minimum BIAS input voltage of 3.0V.

Adjustable Regulator Design

An adjustable output device has output voltage range of 0.8V to 3.3V. To obtain a desired output voltage, the following equation can be used two external resistors as presented in the typical application circuit. The resistor values are given by;

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

It is suggested to use R1 values lower than 10kΩ to obtain better load transient performances. Even, higher values up to 100 kΩ are suitable.

Enable

The TJ47300 feature an active high Enable input (EN) that allows on/off control of the regulator. The enable function of TJ47300 has hysteresis characteristics. Pulling V_{EN} lower than 0.4V disables the chip. Pulling V_{EN} higher than 2.0V enables the output voltage.

Supply Power Sequencing

In common applications where the power on transient of V_{IN} and V_{BIAS} voltages are not particularly fast (Tr > 100us), no power sequencing is required. Where voltage transient input is very fast(Tr<100us), it is recommended to have the V_{IN} voltage present before or, at least, at the same time as the V_{BIAS} voltage in order to avoid over voltage spikes during the power on transient.

Output Capacitors

The TJ47300 requires an of output capacitance to maintain stability. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The TJ47300 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor which value is at least 10uF on the TJ47300 output ensures stability. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. A minimum ceramic capacitor over than 10uF should be very closely placed to the output voltage pin of the TJ47300.

Input Capacitor

A large bulk capacitance over than 10uF should be closely placed to the input supply pin of the TJ47300 to ensure that the input supply voltage does not sag. Also a minimum of 10uF ceramic capacitor is recommended to be placed directly next to the IN pin. It allows for the device being some distance from any bulk capacitor on the rail. Additionally, input droop due to load transients is reduced, improving load transient response. Additional capacitance may be added if required by the application.

Decoupling (Bypass) Capacitor

In very electrically noisy environments, it is recommended that additional ceramic capacitors be placed from VIN to GND. The use of multiple lower value ceramic capacitors in parallel with output capacitor also allows to achieve better transient performance and stability if required by the application. (See Fig.1)

Feed-Forward Capacitor

To get the higher PSRR than the inherent performance of TJ47300, it is recommended that additional ceramic feed-forward capacitor be placed from OUT pin to FB pin. The capacitance of feed-forward capacitor with range of 10pF to 1uF allows to achieve better PSRR performance when required by the application. (See Fig.1)

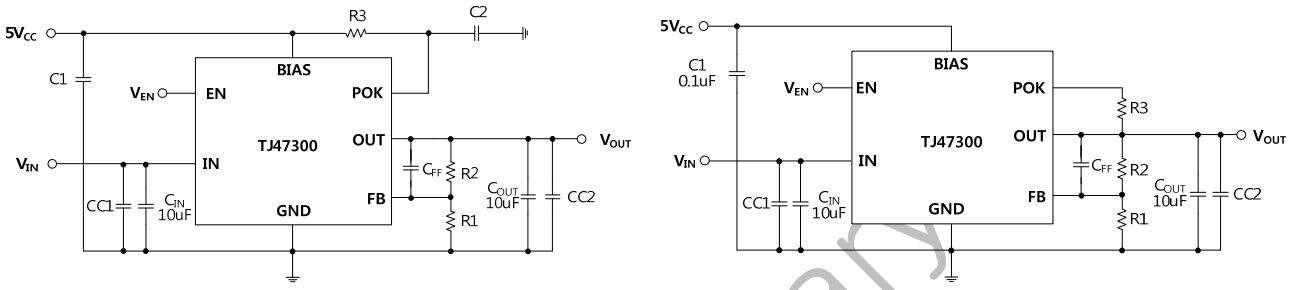


Fig. 1 Application with Decoupling & Feed-Forward Capacitor

Maximum Output Current Capability

The TJ47300 can deliver a continuous current of 3.0A over the full operating junction temperature range. However, the output current is limited by the restriction of power dissipation which differs from packages. A heat sink may be required depending on the maximum power dissipation and maximum ambient temperature of application. With respect to the applied package, the maximum output current of 3.0A may be still undeliverable due to the restriction of the power dissipation of TJ47300. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.
The temperatures over the device are given by:

$$T_C = T_A + P_D \times \theta_{CA} \quad / \quad T_J = T_C + P_D \times \theta_{JC} \; / \quad T_J = T_A + P_D \times \theta_{JA}$$

where T_J is the junction temperature, T_C is the case temperature, T_A is the ambient temperature, P_D is the total power dissipation of the device, θ_{CA} is the thermal resistance of case-to-ambient, θ_{JC} is the thermal resistance of junction-to-case, and θ_{JA} is the thermal resistance of junction to ambient.
The total power dissipation of the device is given by:

$$P_D = P_{IN} - P_{OUT} = \{(V_{IN} \times I_{IN}) + (V_{BIAS} \times I_{BIAS})\} - (V_{OUT} \times I_{OUT})$$

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

The maximum allowable value for junction-to-ambient thermal resistance, θ_{JA}, can be calculated using the formula:

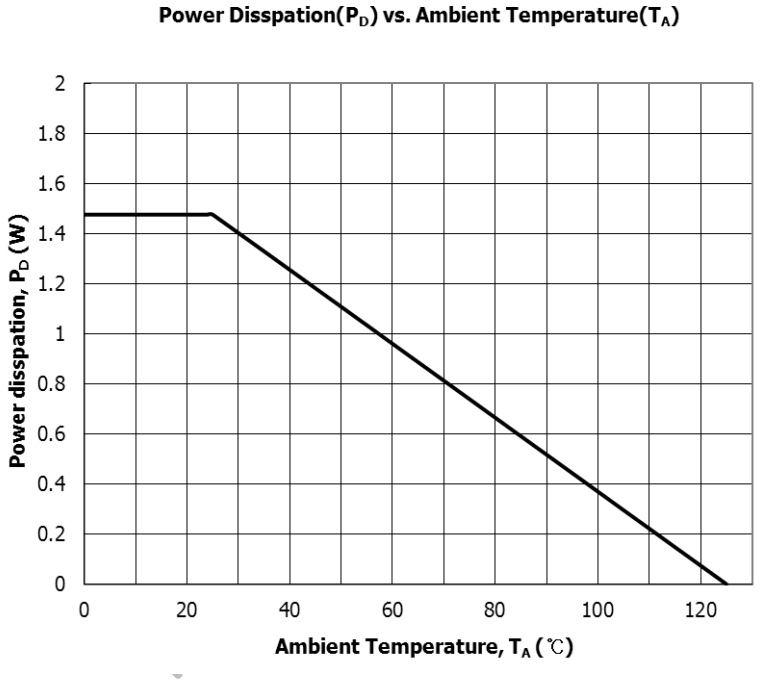
$$\theta_{JA} = T_{Rmax} / P_D = (T_{Jmax} - T_{Amax}) / P_D$$

TJ47300 is available in SOP8-PP package. The thermal resistance depends on amount of copper area or heat sink, and on air flow.

If proper cooling solution such as heat sink, copper plane area, air flow is applied, the maximum allowable power dissipation could be increased. However, if the ambient temperature is increased, the allowable power dissipation would be decreased.

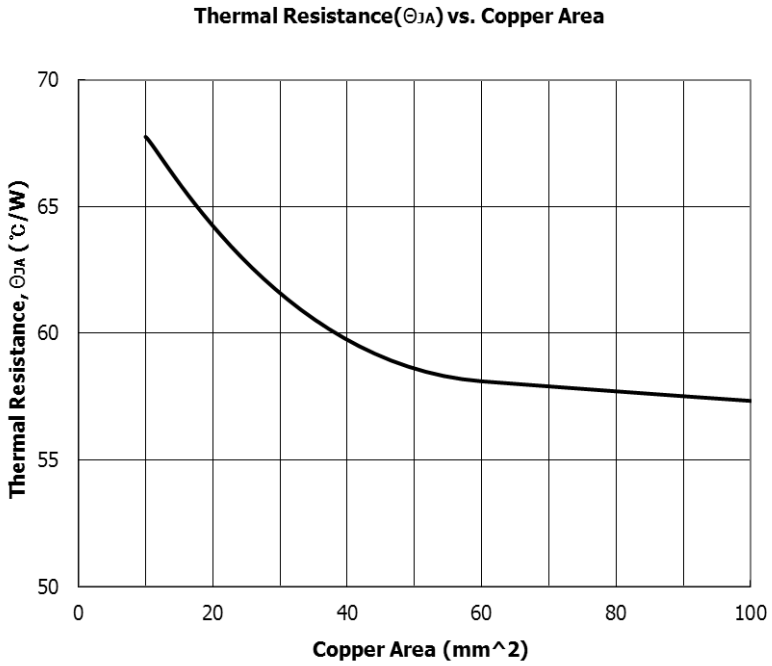
The θ_{JA} could be decreased with respect to the copper plane area. So, the specification of maximum power dissipation for an application is fixed, the proper copper plane area could be estimated by following graphs. Wider copper plane area leads lower θ_{JA}.

The maximum allowable power dissipation is also influenced by the ambient temperature. With the above θ_{JA}-Copper plane area relationship, the maximum allowable power dissipation could be evaluated with respect to the ambient temperature. As shown in graph, the higher copper plane area leads θ_{JA}. And the higher ambient temperature leads lower maximum allowable power dissipation.



The graph above is valid for the thermal impedance specified in the Absolute Maximum Ratings section on page 1.

The θ_{JA} could be decreased with respect to the copper plane area. So, the specification of maximum power dissipation for an application is fixed, the proper plane area could be estimated by following graphs. Wider copper plane area leads lower θ_{JA}.



The maximum allowable power dissipation is also influenced by the ambient temperature. With the θ_{JA}-Copper plane area relationship, the maximum allowable power dissipation could be evaluated with respect to the ambient temperature. As shown in graph, the higher copper plane area leads θ_{JA}. And the higher ambient temperature leads lower maximum allowable power dissipation.

PRELIMINARY REVISION NOTICE

The information in this datasheet can be revised without any notice.