

TIC116A, TIC116B, TIC116C, TIC116D, TIC116E, TIC116M, TIC116N, TIC116S

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

- 8 A Continuous On-State Current
- 80 A Surge-Current
- Glass Passivated Wafer
- 100 V to 800 V Off-State Voltage
- Max I_{GT} of 20 mA
- Compliance to ROHS

ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Value								Unit
		A	B	C	D	E	M	S	N	
V_{DRM}	Repetitive peak off-state voltage (see Note1)	100	200	300	400	500	600	700	800	V
V_{RRM}	Repetitive peak reverse voltage	100	200	300	400	500	600	700	800	V
$I_{T(RMS)}$	Continuous on-state current at (or below) 70°C case temperature (see note2)	8								A
$I_{T(AV)}$	Average on-state current (180° conduction angle) at(or below) 70°C case temperature (see Note3)	5								A
I_{TM}	Surge on-state current (see Note4)	80								A
I_{GM}	Peak positive gate current (pulse width $\leq 300 \mu s$)	3								A
P_{GM}	Peak power dissipation (pulse width $\leq 300 \mu s$)	5								W
$P_{G(AV)}$	Average gate power dissipation (see Note5)	1								W
T_C	Operating case temperature range	-40 to +110								°C
T_{stg}	Storage temperature range	-40 to +125								°C
T_L	Lead temperature 1.6 mm from case for 10 seconds	230								°C

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THERMAL CHARACTERISTICS

Symbol	Ratings		Value	Unit
t_{gt}	Gate-controlled Turn-on time	$V_{AA} = 30\text{ V}$, $R_L = 6\ \Omega$, $R_{GK(eff)} = 100\ \Omega$, $V_{in} = 20\text{ V}$	0.8	μs
t_q	Circuit-communicated Turn-off time	$V_{AA} = 30\text{ V}$, $R_L = 6\ \Omega$, $I_{RM} \approx 10\text{ A}$	11	
$R_{\theta JC}$	Junction to case thermal resistance		≤ 3	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Junction to free air thermal resistance		≤ 62.5	

ELECTRICAL CHARACTERISTICS

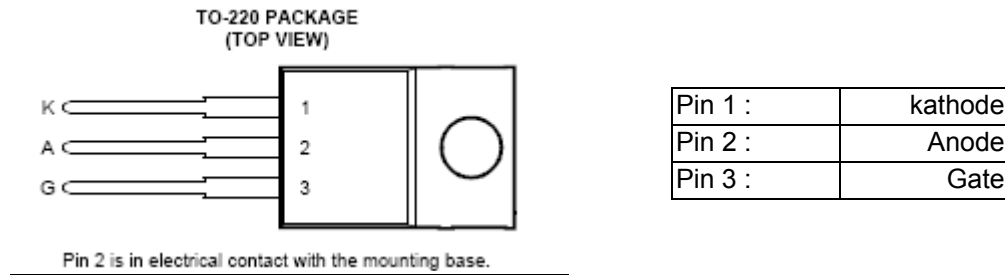
TC=25°C unless otherwise noted

Symbol	Ratings	Test Condition(s)	Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \text{Rated } V_{DRM}$, $R_{GK} = 1\text{ k}\Omega$ $T_C = 110^{\circ}\text{C}$	-	-	2	mA
I_{RRM}	Repetitive peak reverse current	$V_R = \text{Rated } V_{RRM}$, $I_G = 0$ $T_C = 110^{\circ}\text{C}$	-	-	2	mA
I_{GT}	Gate trigger current	$V_{AA} = 6\text{ V}$, $R_L = 100\ \Omega$ $t_{p(g)} \geq 20\mu\text{s}$	-	5	20	mA
V_{GT}	Gate trigger voltage	$V_{AA} = 6\text{ V}$, $R_L = 100\ \Omega$ $R_{GK} = 1\text{ k}\Omega$, $t_{p(g)} \geq 20\mu\text{s}$ $T_C = -40^{\circ}\text{C}$	-	-	2.5	V
		$V_{AA} = 6\text{ V}$, $R_L = 100\ \Omega$ $R_{GK} = 1\text{ k}\Omega$, $t_{p(g)} \geq 20\mu\text{s}$	-	0.8	1.5	
		$V_{AA} = 6\text{ V}$, $R_L = 100\ \Omega$ $R_{GK} = 1\text{ k}\Omega$, $t_{p(g)} \geq 20\mu\text{s}$ $T_C = 110^{\circ}\text{C}$	0.2	-	-	
I_H	Holding current	$V_{AA} = 6\text{ V}$, $R_{GK} = 1\text{ k}\Omega$ initiating $I_T = 100\text{ mA}$	-	-	40	mA
		$V_{AA} = 6\text{ V}$, $R_{GK} = 1\text{ k}\Omega$ initiating $I_T = 100\text{ mA}$ $T_C = -40^{\circ}\text{C}$	-	-	70	
V_{TM}	Peak on-state voltage	$I_{TM} = 8\text{ A}$ (see Note6)	-	-	1.7	V
dv/dt	Critical rate of rise of off-state voltage	$V_D = \text{Rated } V_D$ $T_C = 110^{\circ}\text{C}$	-	100	-	V/ μs



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PINNING



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