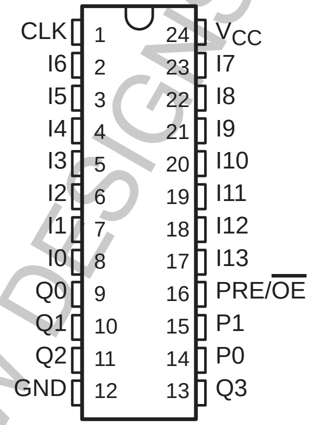
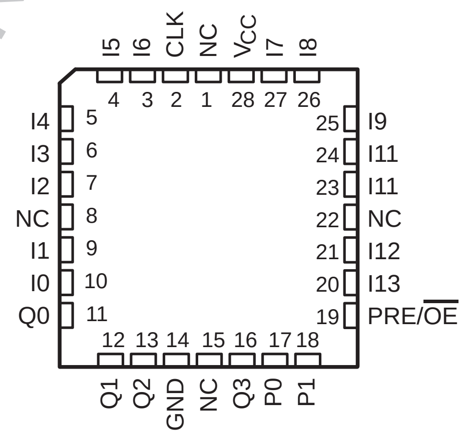
- **Programmable Asynchronous Preset or Output Control**
- **Power-On Preset of All Flip-Flops**
- **8-Bit Internal State Register With 4-Bit Output Register**
- **Power Dissipation . . . 600 mW Typical**
- **Functionally Equivalent to, but Faster Than 82S167A†**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TIB82S167BC is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 12 pairs of sum terms (OR terms). The product and sum terms are used to control the 8-bit internal state register and the 4-bit output register.

The outputs of the internal state register (P0–P7) are fed back and combined with the 14 inputs (I0–I13) to form the AND array. In addition the first two bits of the internal state register (P0–P1) are brought off-chip to allow the output register to be extended to 6 bits if desired. A single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as inputs to the AND array.

The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high during power up. PRE/$\overline{\text{OE}}$ can be used as PRE to preset both registers or, by blowing the proper fuse, be converted to an output control function, $\overline{\text{OE}}$.

The TIB82S167BC is characterized for operation from 0°C to 75°C.

NOT RECOMMENDED FOR NEW DESIGNS

† Power-up preset and asynchronous preset functions are not identical to 82S167A.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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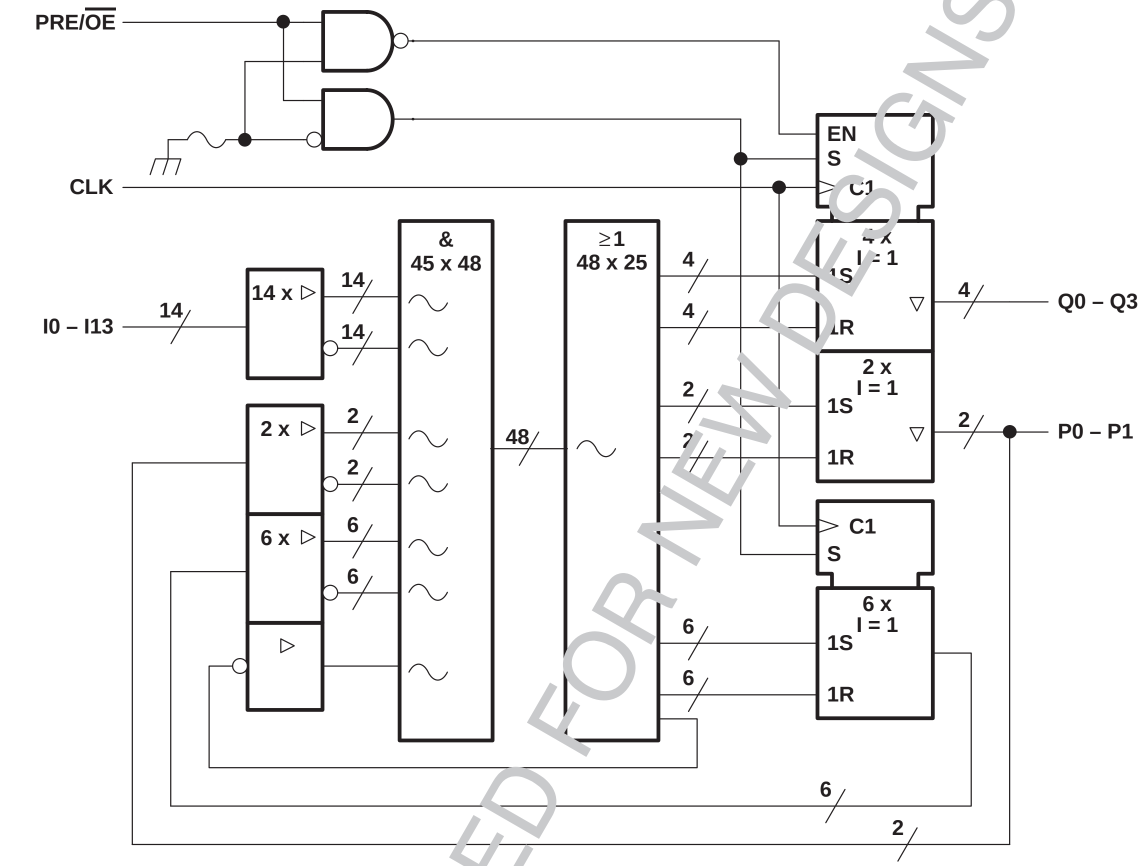
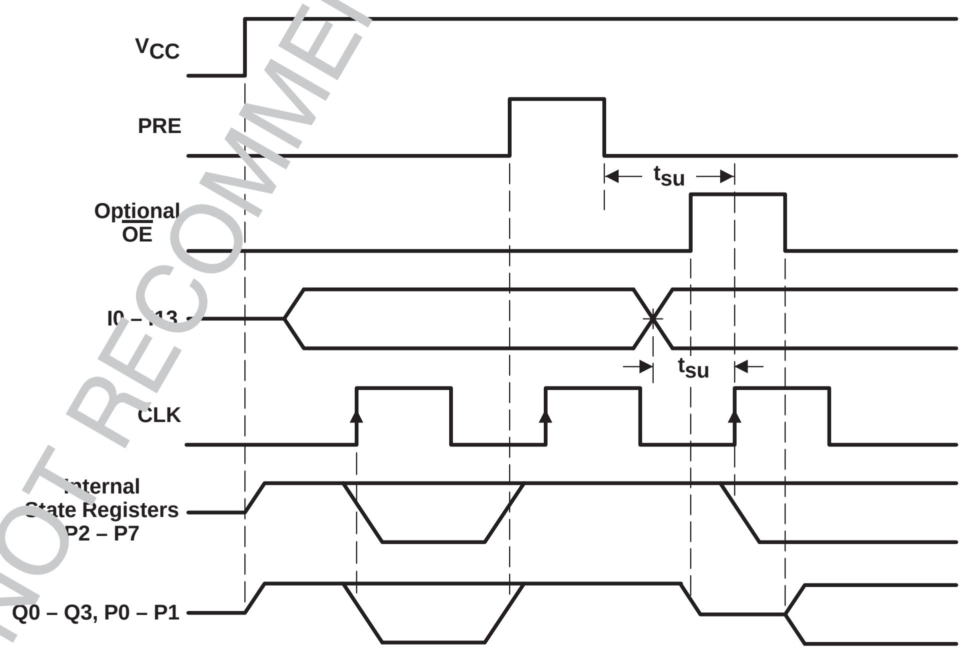
functional block diagram (positive logic)



denotes fused inputs

timing diagram



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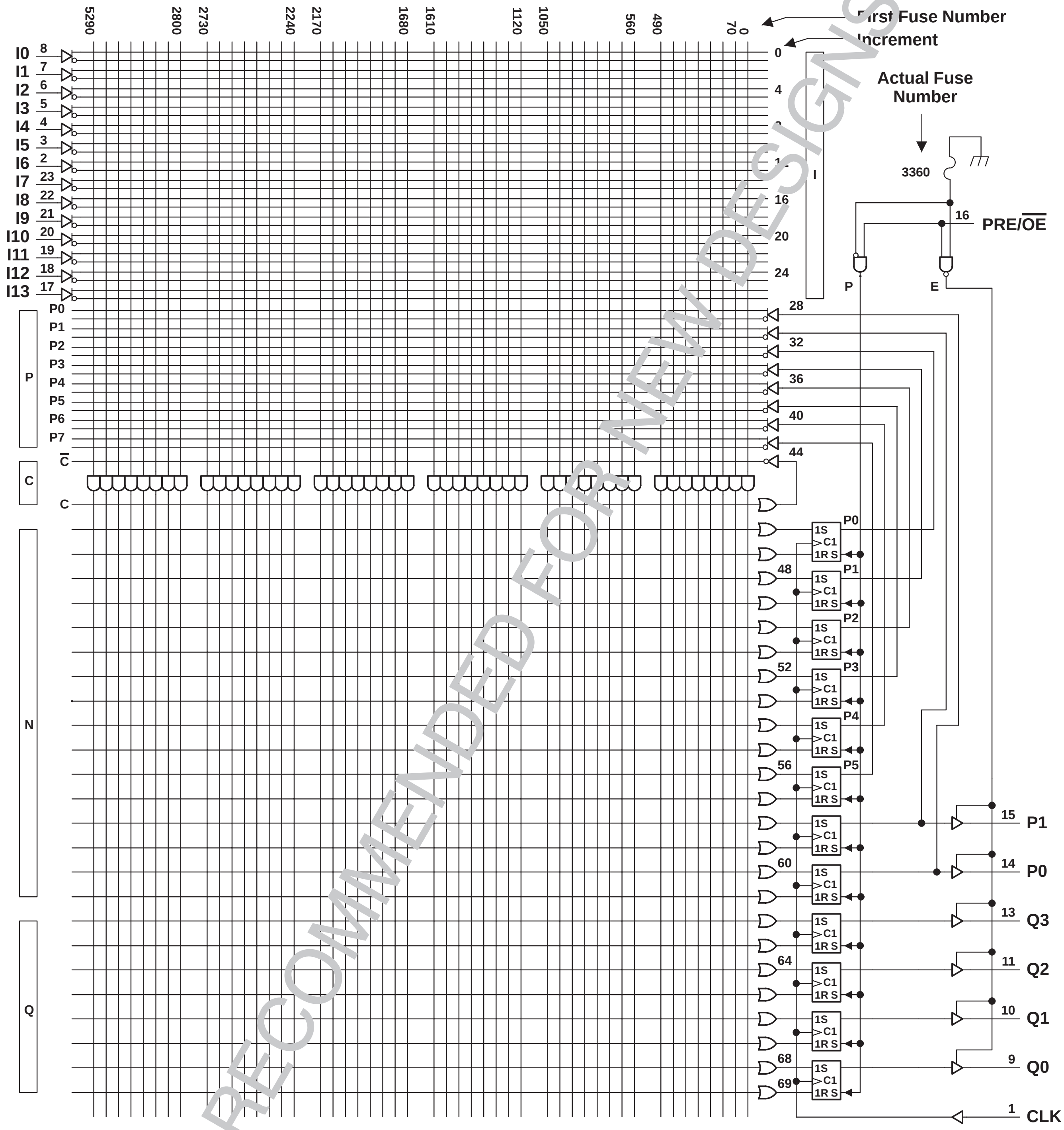
logic diagram (positive logic)



NOTES: 1. All AND gate inputs with a blown link float to the high level.
2. All OR gate inputs with a blown link float to the low level.
3. Fuse numbers = First fuse number + Increment

NOT RECOMMENDED FOR NEW DESIGNS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . 7 V
Input voltage (see Note 4) . . . . 5.5 V
Voltage applied to disabled output (see Note 4) . . . . 5.5 V
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . –65°C to 150°C

NOTE 4: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array ‡	0		50	MHz
		1 thru 48 product terms with C-array	0		30	
t_w	Pluse duration	Clock high or low	10			ns
		Preset	15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	15			ns
		With C-array	30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		8			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

† The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡ The C-array is the single sum term that is complemented and fed back to the AND array.
§ After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

NOT RECOMMENDED FOR NEW DESIGNS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.37	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			25	μA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.25	mA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} = 5.25 V, PRE/$\overline{OE}$ at GND,	V_I = 4.5 V, Outputs open		90	160	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array		R1 = 500 Ω, R2 = 500 Ω, See Figure 5	50	70		MHz
	With C array			30	45		
t_{pd}	CLK↑	Q			10	15	ns
t_{pd}	PRE↑	Q			8	20	ns
t_{pd}	V_{CC}↑	Q			0	10	ns
t_{en}	$\overline{OE}$↓	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			5	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions hace been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
§ f_{max} is independent of the internal programmed configuration and the number of product terms used.

programming information

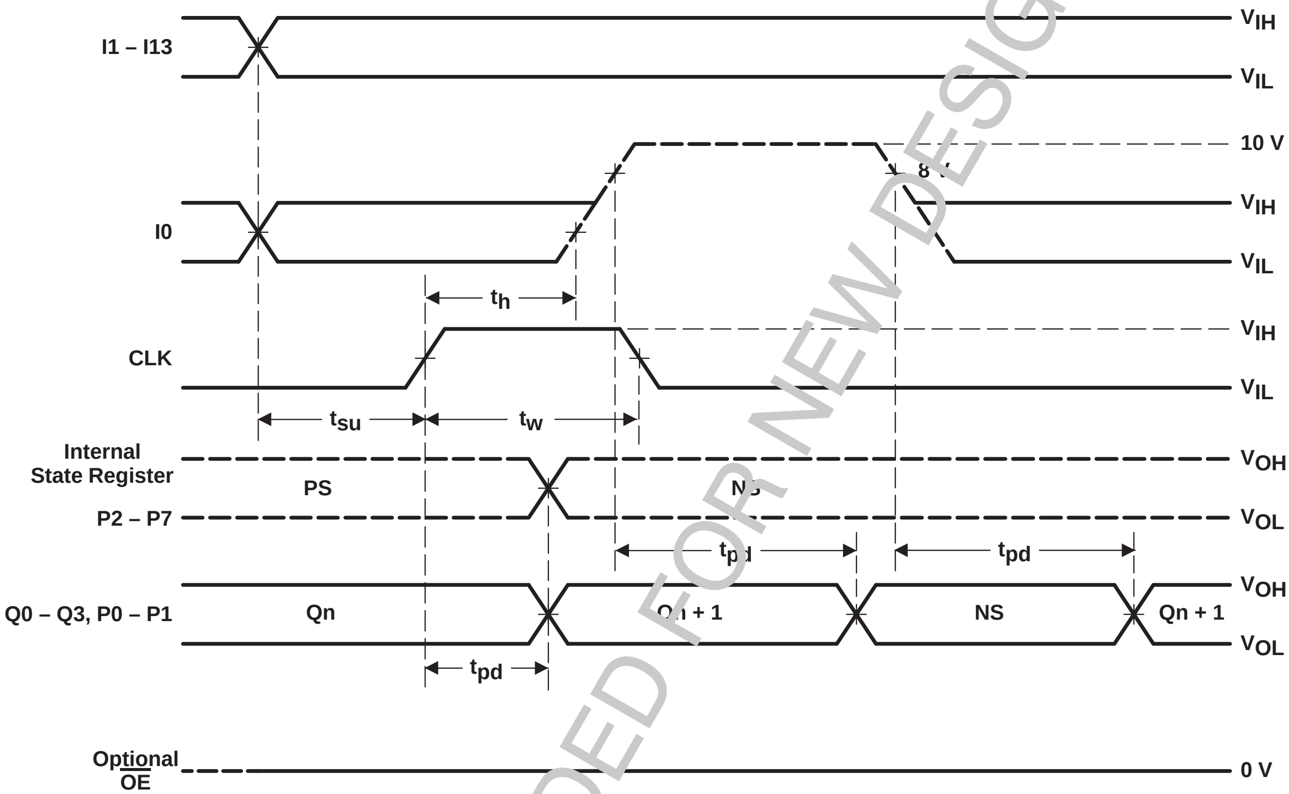
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

NOT RECOMMENDED FOR NEW DESIGNS

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 is held at 10 V, the state register bits P2–P7 will appear at the Q0–Q3 and P0–P1 outputs. The contents of the output registers, Q0–Q3, P0–P1 remain unchanged.



PS = Present State, NS = Next State

Figure 1. Diagnostic Waveforms

NOT RECOMMENDED FOR NEW DESIGNS

test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown in Table 1. Testing is accomplished by connecting Q0–Q3 to I10–I13, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in Figure 2. Product lines 48 and 49 must be deleted during user programming to avoid interference with the programmed logic function.

Table 1. Test Array Program

PRODUCT LINE	AND																								OR (OPTION PRE/$\overline{OE}$ H)													
	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	X	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	–	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

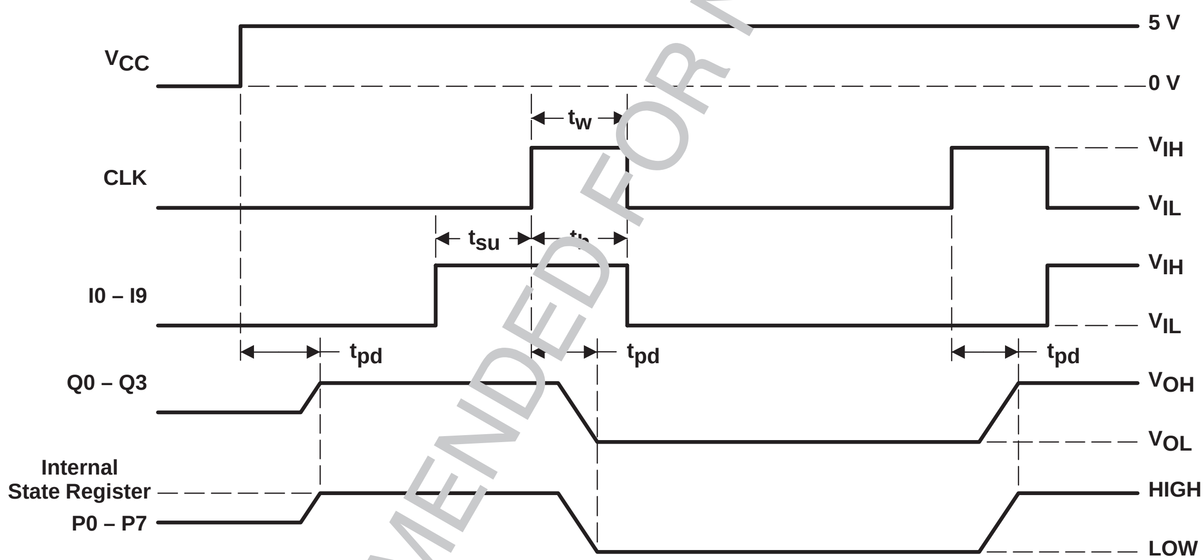


Figure 2. Test Array Waveforms

Table 2. Test Array Deleted

PRODUCT LINE	AND																								OR (OPTION PRE/$\overline{OE}$ H)													
	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	–	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
49	–	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–

X = Fuse intact – = Fuse blown

NOT RECOMMENDED FOR NEW DESIGNS

TIB82S167B, 82S167A COMPARISON

The Texas Instruments TIB82S167B is a 14 × 48 × 6 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S167A. However, the TIB82S167B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S167B differs from the 82S167A in speed and in the preset recovery function.

The TIB82S167B is a high-speed version of the original 82S167A. The TIB82S167B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S167A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S167B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraph.

The TIB82S167B and the 82S167A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S167A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 3. The Texas Instruments TIB82S167B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 4.

The TIB82S167B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S167B be used in new designs. ***However, if the TIB82S167B is used to replace the 82S167A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

Table 3. Speed Differences

PARAMETER	82S167A SIGNETICS	TIB82S167B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

NOT RECOMMENDED FOR NEW DESIGNS

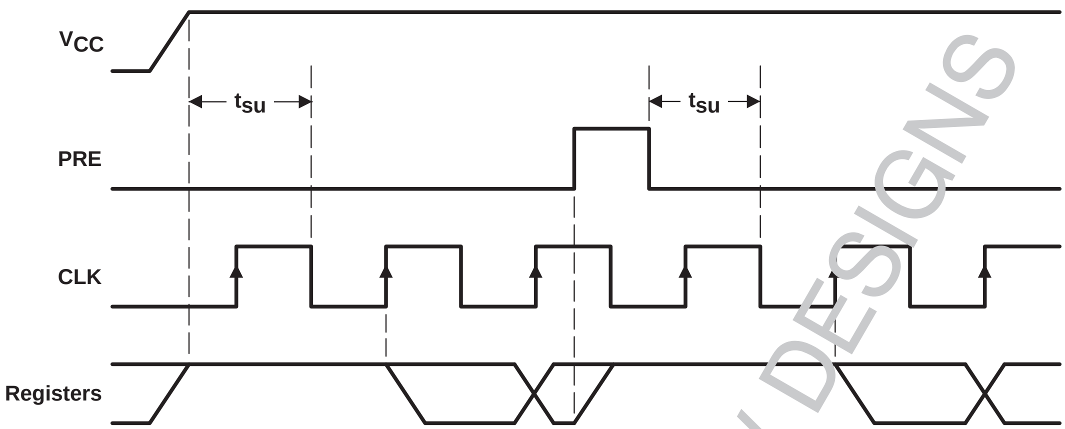


Figure 3. 82S167A Preset Recovery Operation

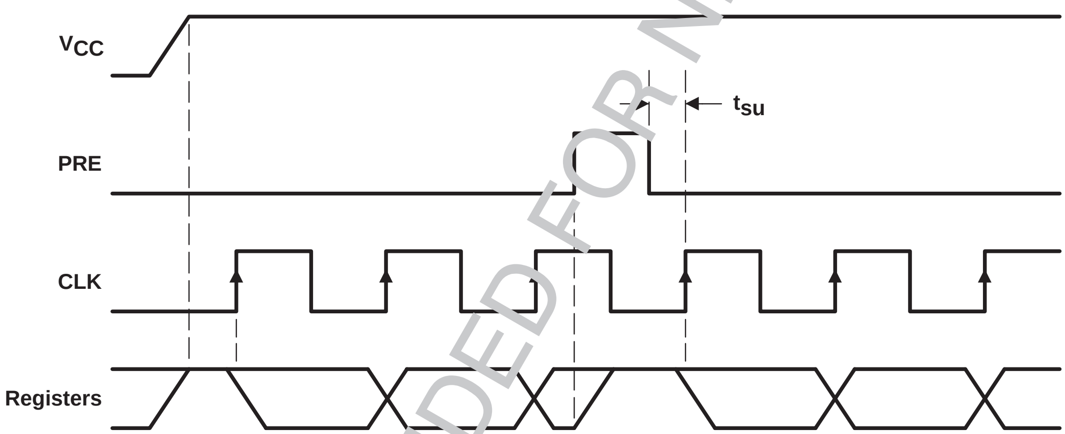
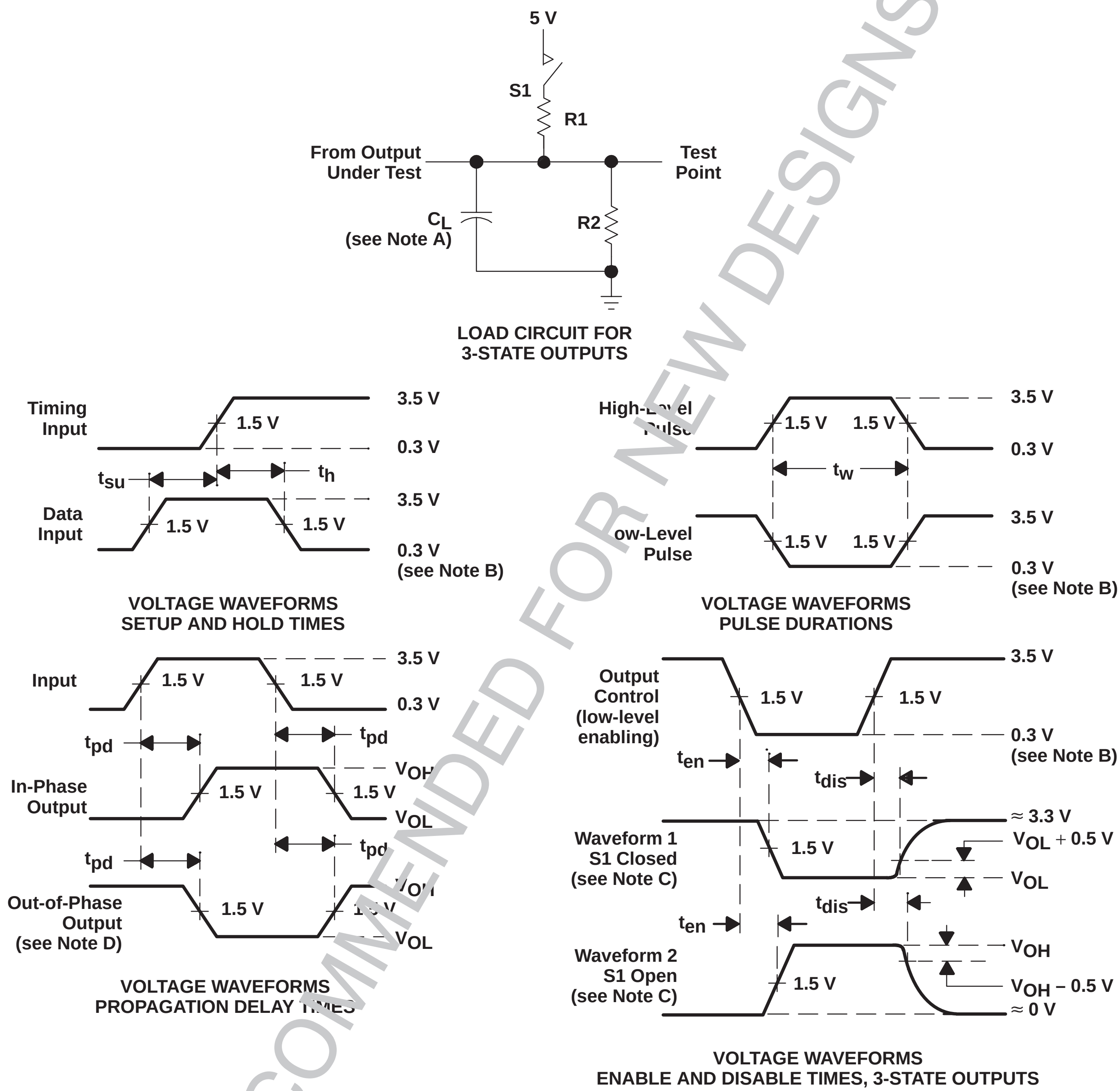


Figure 4. TIB82S167B Preset Recovery Operation

NOT RECOMMENDED FOR NEW DESIGNS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 5. Load Circuit and Voltage Waveforms

NOT RECOMMENDED FOR NEW DESIGNS

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