THS4509-Q1 Wideband Low-Noise Low-Distortion Fully Differential Amplifier

1 Features

- Qualified for Automotive Applications
- Fully Differential Architecture
- Centered Input Common-Mode Range
- Minimum Gain of 2 V/V (6 dB)
- Bandwidth: 1900 MHz
- Slew Rate: 6600 V/μs
- 1% Settling Time: 2 ns
- HD_2: –75 dBc at 100 MHz
- HD_3: –80 dBc at 100 MHz
- OIP_2: 73 dBm at 70 MHz
- OIP_3: 37 dBm at 70 MHz
- Input Voltage Noise: 1.9 nV/√Hz (f > 10 MHz)
- Noise Figure: 17.1 dB
- Output Common-Mode Control
- Power Supply:
  - Voltage: 3 V (±1.5 V) to 5 V (±2.5 V)
  - Current: 37.7 mA
- Power-Down Capability: 0.65 mA

2 Applications

- Adaptive Cruise Control
- Blind Spot Detection
- Collision Warning
- Industrial
- 5-V Data Acquisition Systems High Linearity ADC Amplifier
- Test and Measurement

3 Description

The THS4509-Q1 is a wideband, fully differential operational amplifier designed for 5-V data-acquisition systems. It has very low noise at 1.9 nV/√Hz, and extremely low harmonic distortion of –75-dBc HD_2 and –80-dBc HD_3 at 100 MHz with 2 Vpp, G = 10 dB, and 1-kΩ load. Slew rate is very high at 6600 V/μs and with settling time of 2 ns to 1% (2-V step), it is ideal for pulsed applications. It is designed for minimum gain of 6 dB but is optimized for gain of 10 dB.

To allow for dc coupling to analog-to-digital converters (ADCs), its unique output common-mode control circuit maintains the output common-mode voltage within 3-mV offset (typical) from the set voltage, when set within 0.5 V of mid-supply, with less than 4-mV differential offset voltage. The common-mode set point is set to mid-supply by internal circuitry, which may be overdriven from an external source.

The input and output are optimized for best performance with their common-mode voltages set to mid-supply. Along with high-performance at low power-supply voltage, this makes for extremely high-performance single-supply 5-V data-acquisition systems.

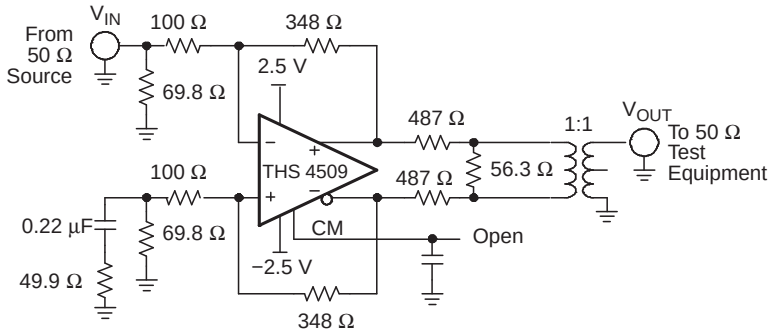
The THS4509-Q1 is offered in a quad 16-pin leadless QFN package (RGT) and is characterized for operation over the full automotive temperature range from –40°C to 125°C.

Device Information(1)

PART NUMBER	MINIMUM GAIN	COMMON-MODE RANGE OF INPUT
THS4509-Q1	6 dB	0.75 V to 4.25 V

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

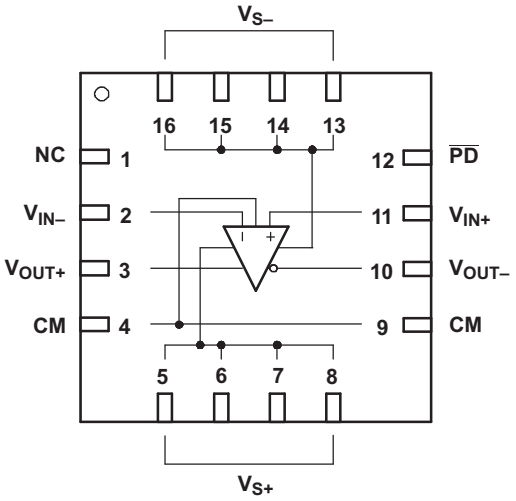
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2008) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

RGT Package
16-Pin QFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CM	4,9	I	Common-mode voltage input
NC	1	—	No internal connection
$\overline{PD}$	12	I	Power down, $\overline{PD}$ = logic low puts part into low-power mode, $\overline{PD}$ = logic high or open for normal operation
V_{IN-}	2	I	Inverting amplifier input
V_{IN+}	11	I	Noninverting amplifier input
V_{OUT-}	10	O	Inverted amplifier output
V_{OUT+}	3	O	Noninverted amplifier output
V_{S-}	13, 14, 15, 16	I	Negative amplifier power supply input
V_{S+}	5, 6, 7, 8	I	Positive amplifier power-supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		6	V
V_I	Input voltage	$-V_S$	$+V_S$	
V_{ID}	Differential input voltage		4	V
I_O	Output current(2)		200	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The THS4509-Q1 incorporates a (QFN) exposed thermal pad on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the QFN thermally enhanced package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
		Machine Model (MM)	±100	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Total supply voltage	3		5	V
Operating temperature, T_J	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS4509-Q1 RGT (QFN) 16-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V

test conditions (unless otherwise noted): $V_{S+} = 2.5$ V, $V_{S-} = -2.5$ V, G = 10 dB, CM = open, $V_O = 2$ Vpp, $R_F = 349$ Ω, $R_L = 200$ Ω differential, $T_A = 25°C$, single-ended input, differential output, input and output referenced to mid-supply

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE							
Small-signal bandwidth	G = 6 dB, V_O = 100 mVpp		C		2		GHz
	G = 10 dB, V_O = 100 mVpp				1.9		
	G = 14 dB, V_O = 100 mVpp				600		MHz
	G = 20 dB, V_O = 100 mVpp				275		
Gain-bandwidth product	G = 20 dB				3		GHz
Bandwidth for 0.1-dB flatness	G = 10 dB, V_O = 2 Vpp				300		MHz
Large-signal bandwidth	G = 10 dB, V_O = 2 Vpp				1.5		GHz
Slew rate (differential)	2-V step				6600		V/µs
Rise time	2-V step				0.5		ns
Fall time	2-V step				0.5		ns
Settling time to 1%	2-V step				2		ns
Settling time to 0.1%	2-V step				10		ns
Second-order harmonic distortion	f = 10 MHz				–104		dBc
	f = 50 MHz				–80		
	f = 100 MHz				–68		
Third-order harmonic distortion	f = 10 MHz				–108		dBc
	f = 50 MHz				–92		
	f = 100 MHz				–81		
Second-order intermodulation distortion	200-kHz tone spacing, R_L = 499 Ω	f_C = 70 MHz			–78		dBc
		f_C = 140 MHz			–64		
Third-order intermodulation distortion	200-kHz tone spacing, R_L = 499 Ω	f_C = 70 MHz			–95		dBc
		f_C = 140 MHz			–78		
Second-order output intercept point	200-kHz tone spacing, R_L = 100 Ω, referenced to 50-Ω output	f_C = 70 MHz			78		dBm
		f_C = 140 MHz			58		
Third-order output intercept point	200-kHz tone spacing, R_L = 100 Ω, referenced to 50-Ω output	f_C = 70 MHz			43		dBm
		f_C = 140 MHz			38		
1-dB compression point	f_C = 70 MHz				12.2		dBm
	f_C = 140 MHz				10.8		
Noise figure	50-Ω system, 10 MHz				17.1		dB
Input voltage noise	f > 10 MHz				1.9		nV/√Hz
Input current noise	f > 10 MHz				2.2		pA/√Hz
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})			C		68		dB
Input offset voltage	T_A = 25°C		A		1	4	mV
	T_A = –40°C to 125°C				1	5	mV
Average input offset voltage drift	T_A = –40°C to 125°C		B		2.6		µV/°C
Input bias current	T_A = 25°C		A		8	15.5	µA
	T_A = –40°C to 125°C				8	18.5	
Average input bias current drift	T_A = –40°C to 125°C		B		20		nA/°C
Input offset current	T_A = 25°C		A		1.6	3.6	µA
	T_A = –40°C to 125°C				1.6	7	
Average input offset current drift	T_A = –40°C to 125°C		B		4		nA/°C

(1) Test levels: A = 100% tested at 25°C, overtemperature limits by characterization and simulation; B = Limits set by characterization and simulation; C = Typical value only for information.

Electrical Characteristics: $V_{S+} - V_{S-} = 5$ V (continued)

test conditions (unless otherwise noted): $V_{S+} = 2.5$ V, $V_{S-} = -2.5$ V, G = 10 dB, CM = open, $V_O = 2$ Vpp, $R_F = 349\ \Omega$, $R_L = 200\ \Omega$ differential, $T_A = 25°C$, single-ended input, differential output, input and output referenced to mid-supply

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
INPUT							
Common-mode input range high			B		1.75		V
Common-mode input range low					–1.75		
Common-mode rejection ratio					90		dB
Differential input impedance			C		1.35 || 1.77		MΩ || pF
Common-mode input impedance			C		1.02 || 2.26		MΩ || pF
OUTPUT							
Maximum output voltage high	Each output with 100 Ω to mid-supply	$T_A = 25°C$	A	1.2	1.4		V
		$T_A = –40°C$ to 125°C		1.1	1.4		
Minimum output voltage low	Each output with 100 Ω to mid-supply	$T_A = 25°C$			–1.4	–1.2	V
		$T_A = –40°C$ to 125°C			–1.4	–1.1	
Differential output voltage swing			C	4.8	5.6		V
	$T_A = –40°C$ to 125°C			4.4			
Differential output current drive	$R_L = 10\ \Omega$				96		mA
Output balance error	$V_O = 100$ mV, f = 1 MHz				–49		dB
Closed-loop output impedance	f = 1 MHz				0.3		Ω
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-signal bandwidth			C		700		MHz
Slew rate					110		V/µs
Gain					1		V/V
Output common-mode offset from CM input	1.25 V < CM < 3.5 V				5		mV
CM input bias current	1.25 V < CM < 3.5 V				±40		µA
CM input voltage range					–1.5 to 1.5		V
CM input impedance					23 || 1		kΩ || pF
CM default voltage					0		V
POWER SUPPLY							
Specified operating voltage			C	3	5	5.25	V
Maximum quiescent current	$T_A = 25°C$		A		37.7	40.9	mA
	$T_A = –40°C$ to 125°C				37.7	41.9	
Minimum quiescent current	$T_A = 25°C$			34.5	37.7		mA
	$T_A = –40°C$ to 125°C			33.5	37.7		
Power-supply rejection (±PSRR)			C		90		dB
POWER DOWN	Referenced to V_{S-}						
Enable voltage threshold	Assured *on* above 2.1 V + V_{S-}		C		>2.1 + V_{S-}		V
Disable voltage threshold	Assured *off* below 0.7 V + V_{S-}				<0.7 + V_{S-}		V
Powerdown quiescent current	$T_A = 25°C$		A		0.65	0.9	mA
	$T_A = –40°C$ to 125°C				0.65	1	
Input bias current	$\overline{PD} = V_{S-}$		C		100		µA
Input impedance					50 || 2		kΩ || pF
Turn-on time delay	Measured to output on				55		ns
Turn-off time delay	Measured to output off				10		µs

6.6 Electrical Characteristics: $V_{S+} - V_{S-} = 3$ V

test conditions (unless otherwise noted): $V_{S+} = 1.5$ V, $V_{S-} = -1.5$ V, G = 10 dB, CM = open, $V_O = 1$ Vpp, $R_F = 349\ \Omega$, $R_L = 200\ \Omega$ differential, $T_A = 25°C$, single-ended input, differential output, input and output referenced to mid-supply

PARAMETER	TEST CONDITIONS		TEST LEVEL (1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE							
Small-signal bandwidth	G = 6 dB, V_O = 100 mVpp		C		1.9		GHz
	G = 10 dB, V_O = 100 mVpp				1.6		
	G = 14 dB, V_O = 100 mVpp				625		MHz
	G = 20 dB, V_O = 100 mVpp				260		
Gain-bandwidth product	G = 20 dB				3		GHz
Bandwidth for 0.1-dB flatness	G = 10 dB, V_O = 1 Vpp				400		MHz
Large-signal bandwidth	G = 10 dB, V_O = 1 Vpp				1.5		GHz
Slew rate (differential)	2-V step				3500		V/µs
Rise time	2-V step				0.25		ns
Fall time	2-V step				0.25		ns
Settling time to 1%	2-V step				1		ns
Settling time to 0.1%	2-V step				10		ns
Second-order harmonic distortion	f = 10 MHz				–107		dBc
	f = 50 MHz				–83		
	f = 100 MHz				–60		
Third-order harmonic distortion	f = 10 MHz				–87		dBc
	f = 50 MHz				–65		
	f = 100 MHz				–54		
Second-order intermodulation distortion	200-kHz tone spacing, R_L = 499 Ω	f_C = 70 MHz			–77		dBc
		f_C = 140 MHz			–54		
Third-order intermodulation distortion	200-kHz tone spacing, R_L = 499 Ω	f_C = 70 MHz			–77		dBc
		f_C = 140 MHz			–62		
Second-order output intercept point	200-kHz tone spacing R_L = 100 Ω	f_C = 70 MHz			72		dBm
		f_C = 140 MHz			52		
Third-order output intercept point	200-kHz tone spacing R_L = 100 Ω	f_C = 70 MHz			38.5		dBm
		f_C = 140 MHz			30		
1-dB compression point	f_C = 70 MHz				2.2		dBm
	f_C = 140 MHz				0.25		
Noise figure	50-Ω system, 10 MHz				17.1		dB
Input voltage noise	f > 10 MHz				1.9		nV/√Hz
Input current noise	f > 10 MHz				2.2		pA/√Hz
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})			C		68		dB
Input offset voltage	T_A = 25°C				1		mV
Average input offset voltage drift	T_A = –40°C to 125°C				2.6		µV/°C
Input bias current	T_A = 25°C				6		µA
Average input bias current drift	T_A = –40°C to 125°C				20		nA/°C
Input offset current	T_A = 25°C				1.6		µA
Average input offset current drift	T_A = –40°C to 125°C				4		nA/°C

(1) Test levels: A = 100% tested at 25°C, overtemperature limits by characterization and simulation; B = Limits set by characterization and simulation; C = Typical value only for information.

Electrical Characteristics: $V_{S+} - V_{S-} = 3$ V (continued)

test conditions (unless otherwise noted): $V_{S+} = 1.5$ V, $V_{S-} = -1.5$ V, G = 10 dB, CM = open, $V_O = 1$ Vpp, $R_F = 349\ \Omega$, $R_L = 200\ \Omega$ differential, $T_A = 25°C$, single-ended input, differential output, input and output referenced to mid-supply

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
INPUT							
Common-mode input range high			B		0.75		V
Common-mode input range low					–0.75		V
Common-mode rejection ratio					80		dB
Differential input impedance			C		1.35 || 1.77		MΩ || pF
Common-mode input impedance			C		1.02 || 2.26		MΩ || pF
OUTPUT							
Maximum output voltage high	Each output with 100 Ω to mid-supply	$T_A = 25°C$	C		0.45		V
Minimum output voltage low	Each output with 100 Ω to mid-supply	$T_A = 25°C$			–0.45		V
Differential output voltage swing					1.8		V
Differential output current drive	$R_L = 10\ \Omega$				50		mA
Output balance error	$V_O = 100$ mV, f = 1 MHz				–49		dB
Closed-loop output impedance	f = 1 MHz				0.3		Ω
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-signal bandwidth			C		570		MHz
Slew rate					60		V/µs
Gain					1		V/V
Output common-mode offset from CM input	1.25 V < CM < 3.5 V				4		mV
CM input bias current	1.25 V < CM < 3.5 V				±40		µA
CM input voltage range					–1.5 to 1.5		V
CM input impedance					20 || 1		kΩ || pF
CM default voltage					0		V
POWER SUPPLY							
Specified operating voltage			C		3		V
Quiescent current	$T_A = 25°C$		A		34.8		mA
Power-supply rejection (±PSRR)			C		70		dB
POWER DOWN	Referenced to V_{S-}						
Enable voltage threshold	Assured *on* above 2.1 V + V_{S-}		C		>2.1 + V_{S-}		V
Disable voltage threshold	Assured *off* below 0.7 V + V_{S-}				<0.7 + V_{S-}		V
Power-down quiescent current					0.46		mA
Input bias current	$\overline{PD} = V_{S-}$				65		µA
Input impedance					50 || 2		kΩ || pF
Turn-on time delay	Measured to output on				100		ns
Turn-off time delay	Measured to output off				10		µs

6.7 Typical Characteristics

6.7.1 Typical Characteristics: $V_{S+} - V_{S-} = 5$ V

test conditions (unless otherwise noted): V_{S+} = 2.5 V, V_{S-} = –2.5 V, CM = open, V_O = 2 Vpp, R_F = 349 Ω, R_L = 200 Ω differential, G = 10 dB, single-ended input, input and output referenced to midrail

Table 1. Table of Graphs $V_{S+} - V_{S-} = 5$ V

TYPICAL CHARACTERISTIC CURVE			FIGURE NO.
Small-signal frequency response			Figure 1
Large-signal frequency response			Figure 2
Harmonic distortion	HD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 3
	HD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 4
	HD_2, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 5
	HD_3, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 6
	HD_2, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 7
	HD_3, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 8
	HD_2, G = 10 dB	vs Output voltage	Figure 9
	HD_3, G = 10 dB	vs Output voltage	Figure 10
	HD_2, G = 10 dB	vs Common-mode output voltage	Figure 11
	HD_3, G = 10 dB	vs Common-mode output voltage	Figure 12
Intermodulation distortion	IMD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 13
	IMD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 14
	IMD_2, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 15
	IMD_3, G = 10 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 16
	IMD_2, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 17
	IMD_3, G = 14 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 18
Output intercept point	OIP_2	vs Frequency	Figure 19
	OIP_3	vs Frequency	Figure 20
0.1-dB flatness			Figure 21
S-parameters		vs Frequency	Figure 22
Transition rate		vs Output voltage	Figure 23
Transient response			Figure 24
Settling time			Figure 25
Rejection ratio		vs Frequency	Figure 26
Output impedance		vs Frequency	Figure 27
Overdrive recovery			Figure 28
Output voltage swing		vs Load resistance	Figure 29
Turn-off time			Figure 30
Turn-on time			Figure 31
Input offset voltage		vs Input common-mode voltage	Figure 32
Open-loop gain and phase		vs Frequency	Figure 33
Input referred noise		vs Frequency	Figure 34
Noise figure		vs Frequency	Figure 35
Quiescent current		vs Supply voltage	Figure 36
Power-supply current		vs Supply voltage in power-down mode	Figure 37
Output balance error		vs Frequency	Figure 38

Typical Characteristics: $V_{S+} - V_{S-} = 5$ V (continued)

Table 1. Table of Graphs $V_{S+} - V_{S-} = 5$ V (continued)

TYPICAL CHARACTERISTIC CURVE		FIGURE NO.
CM input impedance	vs Frequency	Figure 39
CM small-signal frequency response		Figure 40
CM input bias current	vs CM input voltage	Figure 41
Differential output offset voltage	vs CM input voltage	Figure 42
Output common-mode offset	vs CM input voltage	Figure 43

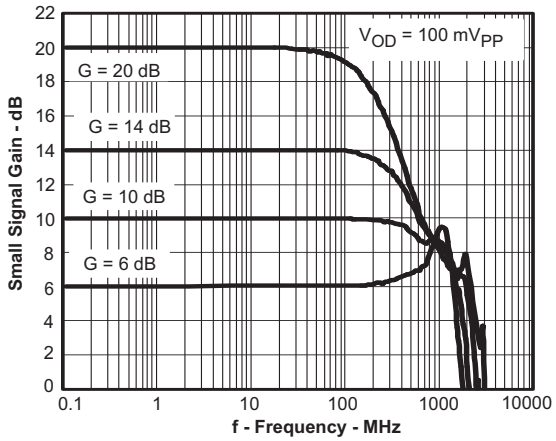


Figure 1. Small-Signal Frequency Response

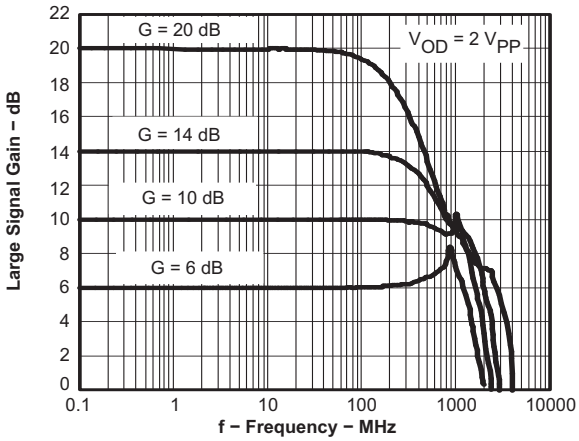


Figure 2. Large-Signal Frequency Response

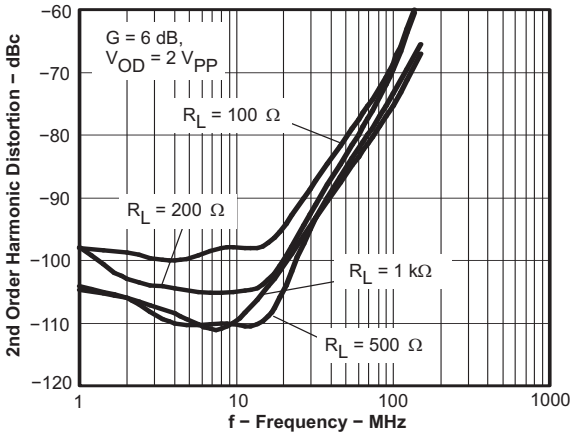


Figure 3. HD2 vs Frequency

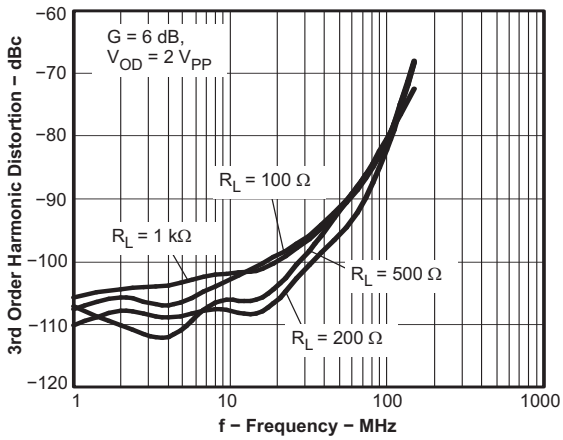


Figure 4. HD3 vs Frequency

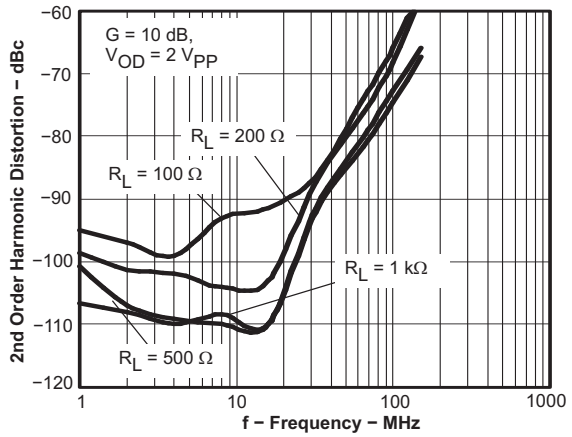


Figure 5. HD2 vs Frequency

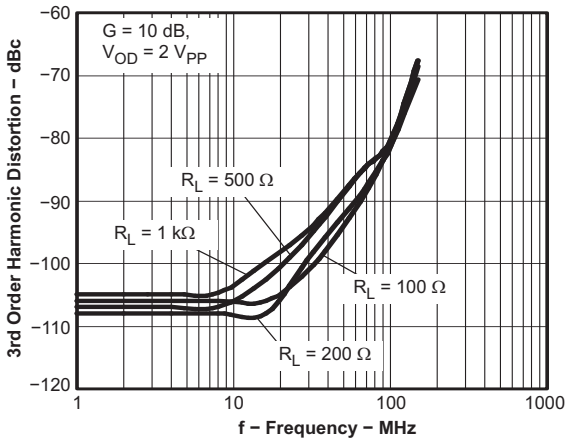


Figure 6. HD3 vs Frequency

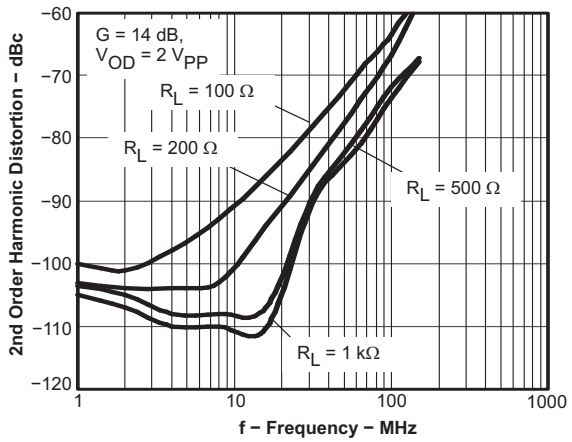


Figure 7. HD2 vs Frequency

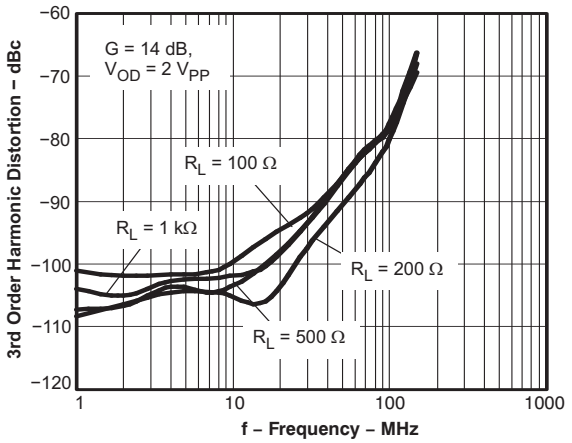


Figure 8. HD3 vs Frequency

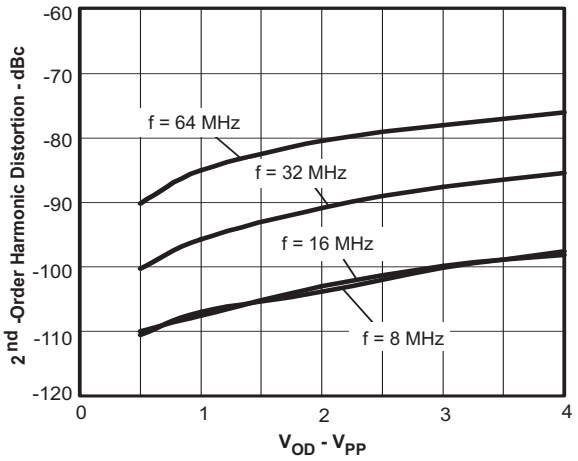


Figure 9. HD2 vs Output Voltage

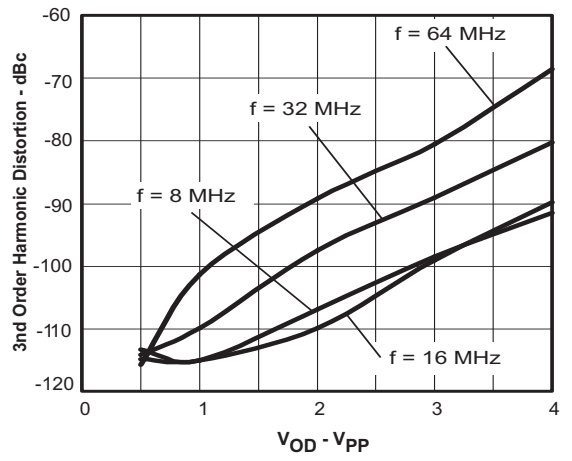


Figure 10. HD3 vs Output Voltage

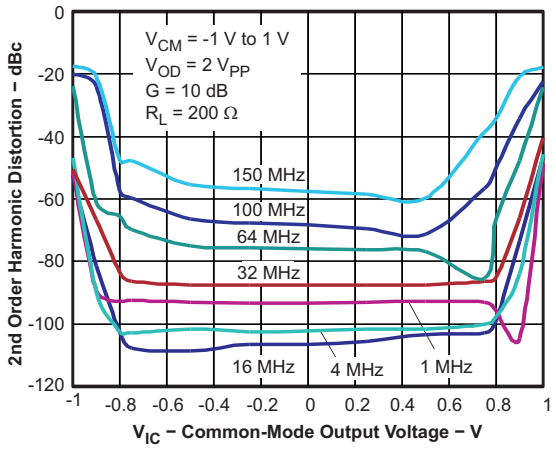


Figure 11. HD2 vs Common-Mode Output Voltage

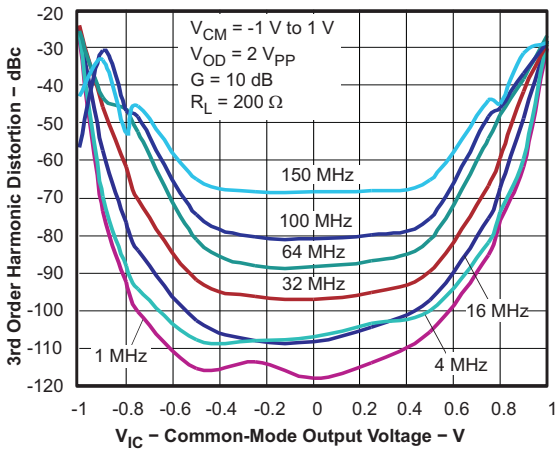


Figure 12. HD3 vs Common-Mode Output Voltage

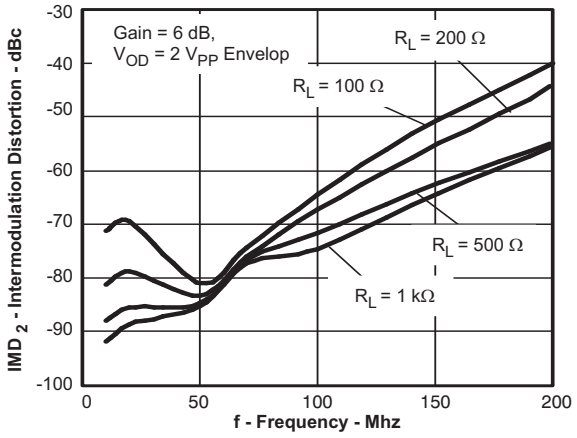


Figure 13. IMD2 vs Frequency

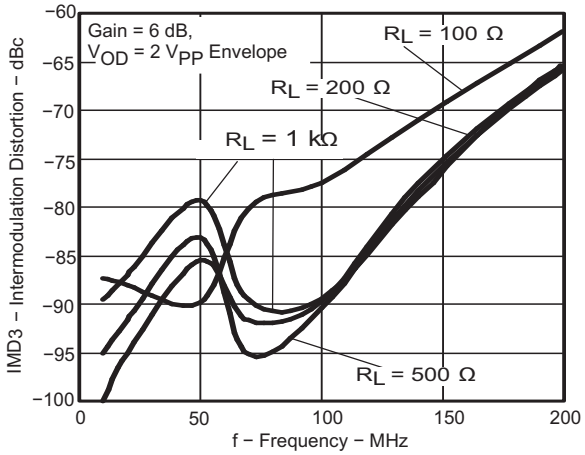


Figure 14. IMD3 vs Frequency

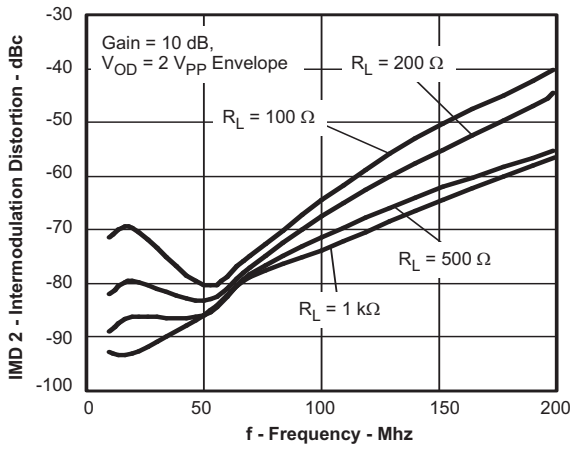


Figure 15. IMD2 vs Frequency

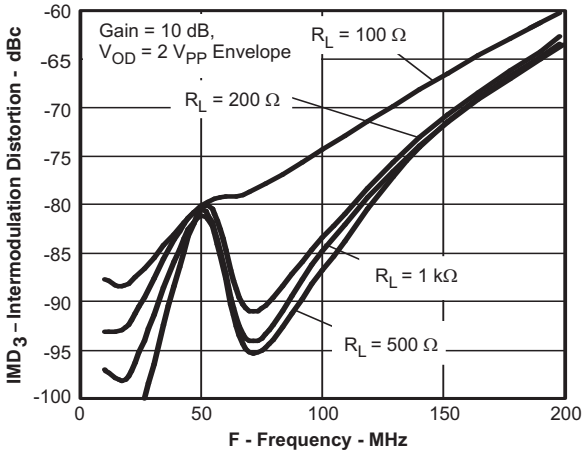


Figure 16. IMD3 vs Frequency

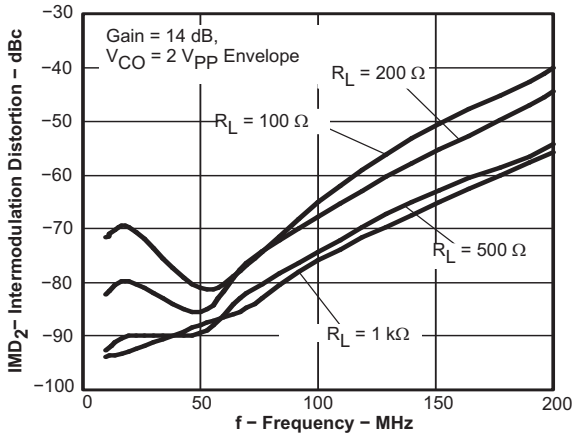


Figure 17. IMD2 vs Frequency

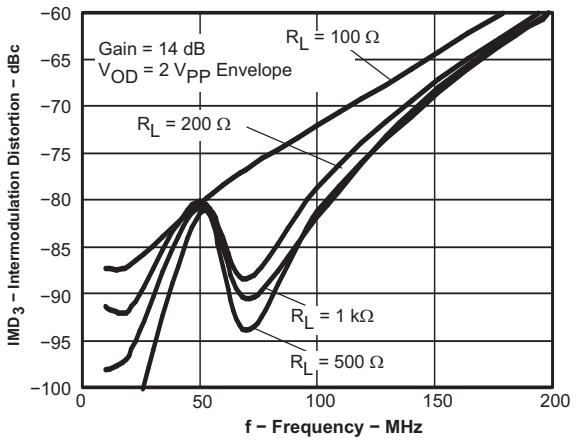


Figure 18. IMD3 vs Frequency

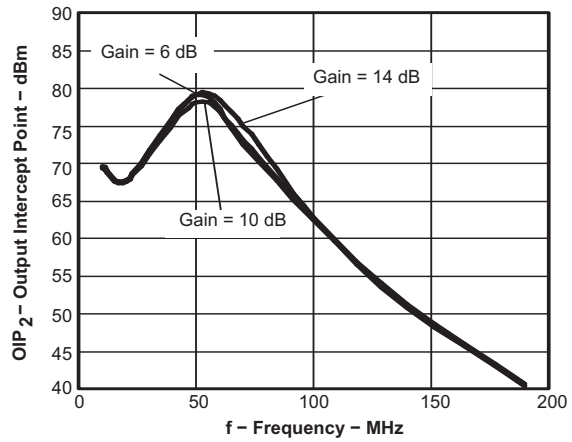


Figure 19. OIP2 vs Frequency

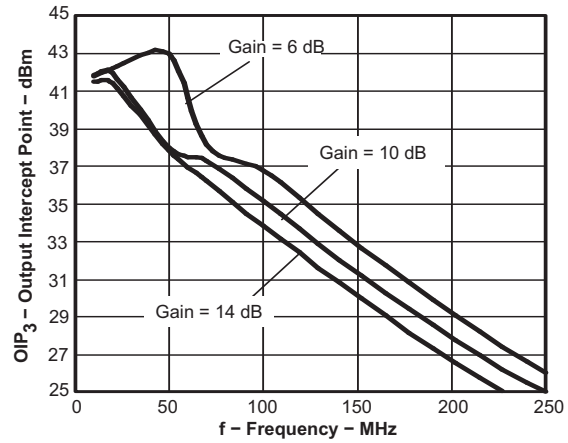


Figure 20. OIP3 vs Frequency

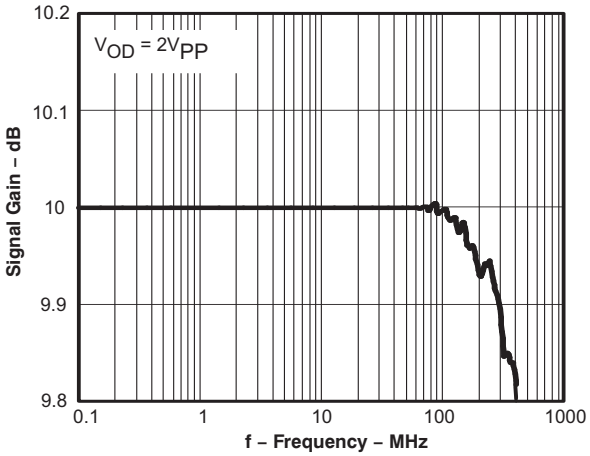


Figure 21. 0.1-dB Flatness

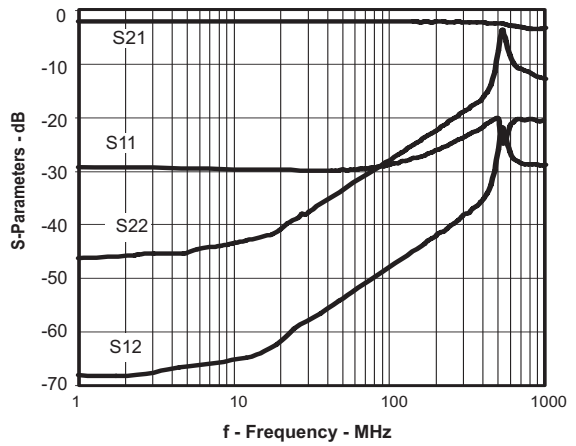


Figure 22. S-Parameters vs Frequency

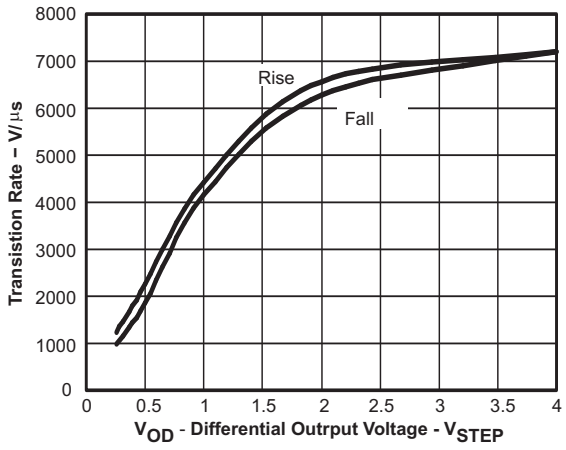


Figure 23. Transition Rate vs Output Voltage

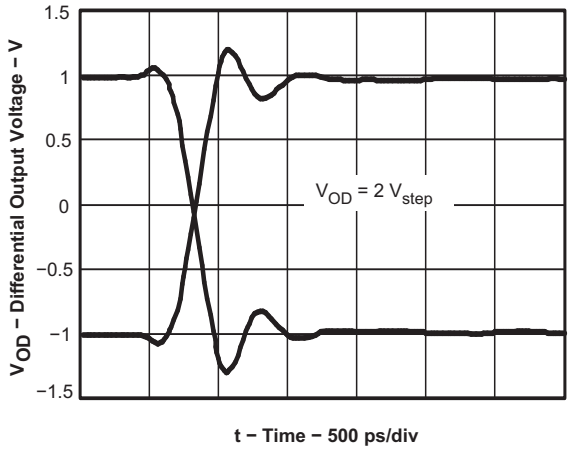


Figure 24. Transient Response

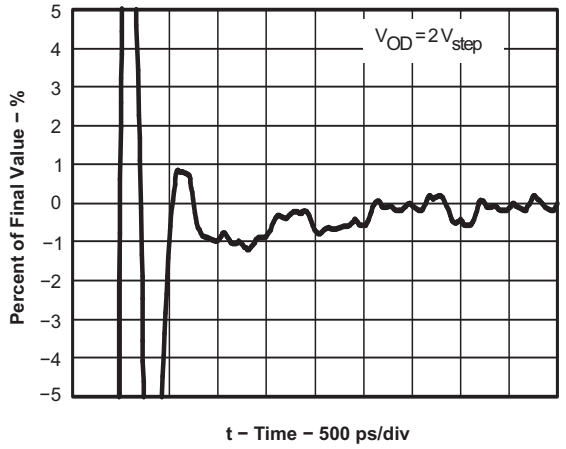


Figure 25. Settling Time

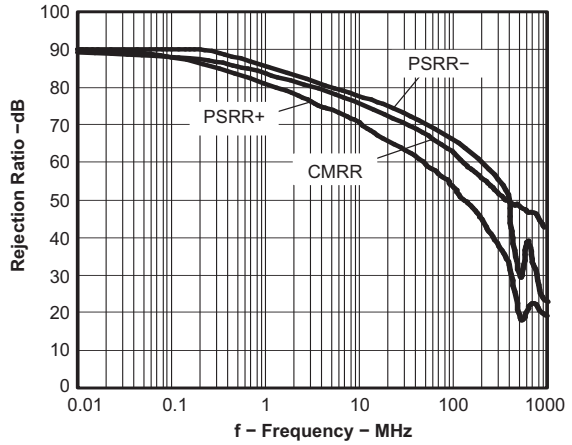


Figure 26. Rejection Ratio vs Frequency

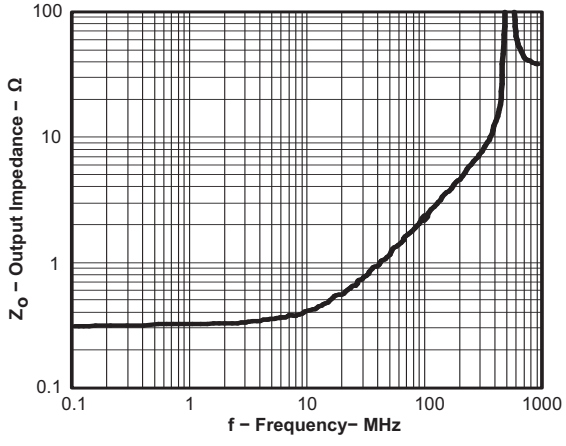


Figure 27. Output Impedance vs Frequency

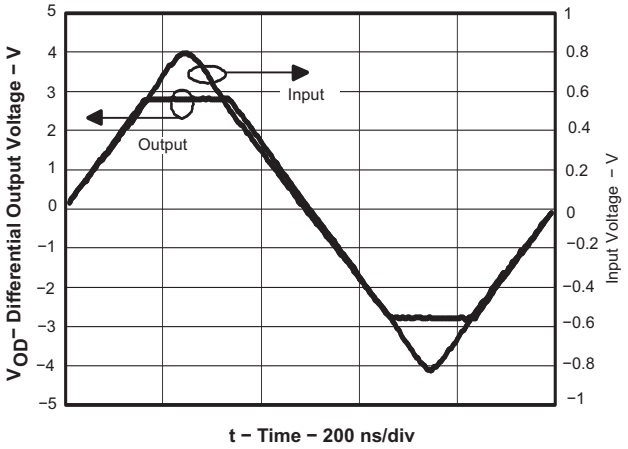


Figure 28. Overdrive Recovery

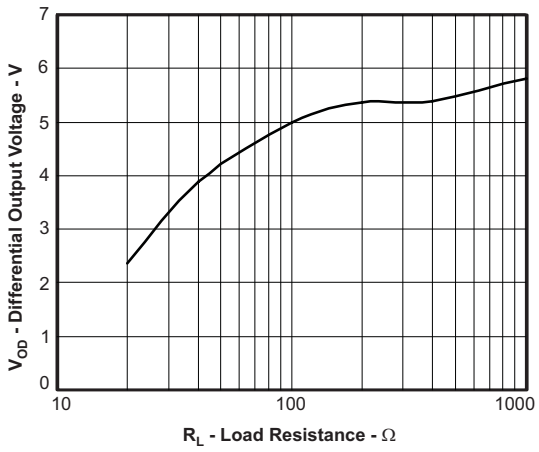


Figure 29. Output Voltage Swing vs Load Resistance

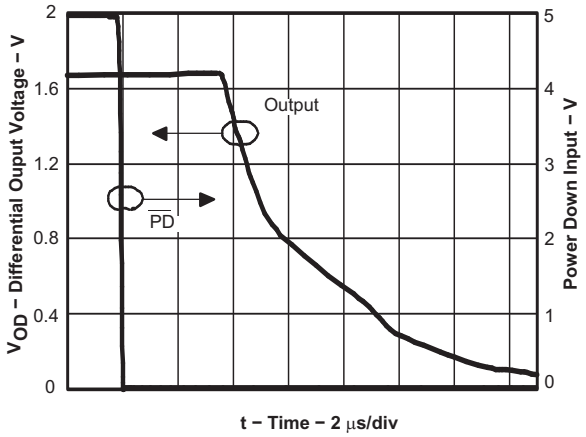


Figure 30. Turnoff Time

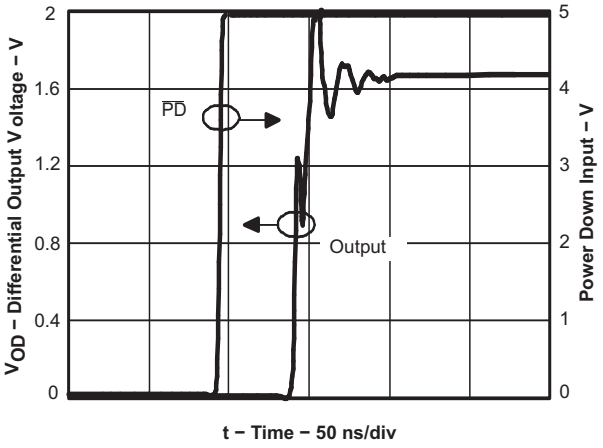


Figure 31. Turnon Time

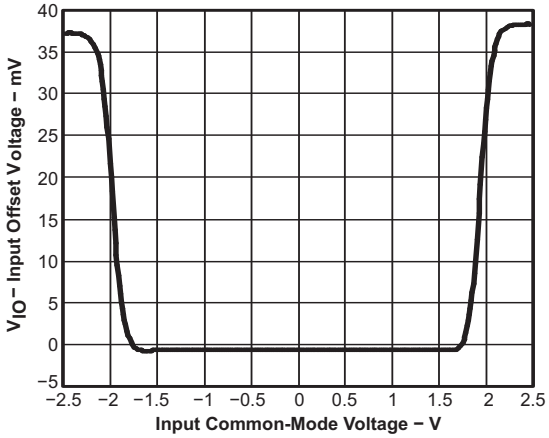


Figure 32. Input Offset Voltage vs Input Common-Mode Voltage

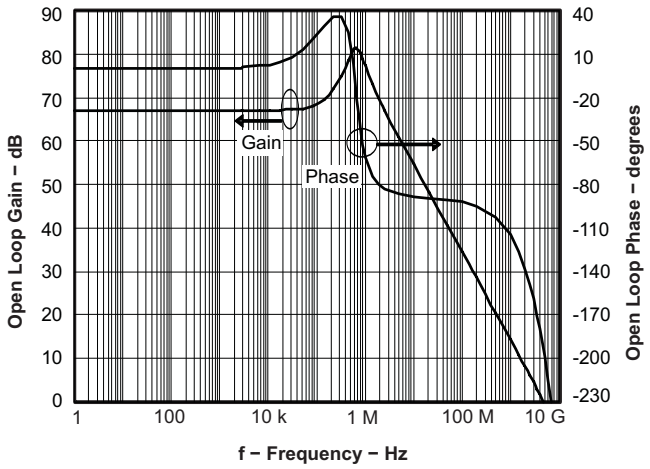


Figure 33. Open-Loop Gain and Phase vs Frequency

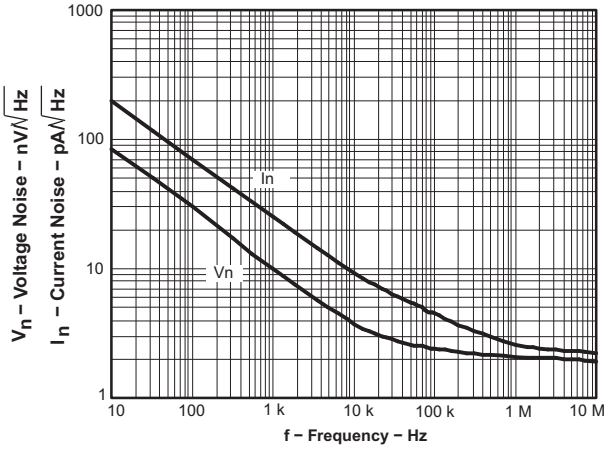


Figure 34. Input Referred Noise vs Frequency

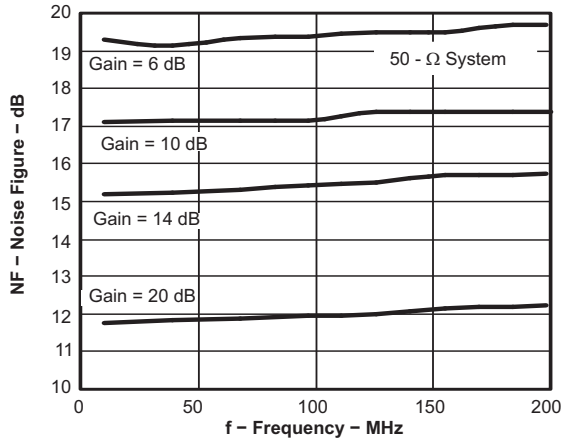


Figure 35. Noise Figure vs Frequency

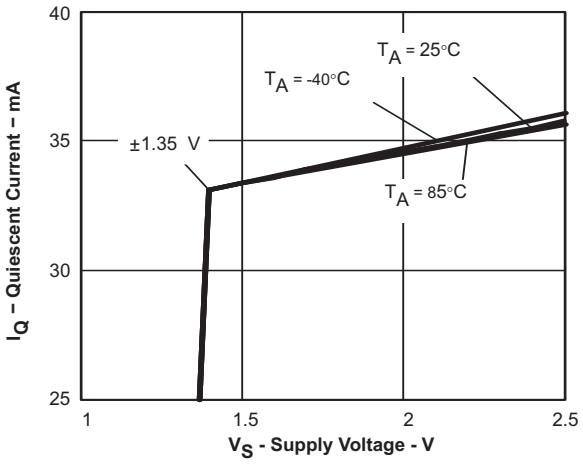


Figure 36. Quiescent Current vs Supply Voltage

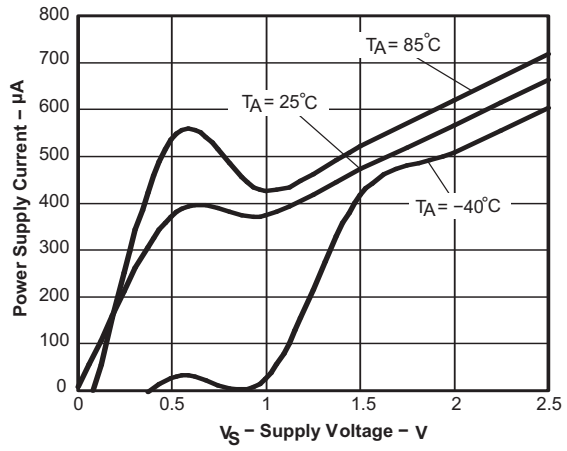


Figure 37. Power-Supply Current vs Supply Voltage in Power-Down Mode

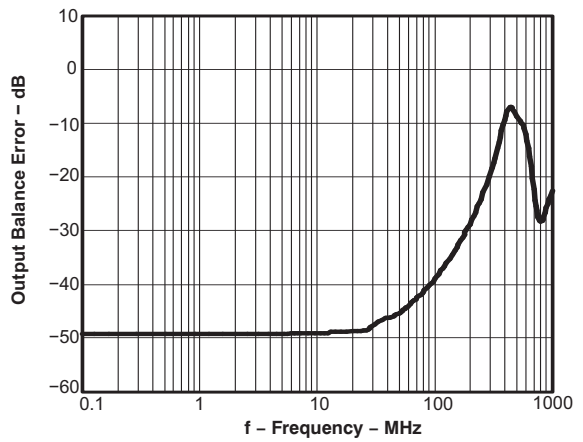


Figure 38. Output Balance Error vs Frequency

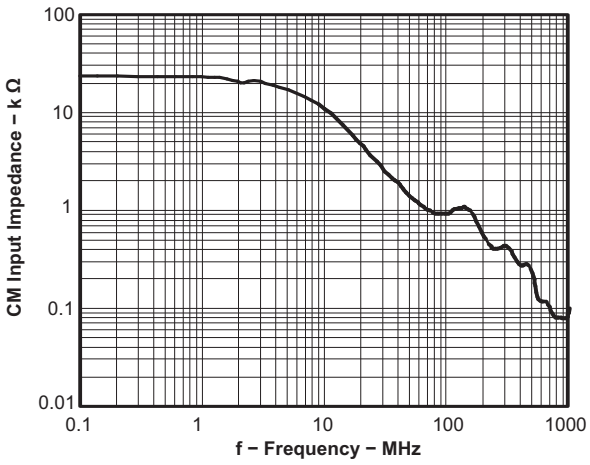


Figure 39. CM Input Impedance vs Frequency

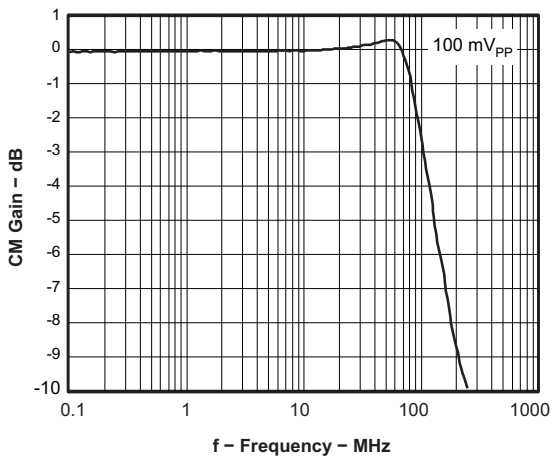


Figure 40. CM Small-Signal Frequency Response

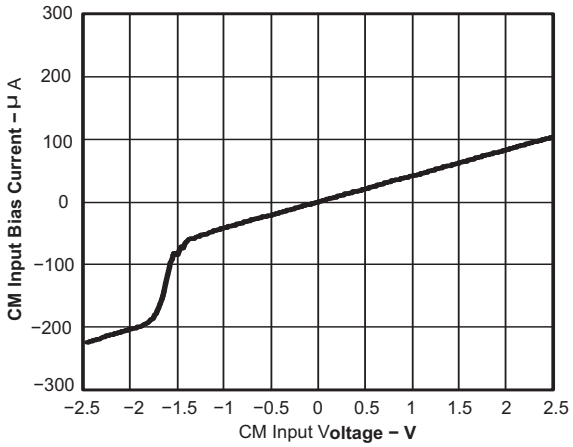


Figure 41. CM Input Bias Current vs CM Input Voltage

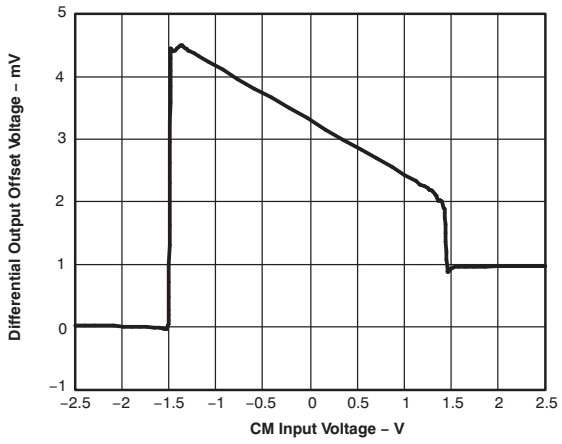


Figure 42. Differential Output Offset Voltage vs CM Input Voltage

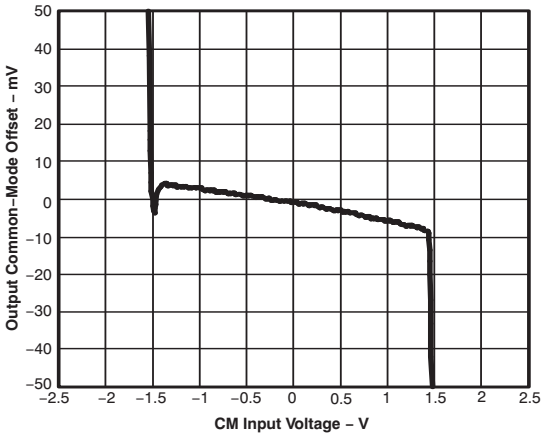


Figure 43. Output Common-Mode Offset vs CM Input Voltage

6.7.2 Typical Characteristics: $V_{S+} - V_{S-} = 3$ V

test conditions (unless otherwise noted): V_{S+} = 1.5 V, V_{S-} = –1.5 V, CM = open, V_{OD} = 1 Vpp, R_F = 349 Ω, R_L = 200 Ω differential, G = 10 dB, single-ended input, input and output referenced to midrail

Table 2. Table of Graphs $V_{S+} - V_{S-} = 3$ V

TYPICAL CHARACTERISTIC CURVE			FIGURE NO.
Small-signal frequency response			Figure 44
Large-signal frequency response			Figure 45
Harmonic distortion	HD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 46
	HD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 47
	HD_2, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 48
	HD_3, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 49
	HD_2, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 50
	HD_3, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 51
Intermodulation distortion	IMD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 52
	IMD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 53
	IMD_2, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 54
	IMD_3, G = 10 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 55
	IMD_2, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 56
	IMD_3, G = 14 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 57
Output intercept point	OIP_2	vs Frequency	Figure 58
	OIP_3	vs Frequency	Figure 59
0.1-dB flatness			Figure 60
S-parameters		vs Frequency	Figure 61
Transition rate		vs Output voltage	Figure 62
Transient response			Figure 63
Settling time			Figure 64
Output voltage swing		vs Load resistance	Figure 65
Rejection ratio		vs Frequency	Figure 66
Overdrive recovery			Figure 67
Output impedance		vs Frequency	Figure 68
Turn-off time			Figure 69
Turn-on time			Figure 70
Output balance error		vs Frequency	Figure 71
Noise figure		vs Frequency	Figure 72
CM input impedance		vs Frequency	Figure 73
Differential output offset voltage		vs CM input voltage	Figure 74
Output common-mode offset		vs CM input voltage	Figure 75

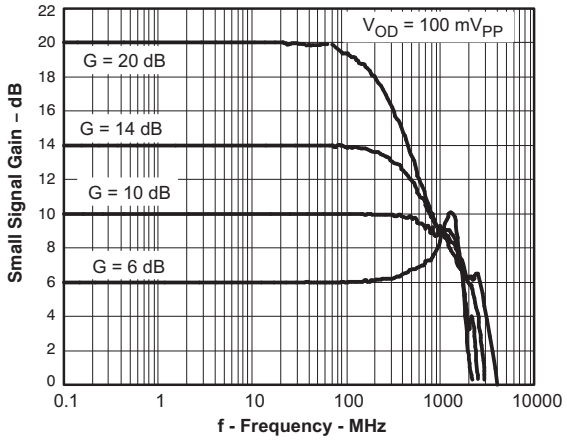


Figure 44. Small-Signal Frequency Response

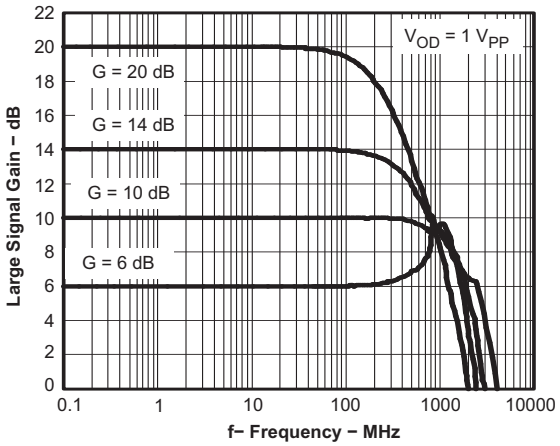


Figure 45. Large-Signal Frequency Response

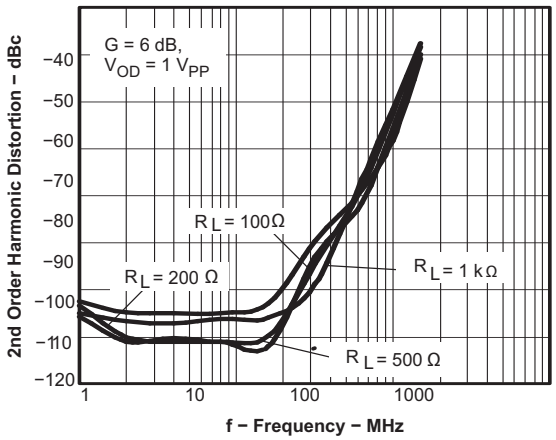


Figure 46. HD2 vs Frequency

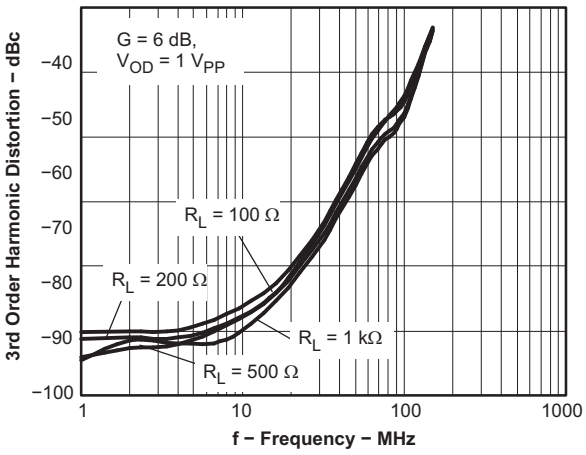


Figure 47. HD3 vs Frequency

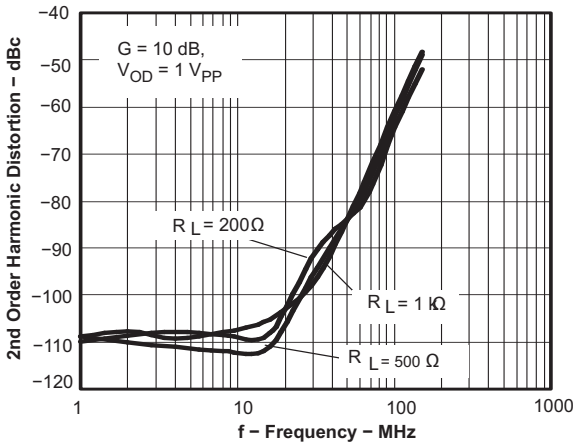


Figure 48. HD2 vs Frequency

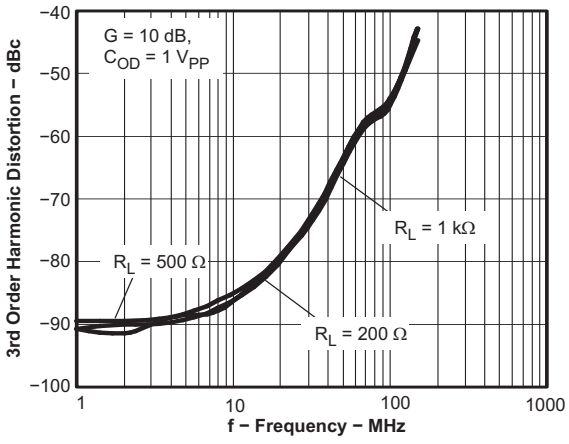


Figure 49. HD3 vs Frequency

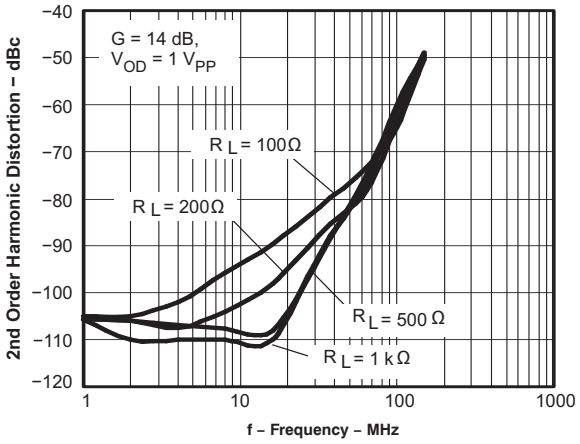


Figure 50. HD2 vs Frequency

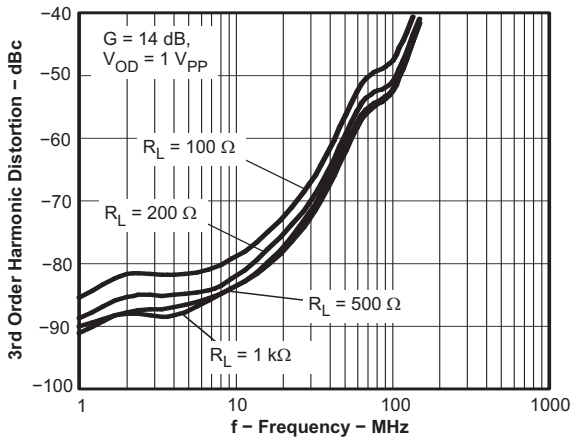


Figure 51. HD3 vs Frequency

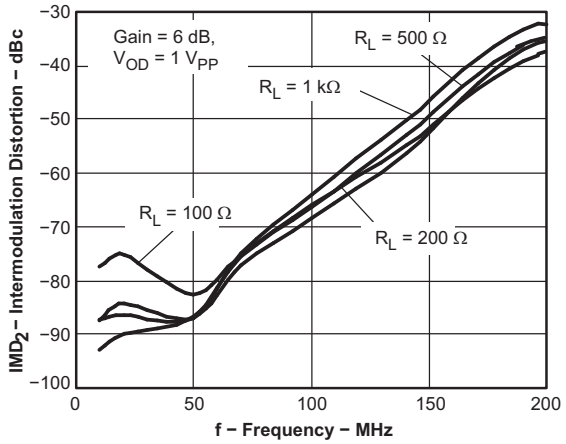


Figure 52. IMD2 vs Frequency

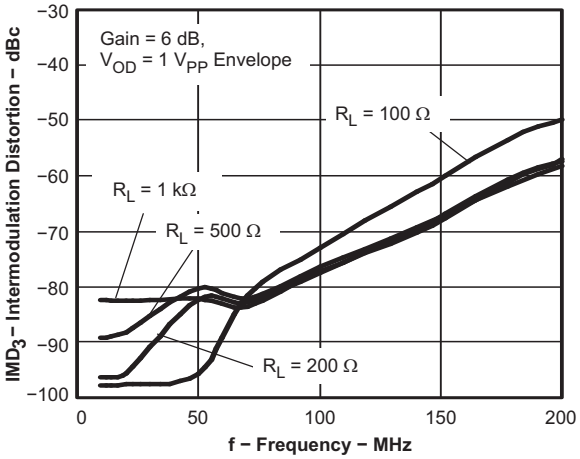


Figure 53. IMD3 vs Frequency

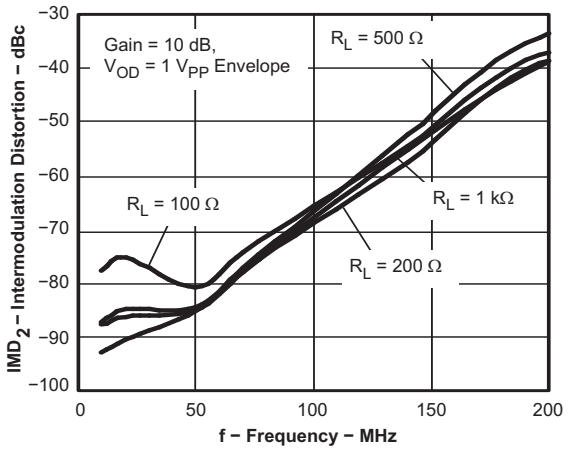


Figure 54. IMD2 vs Frequency

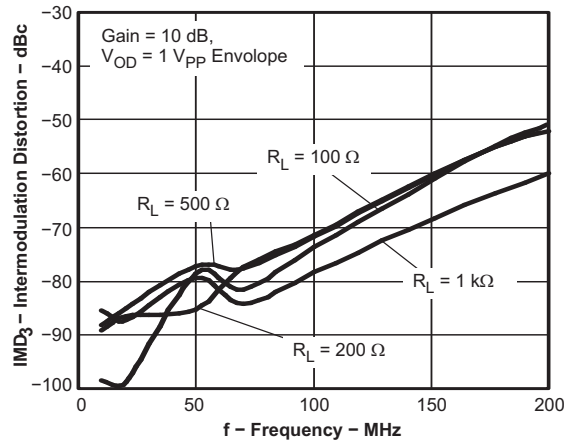


Figure 55. IMD3 vs Frequency

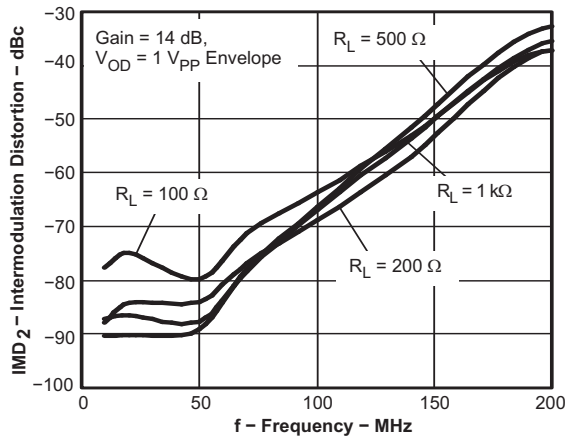


Figure 56. IMD2 vs Frequency

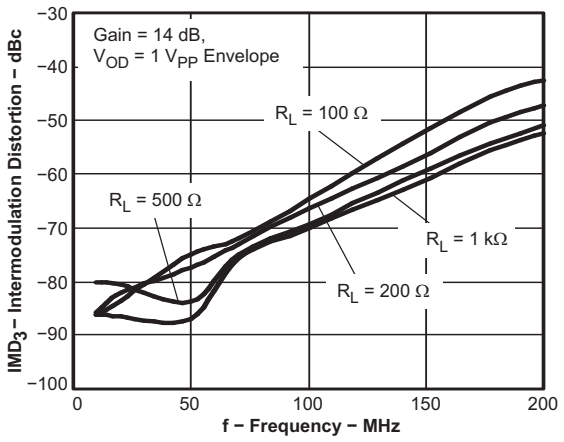


Figure 57. IMD3 vs Frequency

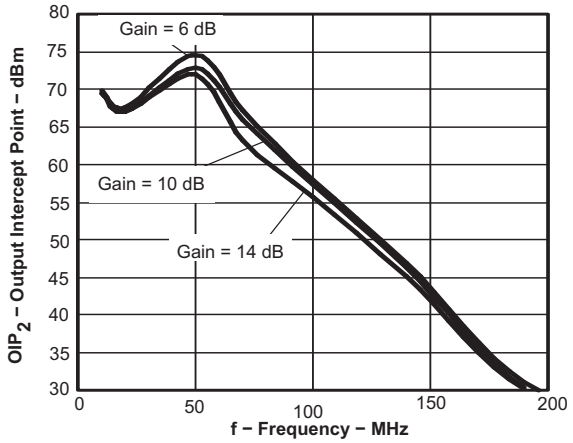


Figure 58. OIP2 vs Frequency

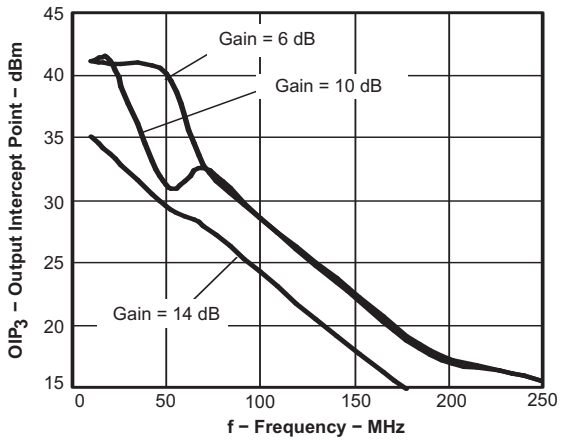


Figure 59. OIP3 vs Frequency

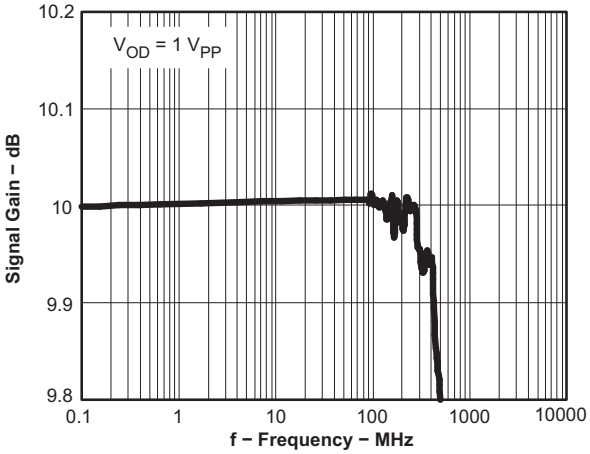


Figure 60. 0.1-dB Flatness

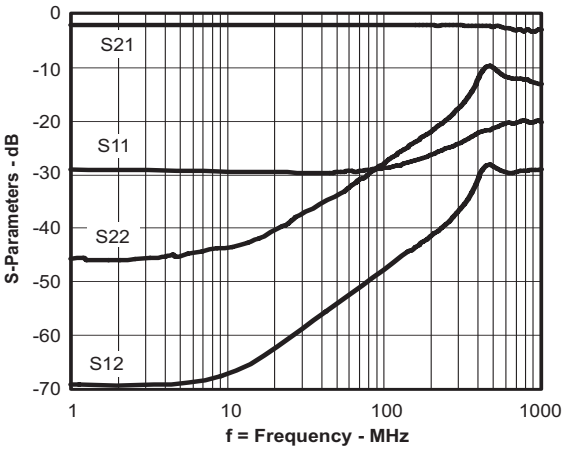


Figure 61. S-Parameters vs Frequency

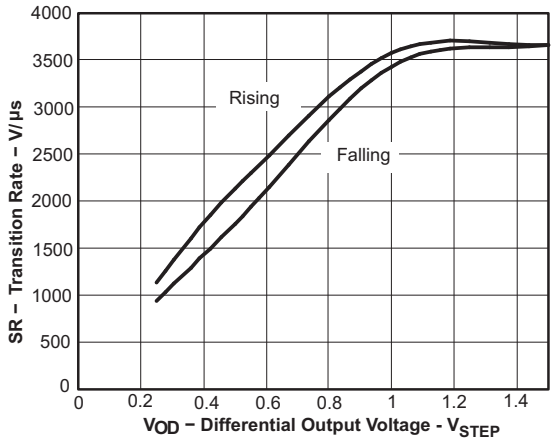


Figure 62. Transition Rate vs Output Voltage

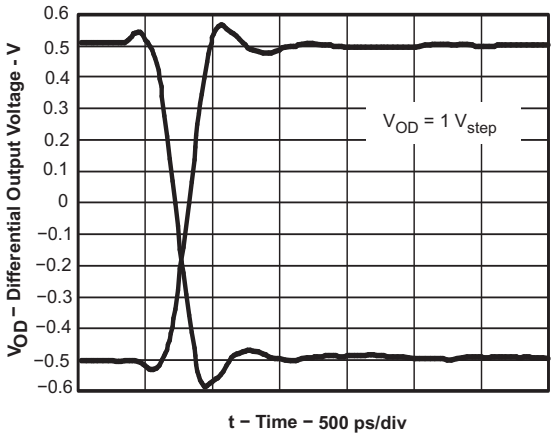


Figure 63. Transient Response

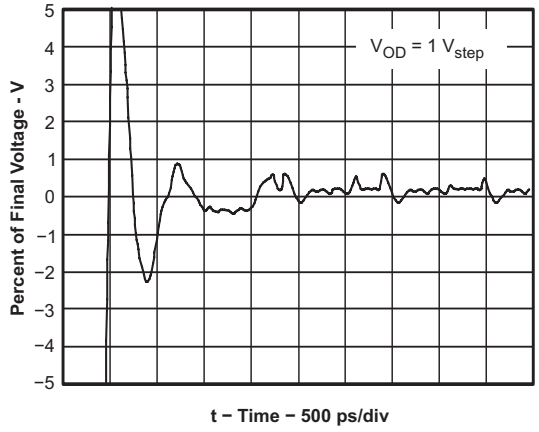


Figure 64. Settling Time

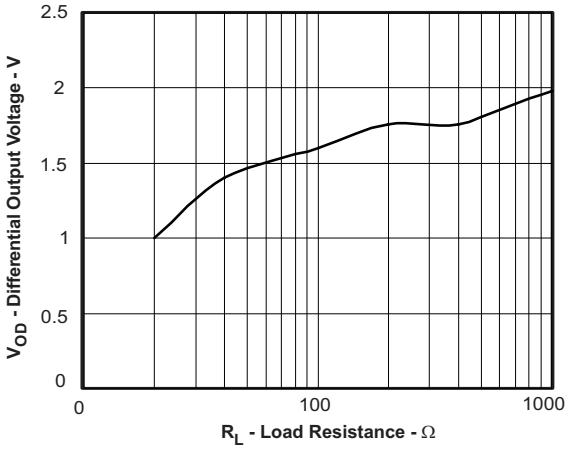


Figure 65. Output Voltage Swing vs Load Resistance

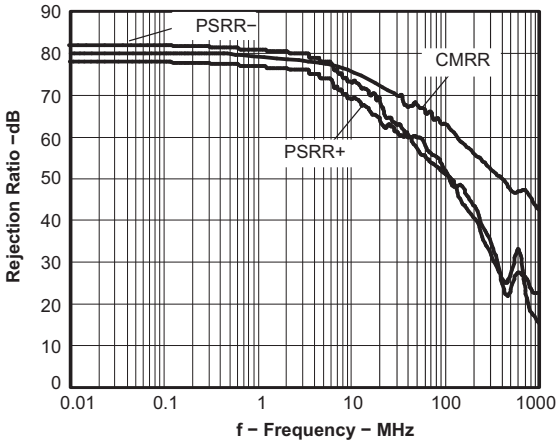


Figure 66. Rejection Ratio vs Frequency

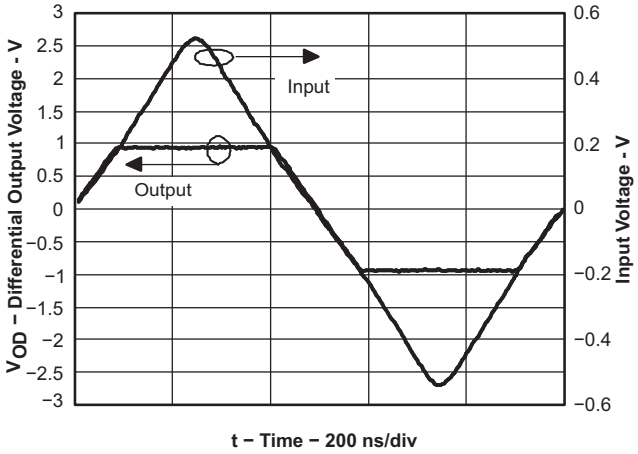


Figure 67. Overdrive Recovery

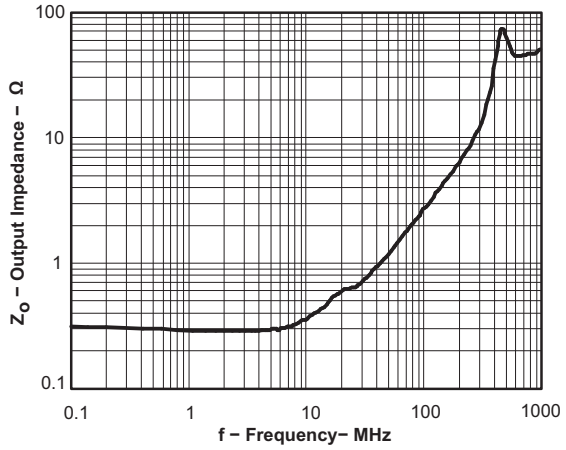


Figure 68. Output Impedance vs Frequency

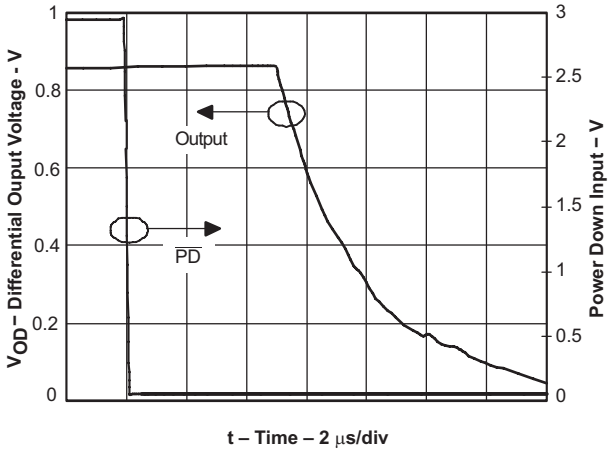


Figure 69. Turn-off Time

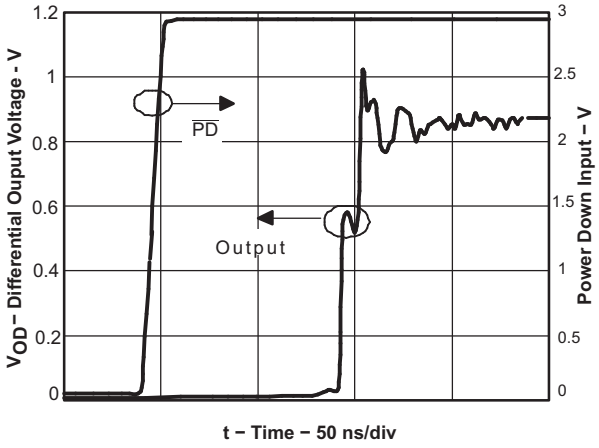


Figure 70. Turn-on Time

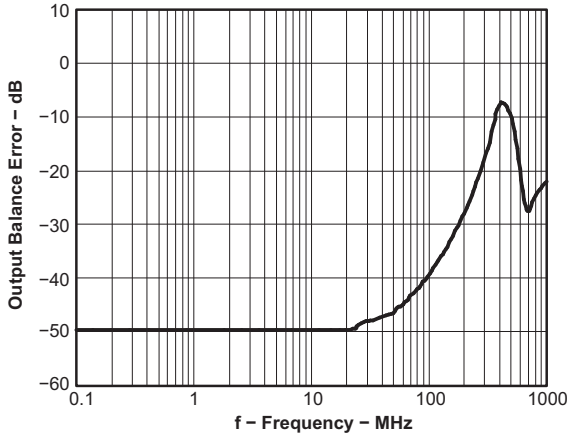


Figure 71. Output Balance Error vs Frequency

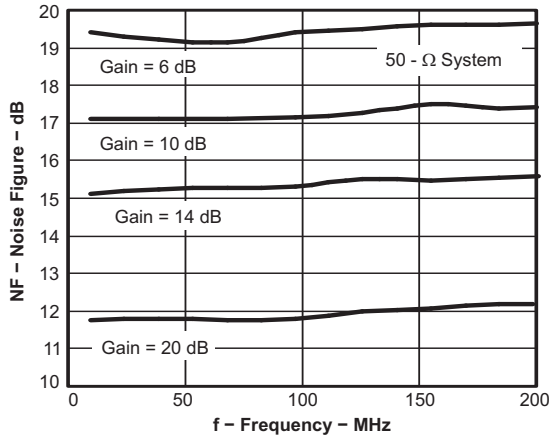


Figure 72. Noise Figure vs Frequency

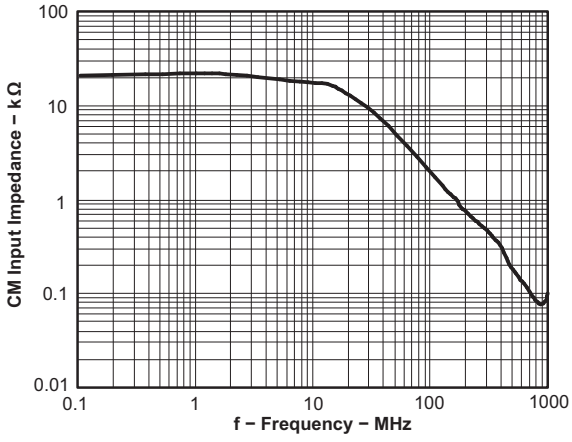


Figure 73. CM Input Impedance vs Frequency

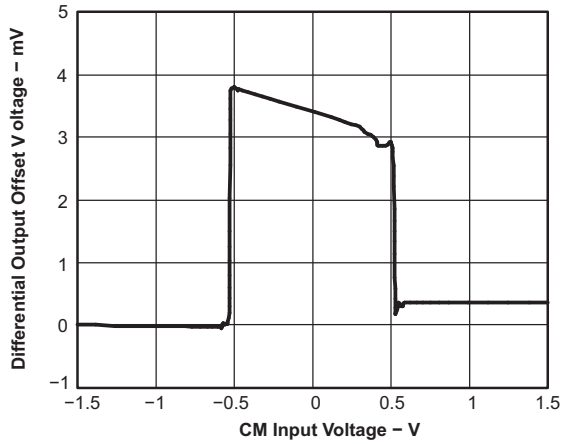


Figure 74. Differential Output Offset Voltage vs CM Input Voltage

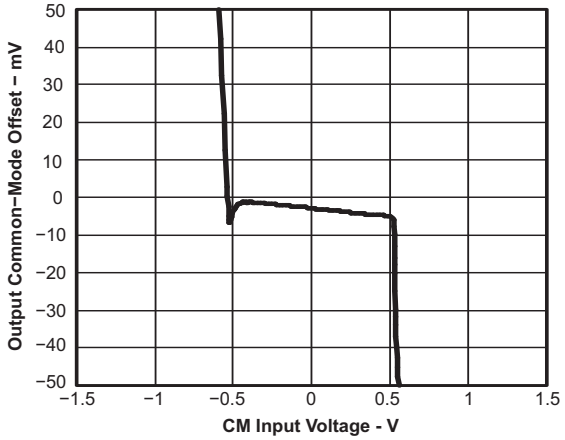


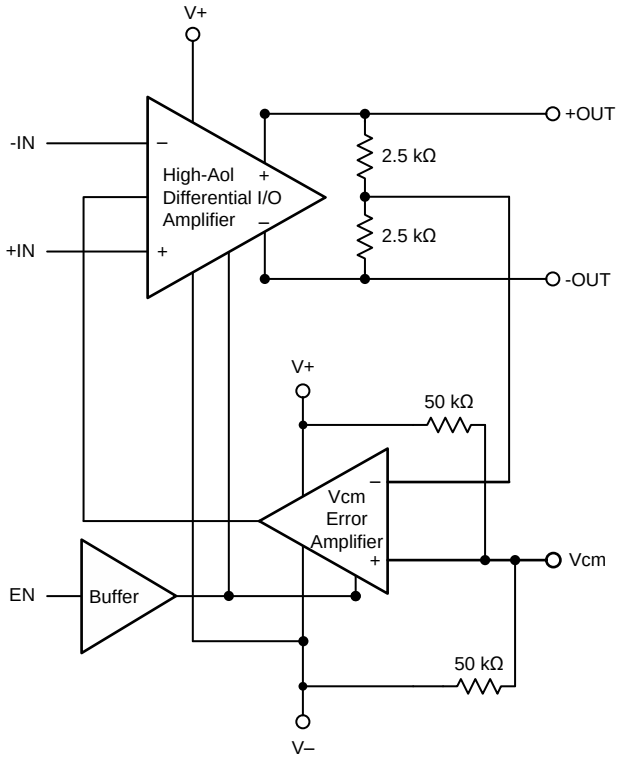
Figure 75. Output Common-Mode Offset vs CM Input Voltage

7 Detailed Description

7.1 Overview

The THS4509-Q1 is a fully differential amplifier designed to provide low distortion amplification to wide bandwidth differential signals. The THS4509-Q1, though fully integrated for ultimate balance and distortion performance, functionally provides three channels. Two of these channels are the positive and negative signal path channels, which function similarly to inverting mode operational amplifiers and are the primary signal paths. The third channel is the common-mode feedback circuit. This is the circuit that sets the output common mode as well as driving the positive and negative outputs to be equal magnitude and opposite phase, even when only one of the two input channels is driven. The common-mode feedback circuit allows single-ended to differential operation.

7.2 Functional Block Diagram



7.3 Feature Description

THS4509-Q1 fully differential amplifier requires external resistors to set a minimum gain of 6 db and optimized gain of 10 db for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either on with the PD pin asserted to a voltage greater than Vs– + 2.1 V, or turned off by asserting PD low. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors. The CM control pin sets the output average voltage. Left open, CM voltage defaults to an internal midsupply value. Driving the CM input with a voltage reference within its valid range sets a target for the internal common mode error amplifier.

7.4 Device Functional Modes

An integrated, fully-differential amplifier is very similar in architecture to a standard, voltage feedback operational amplifier, with a few differences. Both types of amplifiers have differential inputs. Fully differential amplifiers have differential outputs, while a standard operational amplifier's output is single-ended. In a fully-differential amplifier, the output is differential and the output common-mode voltage can be controlled independently of the differential voltage. The purpose of the Vocm input in the fully-differential amplifier is to set the output common-mode voltage. Vocm is biased to the midpoint between positive and negative supplies by an internal voltage divider In a standard operational amplifier with single-ended output, the output common-mode voltage and the signal are the same thing. There is typically one feedback path from the output to the negative input in a standard operational amplifier. A fully-differential amplifier has multiple feedback paths.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following circuits show application information for the THS4509-Q1. For simplicity, power supply decoupling capacitors are not shown in these diagrams. See *THS4509-Q1 EVM* for recommendations. For more detail on the use and operation of fully differential op amps see the application report *Fully-Differential Amplifiers* (SLOA054) .

8.1.1 Test Circuits

The THS4509-Q1 is tested with the following test circuits built on the EVM. For simplicity, power-supply decoupling is not shown – see layout in the applications section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac coupled 50-Ω sources and a 0.22-µF capacitor and a 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single supply, as described in the applications section, with no impact on performance.

Table 3. Gain Component Values

GAIN	R_F	R_G	R_{IT}
6 dB	348 Ω	165 Ω	61.9 Ω
10 dB	348 Ω	100 Ω	69.8 Ω
14 dB	348 Ω	56.2 Ω	88.7 Ω
20 dB	348 Ω	16.5 Ω	287 Ω

NOTE

The gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 4. Load Component Values

R_L	R_O	R_{OT}	ATTEN
100 Ω	25 Ω	open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

NOTE

Note the total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated. The column ATTEN in Table 4 shows the attenuation expected from the resistor divider. When using a transformer at the output, as shown in Figure 77, the signal sees slightly more loss, and these numbers are approximate.

8.1.1.1 Frequency Response

The circuit shown in Figure 76 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

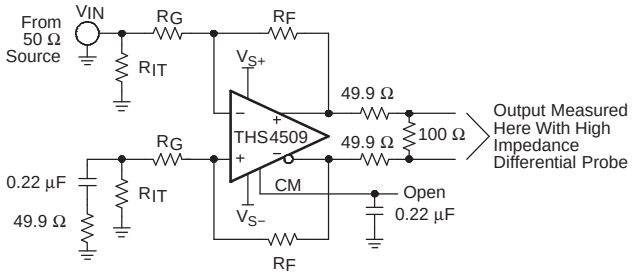


Figure 76. Frequency Response Test Circuit

8.1.1.2 Distortion and 1-dB Compression

The circuit shown in Figure 77 is used to measure harmonic distortion, intermodulation distortion, and 1-db compression point of the amplifier.

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

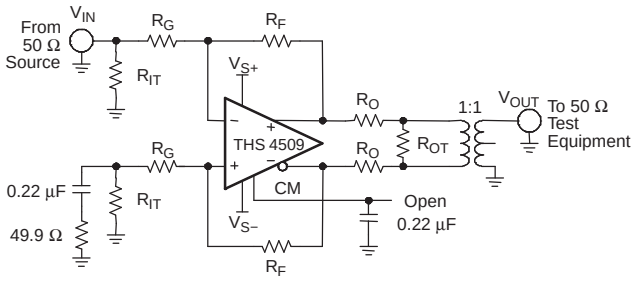


Figure 77. Distortion Test Circuit

The 1-dB compression point is measured with a spectrum analyzer with 50-Ω double termination or 100-Ω termination as shown in Table 4. The input power is increased until the output is 1 dB lower than expected. The number reported in the table data is the power delivered to the spectrum analyzer input. Add 3 dB to see the amplifier output.

8.1.1.3 S-Parameter, Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On and Turn-Off Time

The circuit shown in Figure 78 is used to measure s-parameters, slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turnon and turnoff times of the amplifier. For output impedance, the signal is injected at V_{OUT} with V_{IN} left open and the drop across the 49.9-Ω resistor is used to calculate the impedance seen looking into the amplifier's output.

Because S_{21} is measured single ended at the load with 50-Ω double termination, add 12 dB to refer to the amplifier's output as a differential signal.

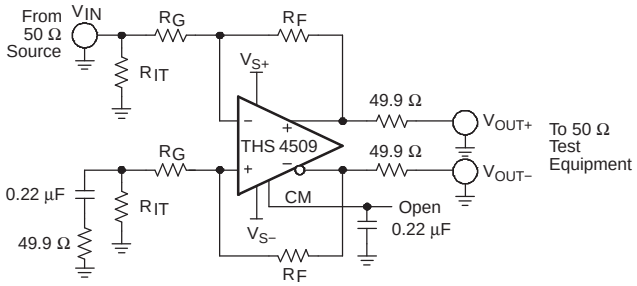


Figure 78. S-Parameter, Sr, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, and Turnon and Turnoff Test Circuit

8.1.1.4 CM Input

The circuit shown in Figure 79 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single ended at V_{OUT+} or $V_{OUT–}$ with the input injected at V_{IN}, R_{CM} = 0 Ω, and R_{CMT} = 49.9 Ω. The input impedance is measured with R_{CM} = 49.9 Ω with R_{CMT} = open, and calculated by measuring the voltage drop across R_{CM} to determine the input current.

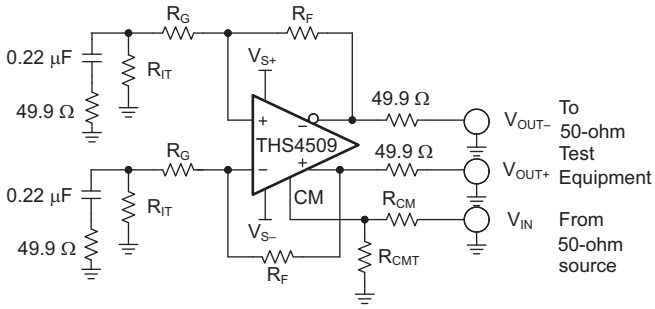


Figure 79. CM Input Test Circuit

8.1.1.5 CMRR and PSRR

The circuit shown in Figure 80 is used to measure the CMRR and PSRR of V_{S+} and $V_{S–}$. The input is switched appropriately to match the test being performed.

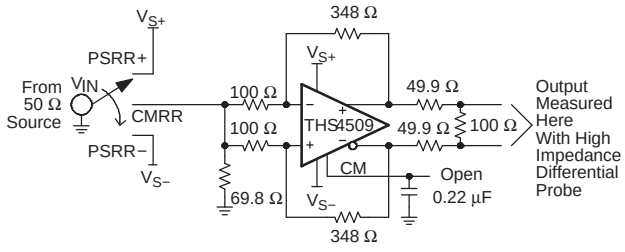


Figure 80. CMRR and PSRR Test Circuit

8.1.2 Differential Input to Differential Output Amplifier

The THS4509-Q1 is a fully differential op amp, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 81 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

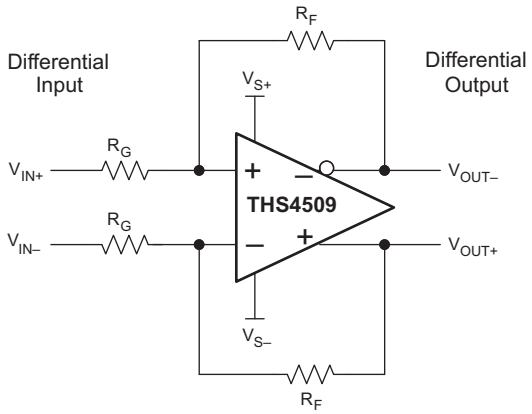


Figure 81. Differential Input to Differential Output Amplifier

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

8.1.3 Single-Ended Input to Differential Output Amplifier

The THS4509-Q1 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 82 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

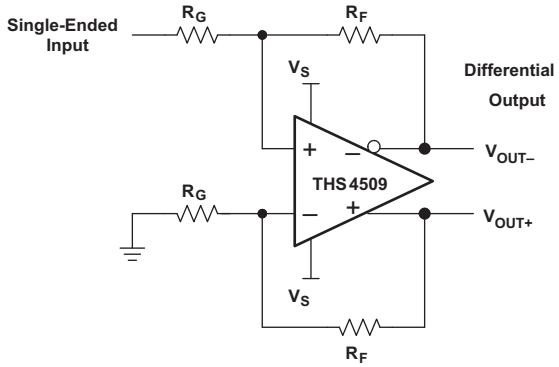


Figure 82. Single-Ended Input to Differential Output Amplifier

8.1.4 Input Common-Mode Voltage Range

The input common-model voltage of a fully differential op amp is the voltage at the + and – input pins of the op amp.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin will determine the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

8.1.5 Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 3-mV offset (typical) from the set voltage, when set within 0.5 V of mid-supply, with less than 4-mV differential offset voltage. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be overdriven from an external source. Figure 83 is representative of the CM input. The internal CM circuit has about 700 MHz of –3-dB bandwidth, which is required for best performance, but it is intended to be a DC bias input pin. To reduce noise at the output, TI recommends bypass capacitors are recommended on this pin. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where

- V_{CM} is the voltage applied to the CM pin.

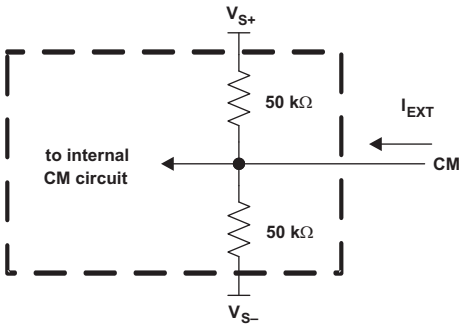


Figure 83. CM Input Circuit

8.1.6 Single-Supply Operation (3 V to 5 V)

To facilitate testing with common lab equipment, the THS4509-Q1 EVM allows split-supply operation, and the characterization data presented in this data sheet was taken with split-supply power inputs. The device can easily be used with a single-supply power input without degrading the performance. Figure 84, Figure 85, and Figure 86 show DC and AC-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to mid-supply allowing for optimum performance. The information presented here can also be applied to differential input sources.

In Figure 84, the source is referenced to the same voltage as the CM pin (V_{CM}). V_{CM} is set by the internal circuit to mid-supply. R_T along with the input impedance of the amplifier circuit provides input termination, which is also referenced to V_{CM}.

Note R_S and R_T are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value R_G+ $R_S||R_T$ on this input. This is also true of the circuits shown in Figure 85 and Figure 86.

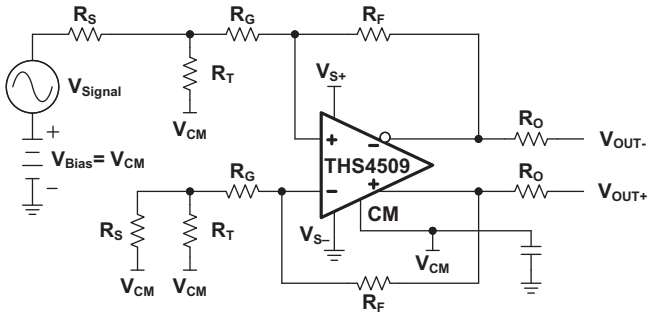


Figure 84. THS4509-Q1 DC-Coupled Single Supply With Input Biased to V_{CM}

In Figure 85 the source is referenced to ground and so is the input termination resistor. R_{PU} is added to the circuit to avoid violating the V_{ICR} of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} = \frac{(V_{IC} - V_{S+})}{V_{CM}\left(\frac{1}{R_F}\right) - V_{IC}\left(\frac{1}{R_{IN}} + \frac{1}{R_F}\right)} \quad (3)$$

where

- V_{IC} is the desire input common-mode voltage
- V_{CM} = CM
- $R_{IN} = R_G + R_S||R_T$

To set to mid-supply, make the value of $R_{PU} = R_G + R_S||R_T$.

Table 5 is a modification of Table 3 to add the proper values with R_{PU} assuming a 50-Ω source impedance and setting the input and output common-mode voltage to mid-supply.

There are two drawbacks to this configuration. One is it requires additional current from the power supply. Using the values shown for a gain of 10 dB requires 37 mA more current with 5-V supply, and 22 mA more current with 3-V supply.

The other drawback is this configuration also increases the noise gain of the circuit. In the 10-dB gain case, noise gain increases by a factor of 1.5.

Table 5. RPU Values for Various Gains

GAIN	R_F	R_G	R_{IT}	R_{PU}
6 dB	348 Ω	169 Ω	64.9 Ω	200 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	133 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	97.6 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	80.6 Ω

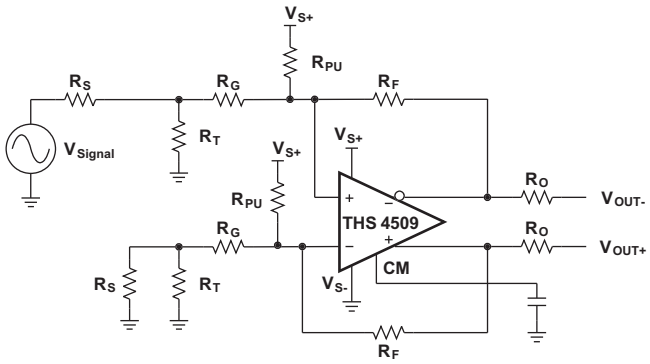


Figure 85. THS4509-Q1 DC-Coupled Single Supply With R_{PU} Used to Set V_{IC}

Figure 86 shows AC coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self bias both input and output to mid-supply.

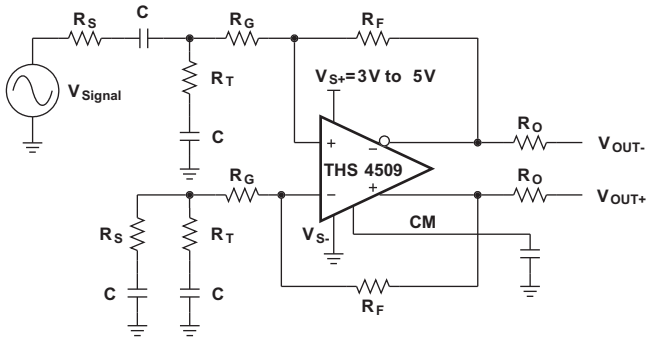


Figure 86. THS4509-Q1 AC-Coupled Single Supply

8.2 Typical Applications

8.2.1 THS4509-Q1 + ADS5500-EP Combined Performance

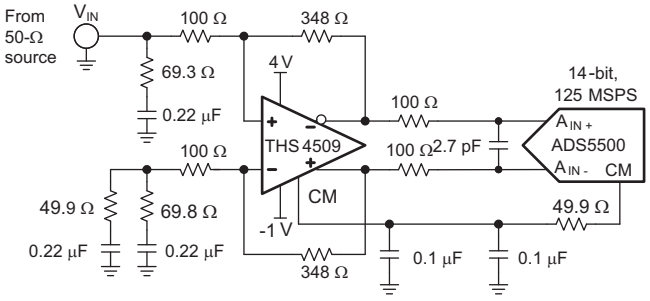


Figure 87. THS4509-Q1 + ADS5500-EP Circuit

Typical Applications (continued)

8.2.1.1 Design Requirements

The THS4509-Q1 can be used in adjacent applications, such as industrial, in combination with HiRel devices. As automotive standards are similar to industrial standards, automotive devices are often suitable alternative options for the industrial customers. Applications using fully differential amplifiers have several requirements. The main requirements are high linearity and good signal amplitude. Linearity is accomplished by using well matched feedback and gain set resistors as well as an appropriate supply voltage. The signal amplitude can be tailored by using an appropriate gain. In this design the gain is set for a gain of 3.48 (RF=348/ RG=100), the SFDR is 80 dBc, and the SNR is 69 dBc at a frequency of 70 Mhz. The supply voltages are set to 4 V and –1 V and the output common mode is 1.55 V. The TSH4509 can be placed into shutdown to reduce power dissipation to less than 5 mW.

8.2.1.2 Detailed Design Procedure

The THS4509-Q1 is designed to be a high performance drive amplifier for high performance data converters like the ADS5500-EP 14-bit 125-MSPS ADC. Figure 87 shows a circuit combining the two devices, and Figure 88 shows the combined SNR and SFDR performance versus frequency with –1-dBFS input signal level sampling at 125 MSPS. The THS4509-Q1 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5500-EP. The 100-Ω resistors and 2.7-pF capacitor between the THS4509-Q1 outputs and ADS5500-EP inputs along with the input capacitance of the ADS5500-EP limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an AC-coupled 50-Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8-Ω resistor and 0.22-µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor are inserted to ground across the 69.8-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See Table 5 for component values to set proper 50-Ω termination for other common gains. A split power supply of 4 V and –1 V is used to set the input and output common-mode voltages to approximately mid-supply while setting the input common-mode of the ADS5500-EP to the recommended 1.55 V. This maintains maximum headroom on the internal transistors of the THS4509-Q1 to ensure optimum performance.

Figure 89 shows the two-tone FFT of the THS4509-Q1 + ADS5500-EP circuit with 65-MHz and 70-MHz input frequencies. The SFDR is 90 dBc.

8.2.1.3 Application Curves

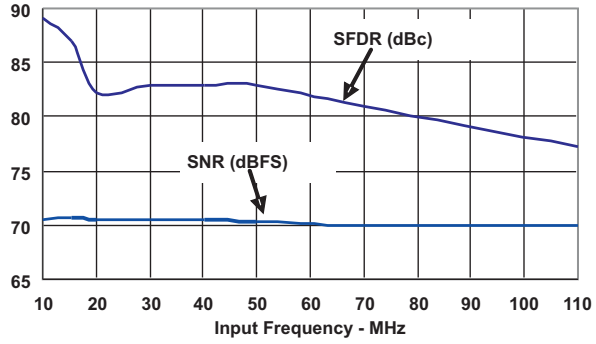


Figure 88. THS4509-Q1 + ADS5500-EP SFDR and SNR Performance Versus Frequency

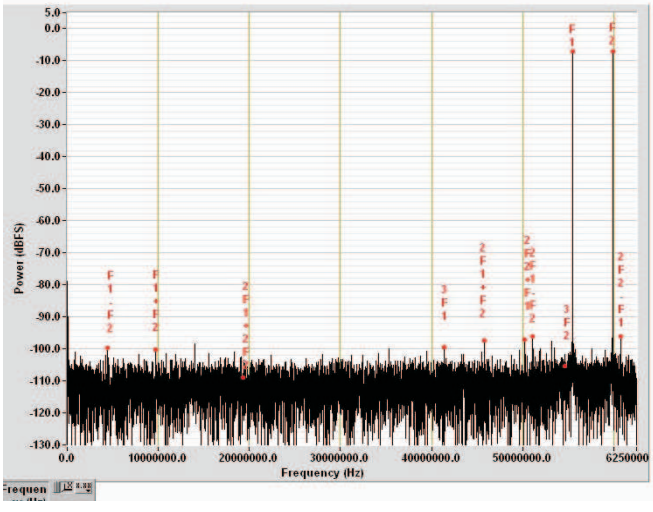


Figure 89. THS4509-Q1 + ADS5500-EP Two-Tone Fft With 65-MHz and 70-MHz Input

Typical Applications (continued)

8.2.2 THS4509-Q1 + ADS5424-SP Combined Performance

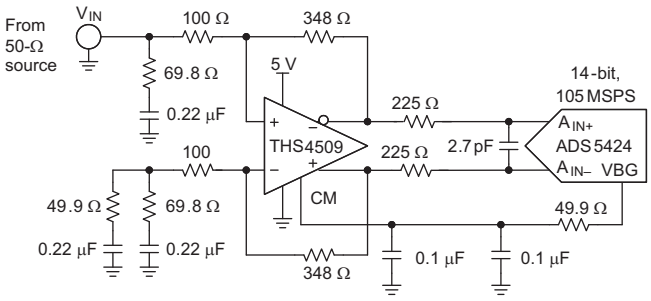


Figure 90. THS4509-Q1 + ADS5424-SP Circuit

8.2.2.1 Detailed Design Procedure

Figure 90 shows the THS4509-Q1 driving the ADS5424-SP ADC, and Figure 91 shows their combined SNR and SFDR performance versus frequency with –1-dBFS input signal level and sampling at 80 MSPS.

As before, the THS4509-Q1 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424-SP. Input termination and circuit testing is the same as previously described for the THS4509-Q1 + ADS5500-EP circuit.

The 225-Ω resistors and 2.7-pF capacitor between the THS4509-Q1 outputs and ADS5424-SP inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (–3 dB).

Since the ADS5424-SP's recommended input common-mode voltage is 2.4 V, the THS4509-Q1 is operated from a single power-supply input with V_{S+} = 5 V and $V_{S–}$ = 0 V (ground).

8.2.2.2 Application Curve

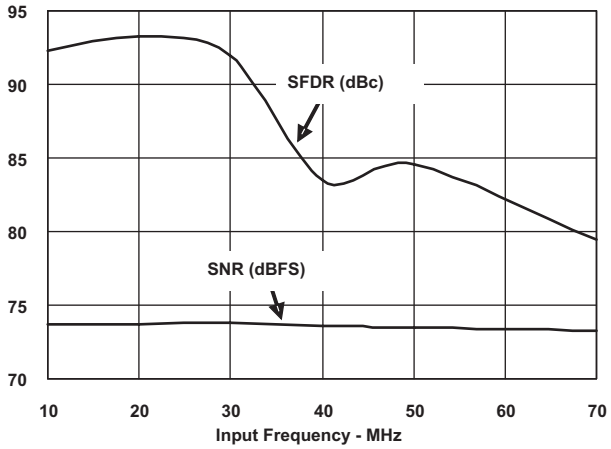


Figure 91. THS4509-Q1 + ADS5424-SP SFDR and SNR Performance vs Frequency

9 Power Supply Recommendations

The THS4509-Q1 can be used with any combination of positive and negative power supplies as long as the combined supply voltage is between 3 V and 5 V. The THS4509-Q1 will provide best performance when the output voltage is set at the mid supply voltage, and when the total supply voltage is between 3 V and 5 V. Power supply bypassing as shown in Figure 93 and Figure 92 is important and power supply regulation should be within 5% or better when using a supply voltage near the edges of the operating range.

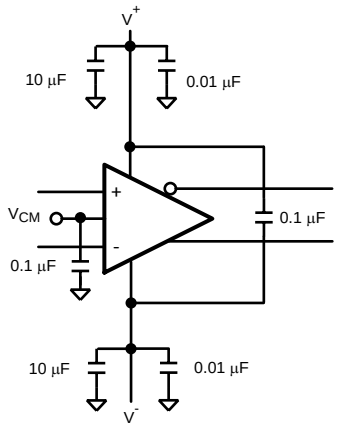


Figure 92. Split Supply Bypassing Capacitors

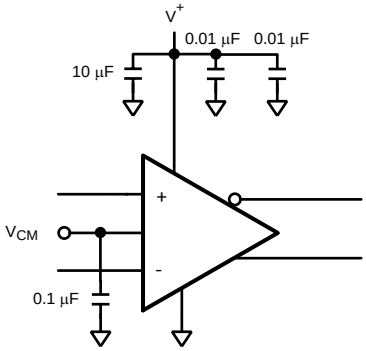


Figure 93. Single Supply Bypassing Capacitors

10 Layout

10.1 Layout Guidelines

TI recommends following the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10-µF and two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1-µF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.
9. The THS4509-Q1 recommended PCB footprint is shown in Figure 94.

Layout Guidelines (continued)

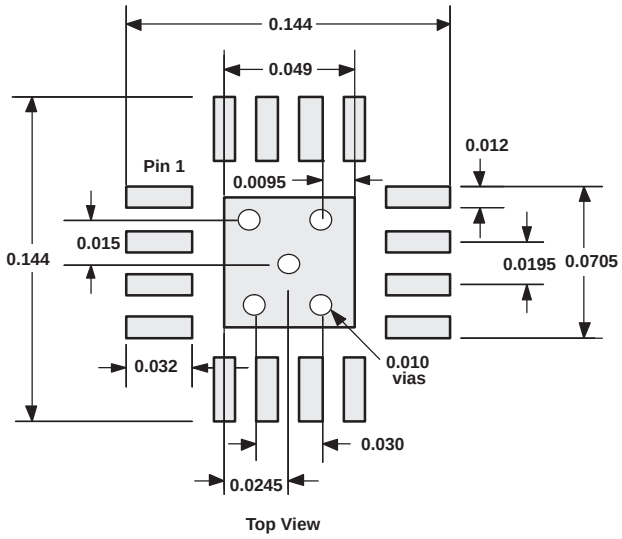


Figure 94. QFN Etch and Via Pattern

10.1.1 THS4509-Q1 EVM

Figure 95 is the THS4509-Q1 EVAL1 EVM schematic, layers 1 through 4 of the PCB are shown in Figure 96, and Table 6 is the bill of material for the EVM as supplied from TI.

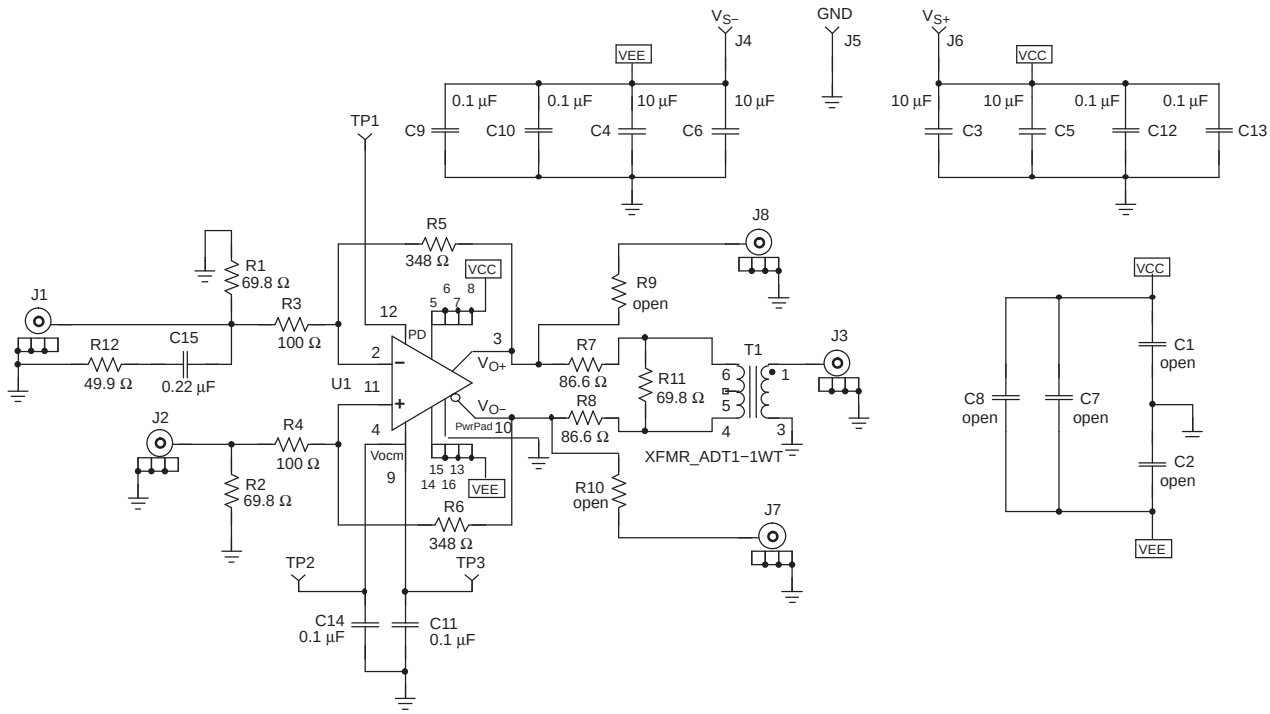


Figure 95. THS4509-Q1 EVAL1 EVM Schematic

Layout Guidelines (continued)

Table 6. THS4509-Q1 EVAL1 EVM Bill Of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER
1	CAPACITOR, 10 µF, ceramic, X5R, 6.3 V	0805	C3, C4, C5, C6	4	(AVX) 08056D106KAT2A
2	CAPACITOR, 0.1 µF, ceramic, X5R, 10 V	0402	C9, C10, C11, C12, C13, C14	6	(AVX) 0402ZD104KAT2A
3	CAPACITOR, 0.22 µF, ceramic, X5R, 6.3 V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8	4	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 Ω, 1/16 W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
8	Resistor, 69.8 Ω, 1/16 W, 1%	0402	R1, R2, R11	3	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 Ω, 1/16 W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 100 Ω, 1/16 W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP1000F
11	Resistor, 348 Ω, 1/16 W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
13	Jack, banana receptacle, 0.25" diameter hole		J4, J5, J6	3	(HH SMITH) 101
14	OPEN		J1, J7, J8	3	
15	Connector, edge, SMA PCB jack		J2, J3	2	(JOHNSON) 142-0701-801
16	Test point, red		TP1, TP2, TP3	3	(KEYSTONE) 5000
17	IC, THS4509		U1	1	(TI) THS4509RGT
18	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
19	Screw, phillips, 4-40, 0.250"			4	SHR-0440-016-SN
20	Printed-circuit-board			1	(TI) EDGE# 6468901

10.1.2 EVM Warnings and Restrictions

It is important to operate this EVM within the input and output voltage ranges below:

- Input Range, V_I: 3 V to 6 V not to exceed V_{S+} or V_{S-}
- Output range, V_O: 3 V to 6 V not to exceed V_{S+} or V_{S-}

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the product data sheet or EVM user's guide (if user's guide is available) prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

10.2 Layout Example

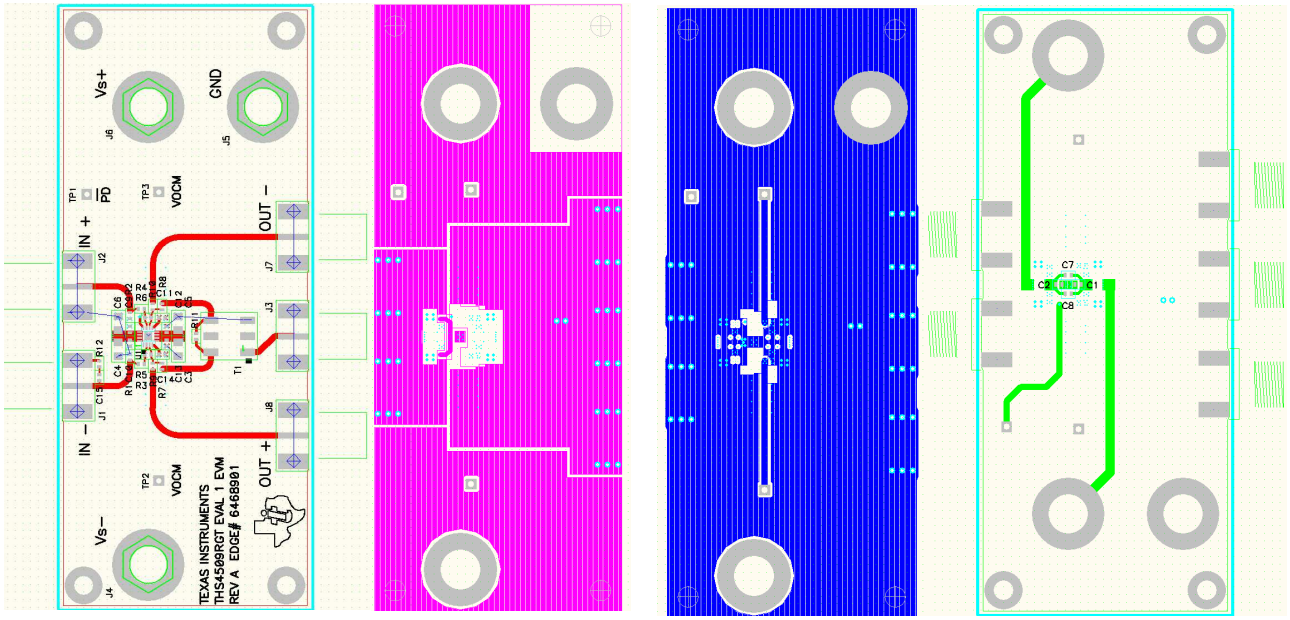


Figure 96. THS4509-Q1 EVAL1 EVM Layer 1 Through 4

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the application report, *Fully-Differential Amplifiers* (SLOA054).

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4509QRGTRQ1	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF THS4509-Q1 :

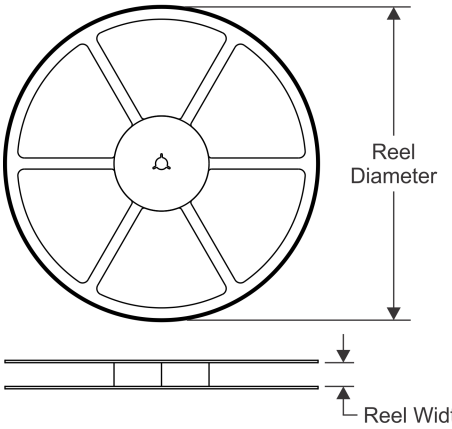
- Catalog: THS4509

NOTE: Qualified Version Definitions:

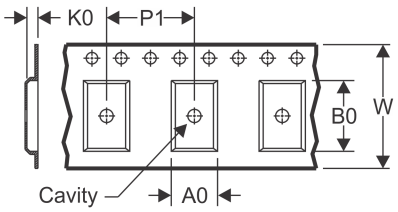
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

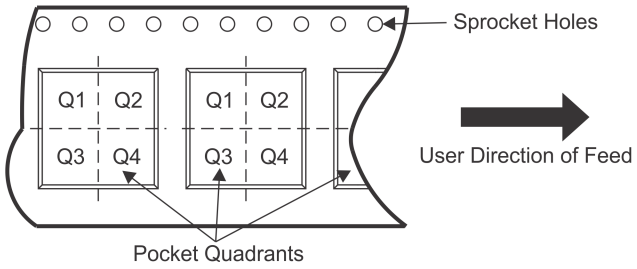


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

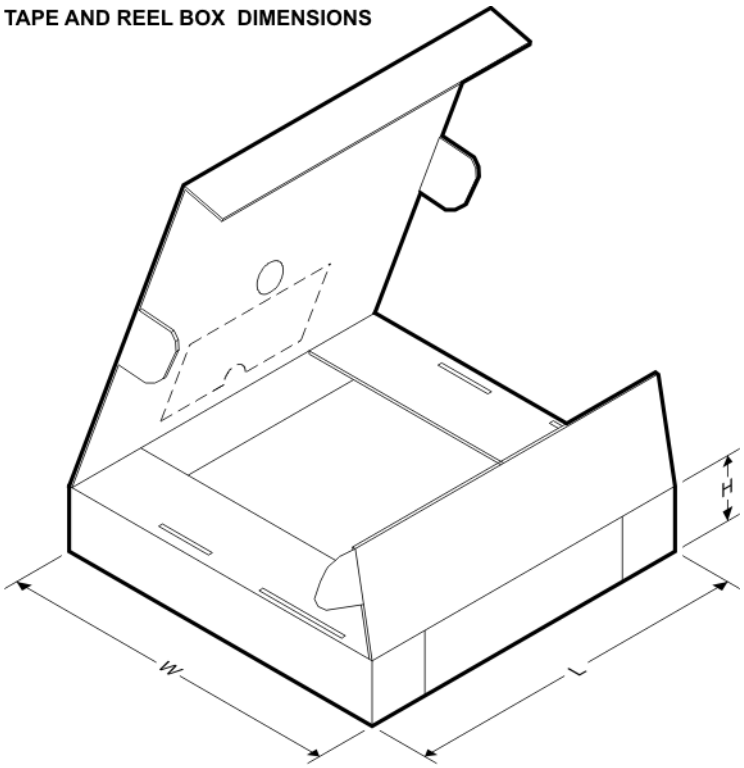
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4509QRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

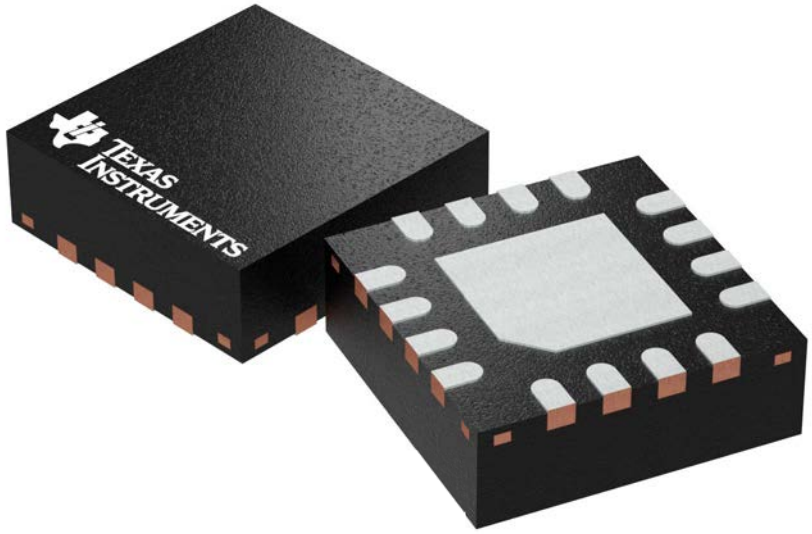


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4509QRGTRQ1	VQFN	RGT	16	3000	853.0	449.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



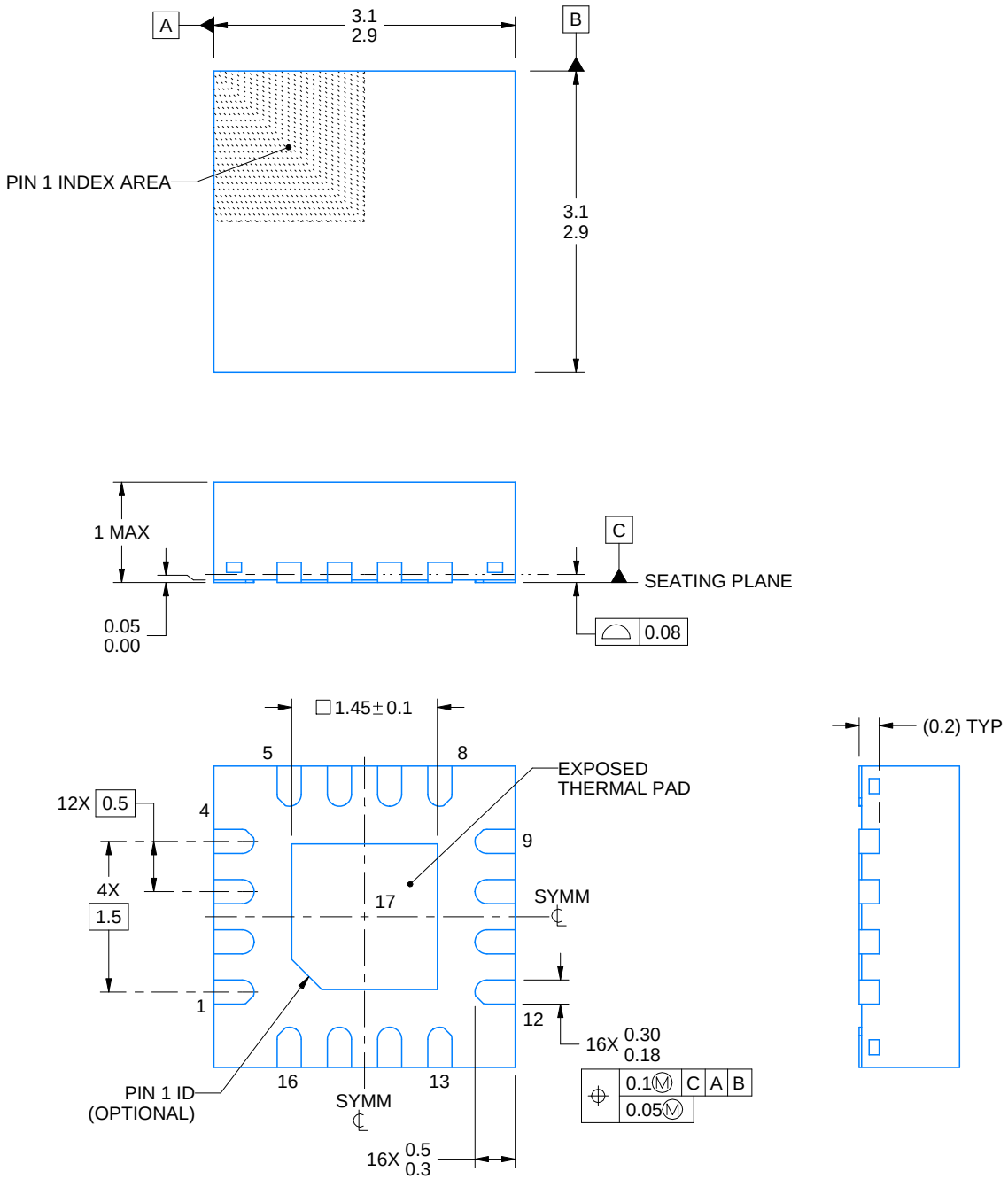
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

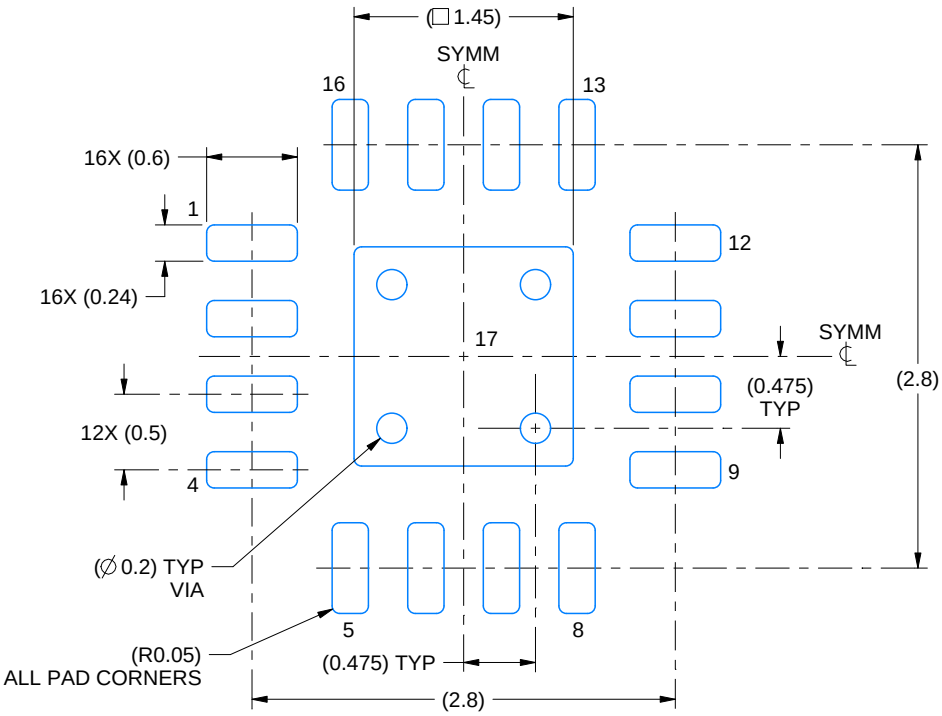
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

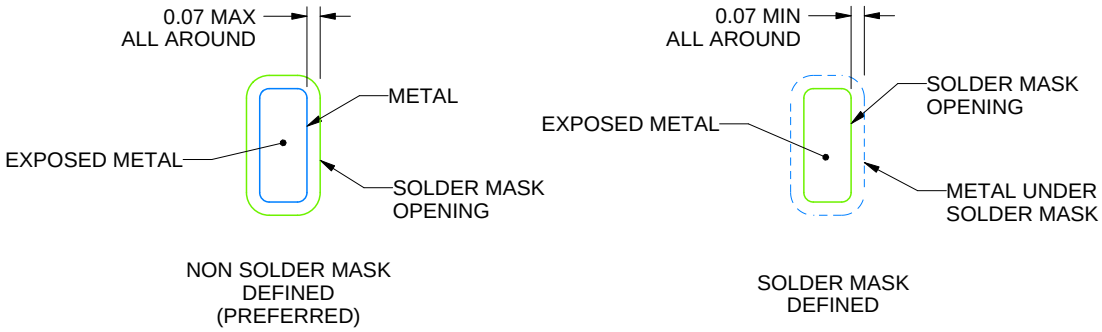


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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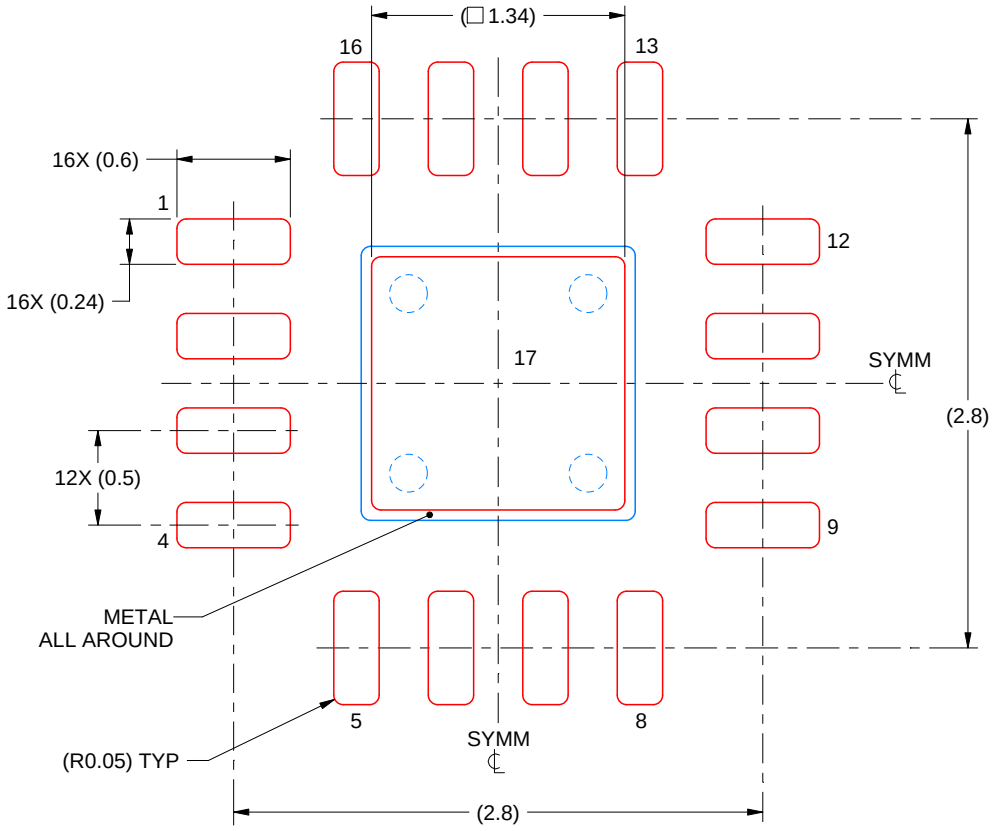
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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