1,048,576 WORDS x 32 BIT DYNAMIC RAM MODULE

**PRELIMINARY**

## DESCRIPTION

The THM321020S is a 1,048,576 words by 32 bits dynamic RAM module which assembled 8 pcs of TC514400J on the printed circuit board. The THM321020S can be as well used as 2,097,152 words by 16 bits dynamic RAM module, by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. The THM321020S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

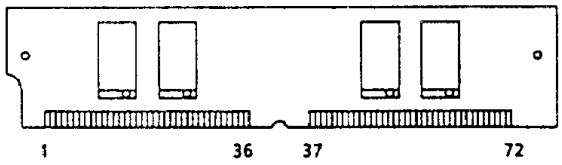
## FEATURES

- 1,048,576 words by 32 bits organization
- Fast access time and cycle time

| | | THM321020 S-80 | THM321020 S-10 |
|---|---|---|---|
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 80ns | 100ns |
| $t_{AA}$ | Column Address Access Time | 40ns | 50ns |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 20ns | 25ns |
| $t_{RC}$ | Cycle Time | 150ns | 180ns |
| $t_{PC}$ | Fast Page Mode Cycle Time | 50ns | 60ns |

- Single power supply of 5V ± 10%
- Low power
  4,620mW MAX. Operating (THMxxxxxx-80)
  3,960mW MAX. Operating (THMxxxxxx-10)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1024 Refresh cycles/16ms
- Tin-Lead Contact : THM321020S-80,10
- Gold Contact : THM321020SG-80,10

## PIN CONNECTION (TOP VIEW)



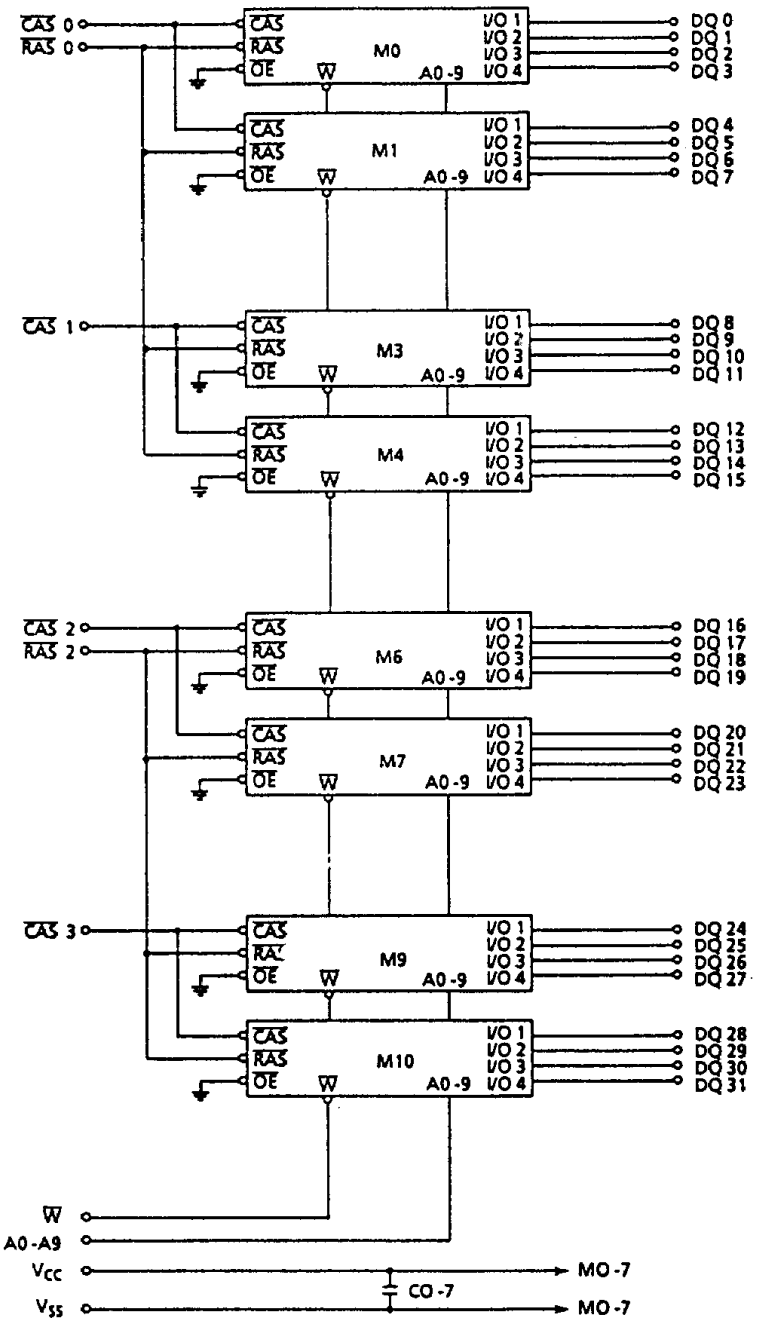

## PIN NAMES

| | |
|---|---|
| A0~A9 | Address Inputs |
| DQ0~DQ31 | Data Input/Outputs |
| $\overline{CAS0}$~$\overline{CAS3}$ | Column Address Strobe |
| $\overline{RAS0}$, $\overline{RAS2}$ | Row Address Strobe |
| $\overline{W}$ | Read/Write Input |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| PD | Presence Detect Pin |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 13 | A1 | 25 | DQ22 | 37 | NC | 49 | DQ8 | 61 | DQ13 |
| 2 | DQ0 | 14 | A2 | 26 | DQ7 | 38 | NC | 50 | DQ24 | 62 | DQ30 |
| 3 | DQ16 | 15 | A3 | 27 | DQ23 | 39 | $V_{SS}$ | 51 | DQ9 | 63 | DQ14 |
| 4 | DQ1 | 16 | A4 | 28 | A7 | 40 | $\overline{CAS0}$ | 52 | DQ25 | 64 | DQ31 |
| 5 | DQ17 | 17 | A5 | 29 | NC | 41 | $\overline{CAS2}$ | 53 | DQ10 | 65 | DQ15 |
| 6 | DQ2 | 18 | A6 | 30 | $V_{CC}$ | 42 | $\overline{CAS3}$ | 54 | DQ26 | 66 | NC |
| 7 | DQ18 | 19 | NC | 31 | A8 | 43 | $\overline{CAS1}$ | 55 | DQ11 | 67 | PD0 |
| 8 | DQ3 | 20 | DQ4 | 32 | A9 | 44 | $\overline{RAS0}$ | 56 | DQ27 | 68 | PD1 |
| 9 | DQ19 | 21 | DQ20 | 33 | NC | 45 | NC | 57 | DQ12 | 69 | PD2 |
| 10 | $V_{CC}$ | 22 | DQ5 | 34 | $\overline{RAS2}$ | 46 | NC | 58 | DQ28 | 70 | PD3 |
| 11 | NC | 23 | DQ21 | 35 | NC | 47 | $\overline{W}$ | 59 | $V_{CC}$ | 71 | NC |
| 12 | A0 | 24 | DQ6 | 36 | NC | 48 | NC | 60 | DQ29 | 72 | $V_{SS}$ |

| | -80 | -10 |
|---|---|---|
| PD0 | $V_{SS}$ | $V_{SS}$ |
| PD1 | $V_{SS}$ | $V_{SS}$ |
| PD2 | NC | $V_{SS}$ |
| PD3 | $V_{SS}$ | $V_{SS}$ |

BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| ITEM | SYMBOL | RATING | UNITS | NOTES |
|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | -1.0~7.0 | V | 1 |
| Output Voltage | $V_{OUT}$ | -1.0~7.0 | V | 1 |
| Power Supply Voltage | $V_{CC}$ | -1.0~7.0 | V | 1 |
| Operating Temperature | $T_{OPR}$ | .0~70 | °C | 1 |
| Storage Temperature | $T_{STG}$ | -55~125 | °C | 1 |
| Soldering Temperature·Time | $T_{SOLDER}$ | 260·10 | °C·sec | 1 |
| Power Dissipation | $P_D$ | 4.8 | W | 1 |
| Short Circuit Output Current | $I_{OUT}$ | 50 | mA | 1 |

## RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2 |
| $V_{IH}$ | Input High Voltage | 2.4 | - | 6.5 | V | 2 |
| $V_{IL}$ | Input Low Voltage | -1.0 | - | 0.8 | V | 2 |

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V ± 10%, Ta = 0~70°C)

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | OPERATING CURRENT<br>Average Power Supply Operating Current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}$ = $t_{RC}$ MIN.) | THM321020S-80 | – | 840 | mA | 3, 4 |
| | | THM321020S-10 | – | 720 | | |
| $I_{CC2}$ | STANDBY CURRENT<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | | – | 16 | mA | |
| $I_{CC3}$ | $\overline{RAS}$ ONLY REFRESH CURRENT<br>Average Power Supply Current, $\overline{RAS}$ Only Mode<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IH}$: $t_{RC}$ = $t_{RC}$ MIN.) | THM321020S-80 | – | 840 | mA | 3 |
| | | THM321020S-10 | – | 720 | | |
| $I_{CC4}$ | FAST PAGE MODE CURRENT<br>Average Power Supply Current, Fast Page Mode<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC}$ = $t_{PC}$ MIN.) | THM321020S-80 | – | 560 | mA | 3, 4 |
| | | THM321020S-10 | – | 480 | | |
| $I_{CC5}$ | STANDBY CURRENT<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ – 0.2V) | | – | 8 | mA | |
| $I_{CC6}$ | $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT<br>Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$<br>Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}$ = $t_{RC}$ MIN.) | THM321020S-80 | – | 840 | mA | 3 |
| | | THM321020S-10 | – | 720 | | |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT<br>Input Leakage Current, any Input<br>(0V ≤ $V_{IN}$ ≤ 6.5V, All Other Pins not under Test = 0V) | | – 80 | 80 | µA | |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT<br>($D_{OUT}$ is disabled, 0V ≤ $V_{OUT}$ ≤ 5.5V) | | – 10 | 10 | µA | |
| $I_{OH}$ | OUTPUT LEVEL<br>Output "H" Level Voltage ($I_{OUT}$ = – 5mA) | | 2.4 | – | V | |
| $V_{OL}$ | OUTPUT LEVEL<br>Output "L" Level Voltage ($I_{OUT}$ = 4.2mA) | | – | 0.4 | V | |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC}$ = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

| SYMBOL | PARAMETER | THM3210205-80 | | THM3210205-10 | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| $t_{RC}$ | Random Read or Write Cycle Time | 150 | - | 180 | - | ns | |
| $t_{PC}$ | Fast Page Mode Cycle Time | 50 | - | 60 | - | ns | |
| $t_{RAC}$ | Access Time from $\overline{RAS}$ | - | 80 | - | 100 | ns | 8, 13 |
| $t_{CAC}$ | Access Time from $\overline{CAS}$ | - | 20 | - | 25 | ns | 8, 13 |
| $t_{AA}$ | Access Time from Column Address | - | 40 | - | 50 | ns | 8, 14 |
| $t_{CPA}$ | Access Time from $\overline{CAS}$ Precharge | - | 45 | - | 55 | ns | 8 |
| $t_{CLZ}$ | $\overline{CAS}$ to Output in Low-Z | 0 | - | 0 | - | ns | 8 |
| $t_{OFF}$ | Output Buffer Turn-off Delay | 0 | 20 | 0 | 20 | ns | 9 |
| $t_T$ | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | ns | 7 |
| $t_{RP}$ | $\overline{RAS}$ Precharge Time | 60 | - | 70 | - | ns | |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 80 | 10,000 | 100 | 10,000 | ns | |
| $t_{RASP}$ | $\overline{RAS}$ Pulse Width (Fast Page Mode) | 80 | 200,000 | 100 | 200,000 | ns | |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time | 20 | - | 25 | - | ns | |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time | 80 | - | 100 | - | ns | |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 20 | 10,000 | 25 | 10,000 | ns | |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | 20 | 60 | 25 | 75 | ns | 13 |
| $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time | 15 | 40 | 20 | 50 | ns | 14 |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | - | 10 | - | ns | |
| $t_{CP}$ | $\overline{CAS}$ Precharge Time (Fast Page Mode) | 10 | - | 10 | - | ns | |
| $t_{ASR}$ | Row Address Set-Up Time | 0 | - | 0 | - | ns | |
| $t_{RAH}$ | Row Address Hold Time | 10 | - | 15 | - | ns | |
| $t_{ASC}$ | Column Address Set-Up Time | 0 | - | 0 | - | ns | |
| $t_{CAH}$ | Column Address Hold Time | 15 | - | 20 | - | ns | |
| $t_{AR}$ | Column Address Hold Time referenced to $\overline{RAS}$ | 60 | - | 75 | - | ns | |
| $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time | 40 | - | 50 | - | ns | |
| $t_{RCS}$ | Read Command Set-Up Time | 0 | - | 0 | - | ns | |
| $t_{RCH}$ | Read Command Hold Time | 0 | - | 0 | - | ns | 10 |
| $t_{RRH}$ | Read Command Hold Time referenced to $\overline{RAS}$ | 0 | - | 0 | - | ns | 10 |
| $t_{WCH}$ | Write Command Hold Time | 15 | - | 20 | - | ns | |
| $t_{WCR}$ | Write Command Hold Time referenced to $\overline{RAS}$ | 60 | - | 75 | - | ns | |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

| SYMBOL | PARAMETER | THM321020S-80 | | THM321020S-10 | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| $t_{WP}$ | Write Command Pulse Width | 15 | - | 20 | - | ns | |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 20 | - | 25 | - | ns | |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 20 | - | 25 | - | ns | |
| $t_{DS}$ | Date Set-Up Time | 0 | - | 0 | - | ns | 11 |
| $t_{DH}$ | Date Hold Time | 15 | - | 20 | - | ns | 11 |
| $t_{DHR}$ | Data Hold Time referenced to $\overline{RAS}$ | 60 | - | 75 | - | ns | |
| $t_{REF}$ | Refresh Period | - | 16 | - | 16 | ms | |
| $t_{WCS}$ | Write Command Set-UP Time | 0 | - | 0 | - | ns | 12 |
| $t_{CSR}$ | $\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 5 | - | 10 | - | ns | |
| $t_{CHR}$ | $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 15 | - | 20 | - | ns | |
| $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 0 | - | 0 | - | ns | |
| $t_{CPT}$ | $\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle) | 40 | - | 50 | - | ns | |
| $t_{WRP}$ | $\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 10 | - | 10 | - | ns | |
| $t_{WRH}$ | $\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle) | 10 | - | 10 | - | ns | |

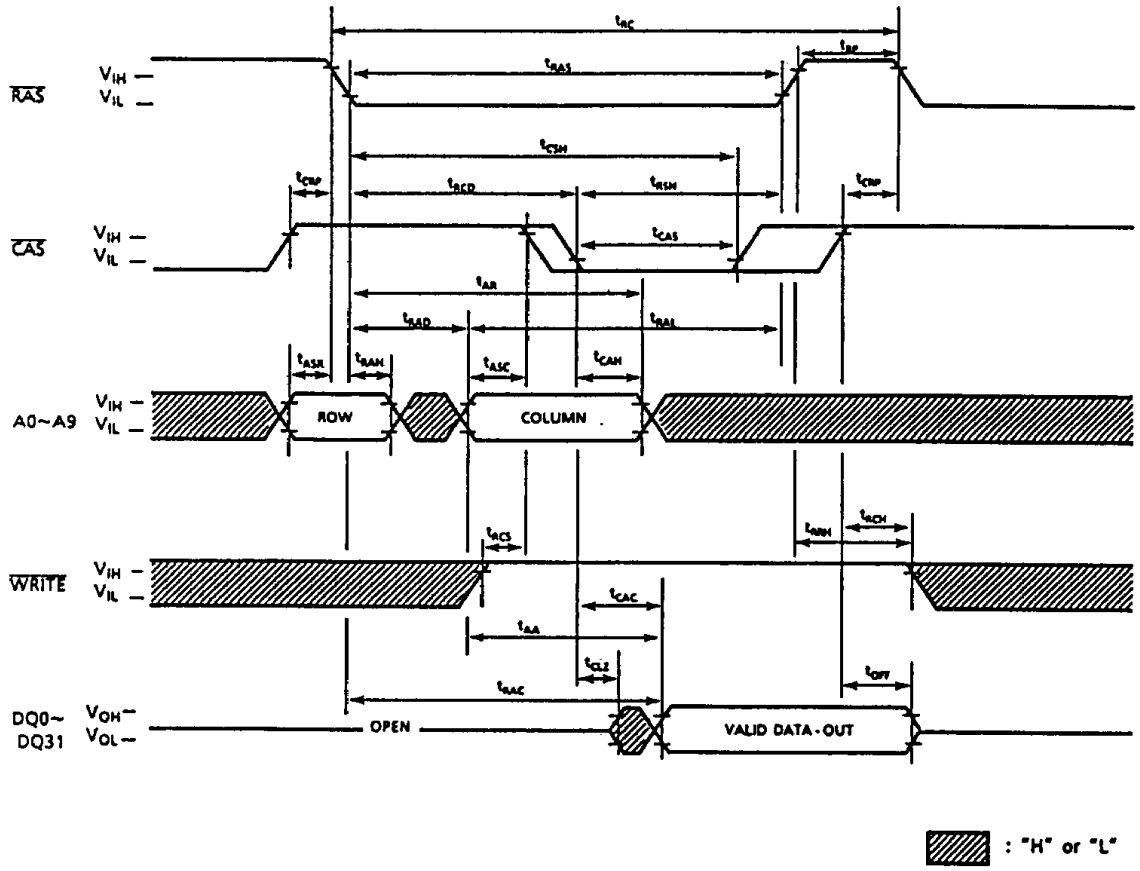
CAPACITANCE ($V_{CC}$ = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| CI1 | Input Capacitance (A0~A9) | - | 88 | pF |
| CI2 | Input Capacitance ($\overline{W}$) | - | 84 | pF |
| CI3 | Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$) | - | 42 | pF |
| CI4 | Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$) | - | 36 | pF |
| CDQ1 | I/O Capacitance (DQ0~31) | - | 17 | pF |

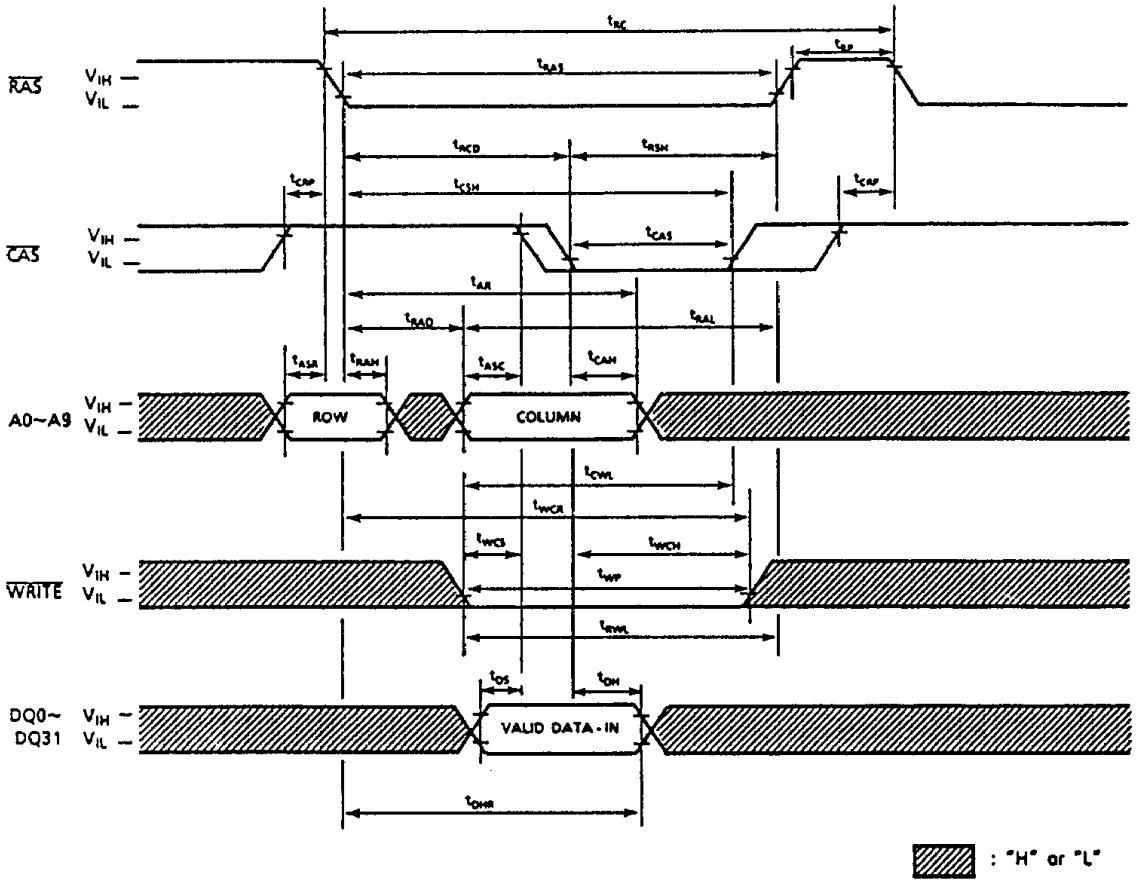
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to $V_{SS}$.
3. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, $I_{CC6}$ depend on cycle rate.
4. $I_{CC1}$, $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T$=5ns.
7. $V_{IH}$(min.) and $V_{IL}$(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. $t_{OFF}$(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. $t_{WCS}$ is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the $t_{RCD}$(max.) limit insures that $t_{RAC}$(max.) can be met. $t_{RCD}$(max.) is specified as a reference point only: If $t_{RCD}$ is greater than the specified $t_{RCD}$(max.) limit, then access time is controlled by $t_{CAC}$.
14. Operation within the $t_{RAD}$(max.) limit, insures that $t_{RAC}$(max.) can be met. $t_{RAD}$(max.) is specified as a reference point only: If $t_{RAD}$ is greater than the specified $t_{RAD}$(max.) limit, then access time is controlled by $t_{AA}$.

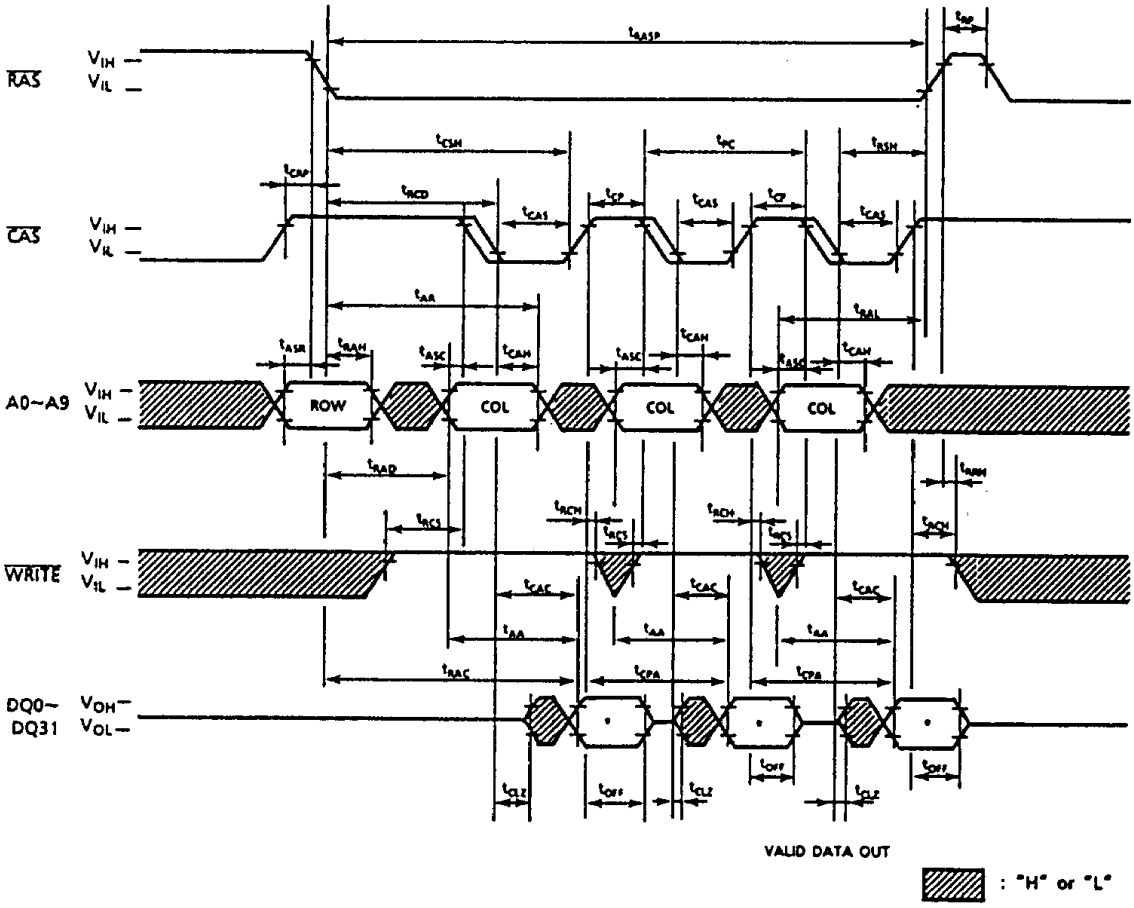
READ CYCLE


RAS
CAS
A0~A9
WRITE
DQ0~ DQ31
ROW
COLUMN
OPEN
VALID DATA-OUT
: "H" or "L"

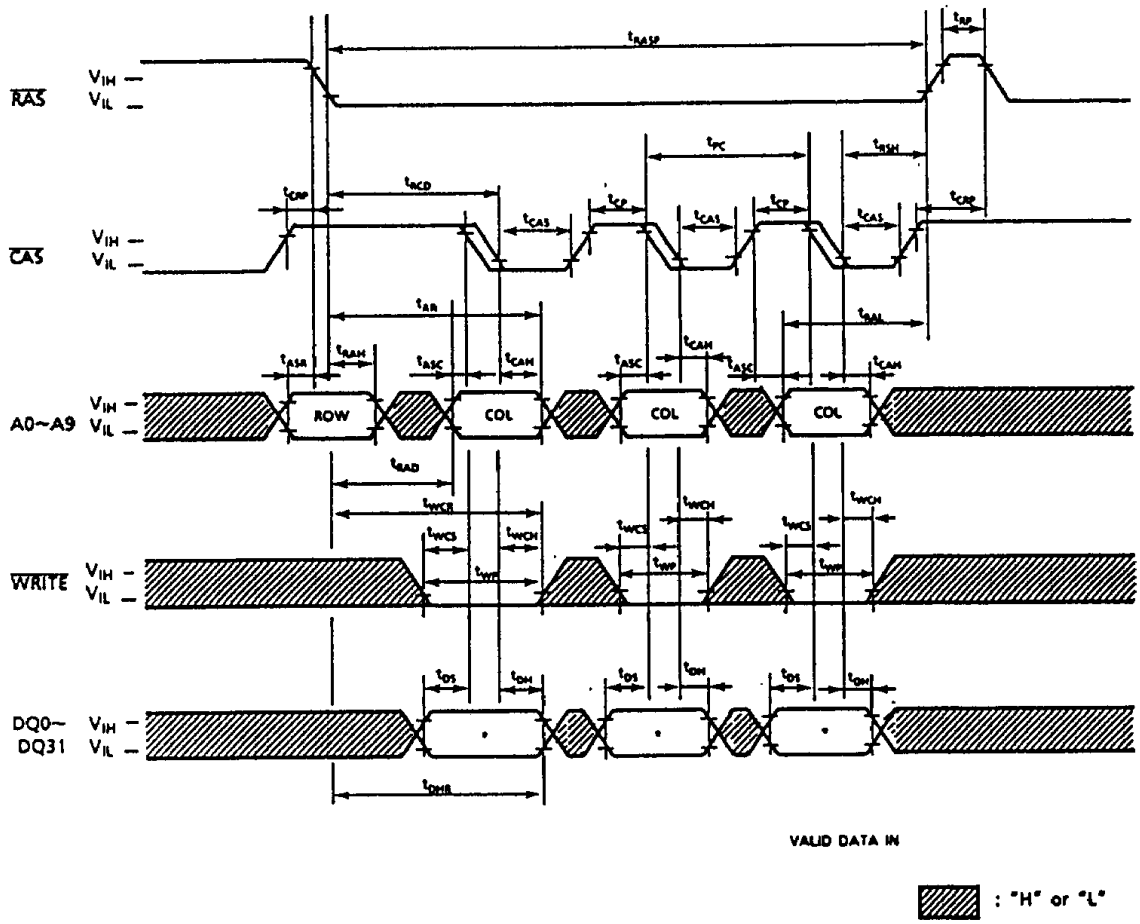
EARLY WRITE CYCLE



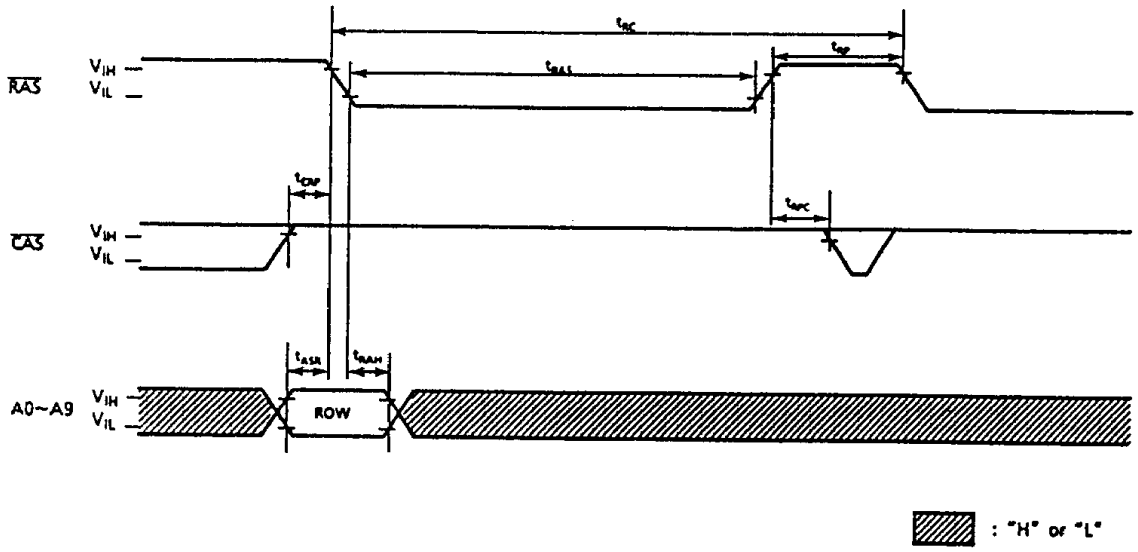
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

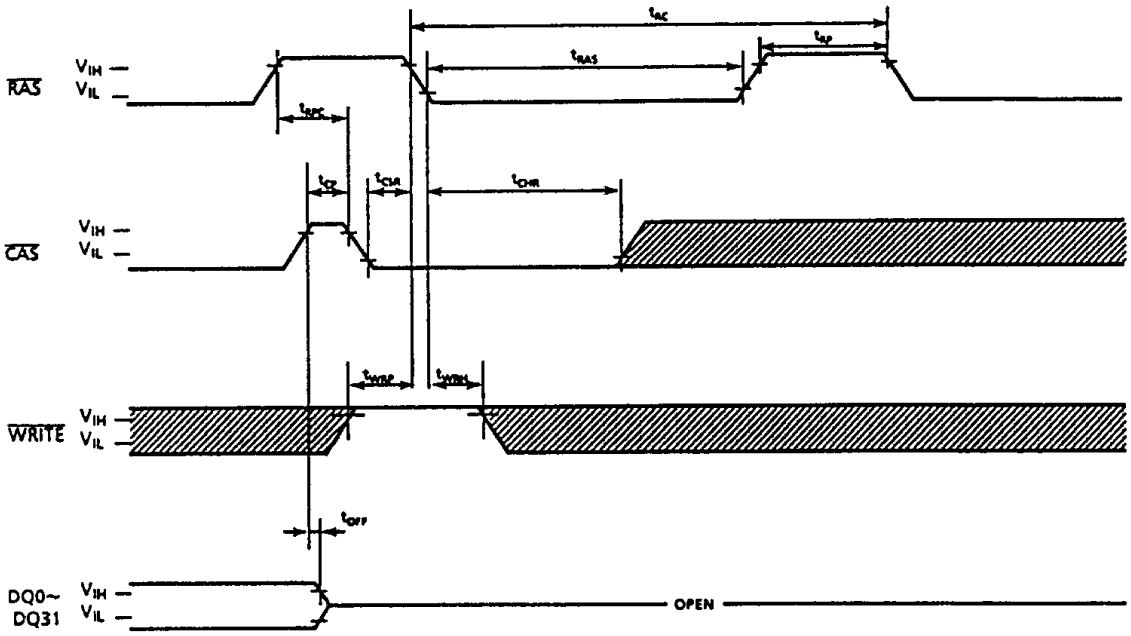


## $\overline{RAS}$ ONLY REFRESH CYCLE




Note: $\overline{WRITE}$ = "H" or "L"

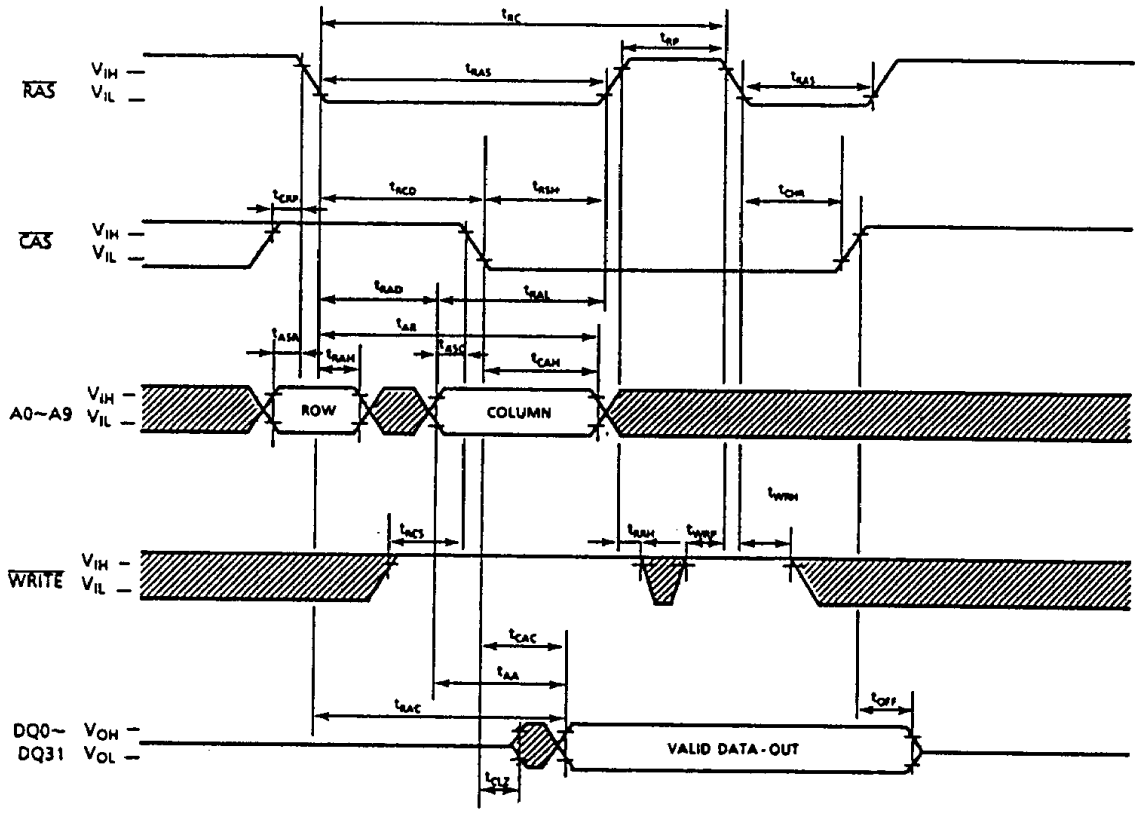
## $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE




: "H" or "L"

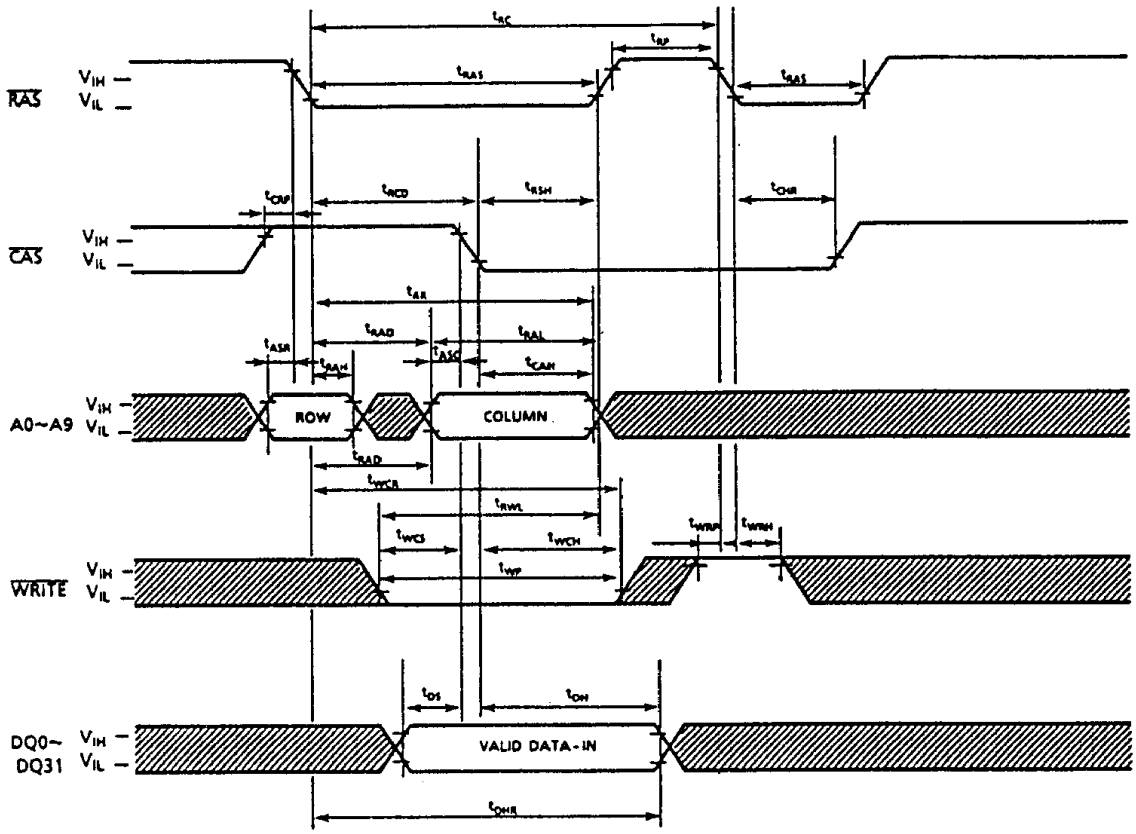
Note: A0~A9 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

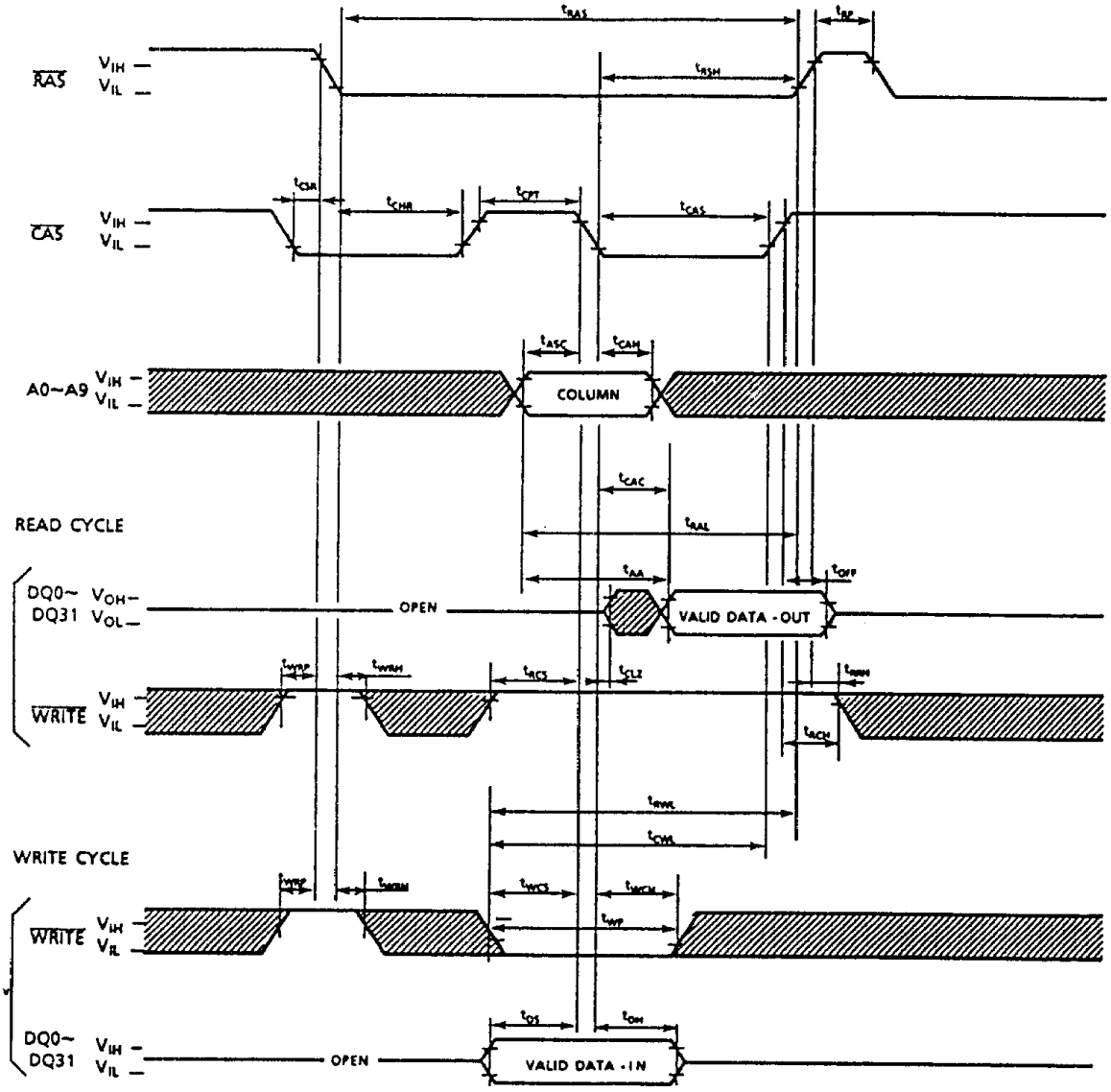



: "H" or "L"

HIDDEN REFRESH CYCLE (WRITE)



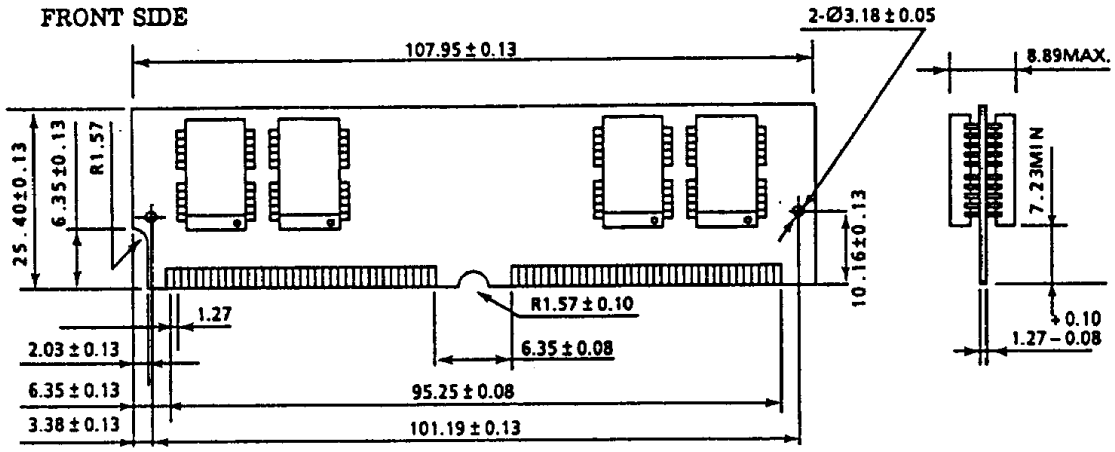
## CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



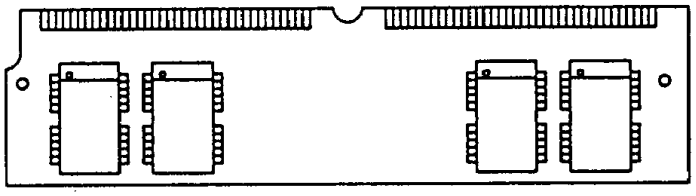
## OUTLINE DRAWINGS

Unit in mm

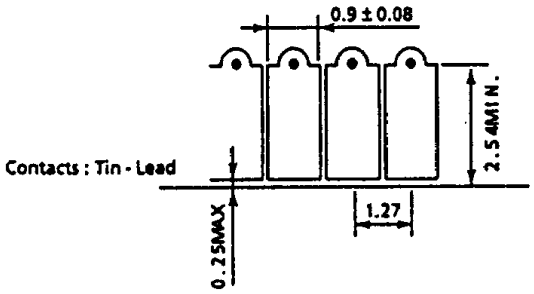
FRONT SIDE




BACK SIDE



• THM321020S




• THM321020SG