TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

128 GBIT (4G × 8 x 4 BIT) CMOS NAND E^2PROM (Multi-Level-Cell)

DESCRIPTION

The TH58NVG7D2F is a single 3.3 V 128Gbit (145,096,704,000 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) organized as (8192 + 448) bytes × 128 pages × 16,400blocks. The device has two 8640-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 8640-byte increments. The Erase operation is implemented in a single block unit (1 Mbytes + 56 Kbytes: 8640 bytes × 128 pages).

The TH58NVG7D2F is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization
  TH58NVG7D2F
  Memory cell array 8640 × 2,050K × 8
  Register 8640 × 8
  Page size 8640 bytes
  Block size (1M + 56 K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy,
  Multi Page Program, Multi Block Erase, Multi Page Copy, Mullti Page Read

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 15,744 blocks
  Max 16,400 blocks

- Power supply
  V_{CC} = 2.7 V to 3.6 V

- Access time
  Cell array to register 250 μs max
  Serial Read Cycle 25 ns min

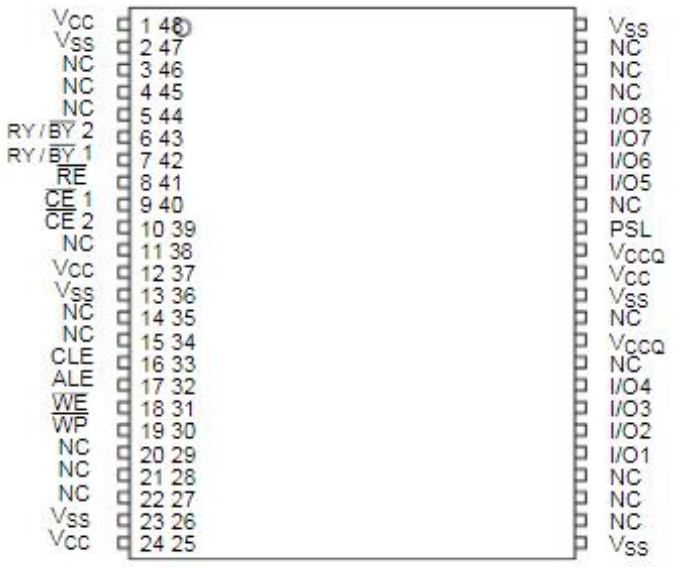
- Program/Erase time
  Auto Page Program 1600 μs/page typ.
  Auto Block Erase 4 ms/block typ.

- Operating current
  Read (25 ns cycle) TBD (50 mA max.) per 1chip
  Program (avg.) TBD (50 mA max.) per 1chip
  Erase (avg.) TBD (50 mA max.) per 1chip
  Standby 200 μA max

- Package
  (Weight: TBD g typ.)

- FOR RELIABILITY GUIDANCE, PLEASE REFER TO THE APPLICATION NOTES AND COMMENTS (17).
  24 bit ECC for each 1024 bytes is required.

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$ 1	Chip enable (Chip A,B)
$\overline{CE}$ 2	Chip enable (Chip C,D)
$\overline{WE}$ Write	enable
$\overline{RE}$ Read	enable
CLE Command	latch enable
ALE Address	latch enable
PSL	Power on select
$\overline{WP}$ Write	protect
RY/$\overline{BY}$ 1 Ready/Busy	(Chip A,B)
RY/$\overline{BY}$ 2	Ready/Busy (Chip C,D)
V_{CC} Power	supply
V_{CCQ}	I/O port Power supply
V_{SS} Ground	

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 V to V_{CC} + 0.3 V (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	-55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f= 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	40 pF	
C_{OUT}	Output	V_{OUT} = 0 V	—	40 pF	

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	15,744	—	16,400	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over the device lifetime.
* The number of valid blocks includes extended blocks.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage		2.7 V	— 3.6	V	V
V_{IH}	High Level input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	0.8 x Vcc	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	−0.3*	—	0.2 x Vcc	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0 to 70□ , V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO0} *1, *2	Power On Reset Current	PSL = GND or NU	—	— TBD		mA
		PSL = V_{CC}, FFh command input after Power On	—	— TBD		mA
I_{CCO1} *2	Serial Read Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 30 ns	—	— TBD		mA
I_{CCO2} *2	Programming Current	—	—	— TBD		mA
I_{CCO3} *2	Erasing Current	—	—	— TBD		mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0 V/V_{CC}, PSL = 0 V/V_{CC}/NU	—	— 200		μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4	—	— V	
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	— 0.4		V
I_{OL} (RY/$\overline{BY}$)	Output current of RY/$\overline{BY}$ pin	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)	— 8		— mA	

*1 Refer to application note (2) for detail

*2 Icco0/1/2/3 are the value of one chip, and an unselected chip is in Standy mode.

Package Dimensions

TSOP I 48-P-1220-0.50 Unit : mm