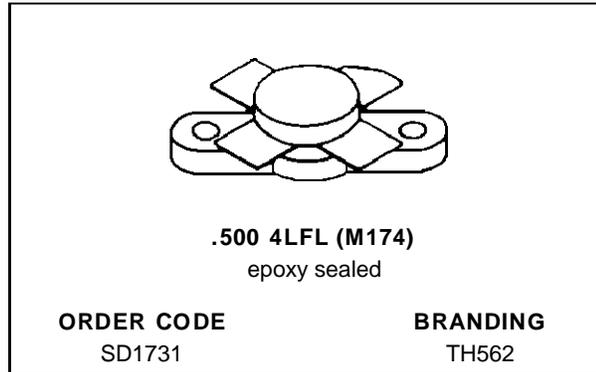


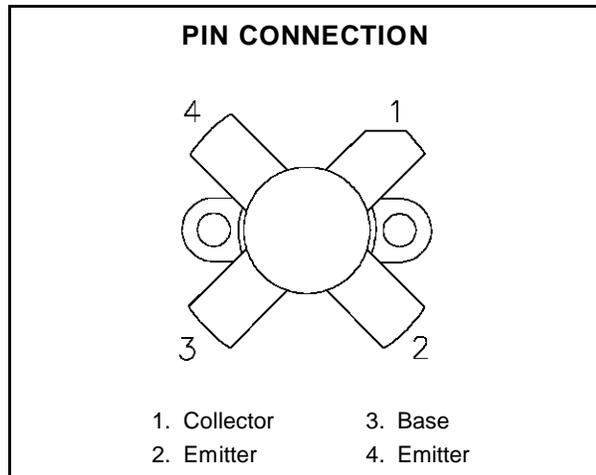
RF & MICROWAVE TRANSISTORS HF SSB APPLICATIONS

- OPTIMIZED FOR SSB
- 30 MHz
- 50 VOLTS
- EFFICIENCY 40%
- COMMON EMITTER
- GOLD METALLIZATION
- $P_{OUT} = 220$ W PEP WITH 13 dB GAIN



DESCRIPTION

The SD1731 is a 50 V epitaxial silicon NPN planar transistor designed primarily for SSB communications. This device utilizes emitter ballasting for improved ruggedness and reliability.



ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	110	V
V_{CEO}	Collector-Emitter Voltage	55	V
V_{EBO}	Emitter-Base Voltage	4.0	V
I_C	Device Current	20	A
P_{DISS}	Power Dissipation ($T_{heatsink} \leq 25^{\circ}C$)	233	W
T_J	Junction Temperature	+200	$^{\circ}C$
T_{STG}	Storage Temperature	- 65 to +150	$^{\circ}C$

THERMAL DATA

$R_{TH(j-c)}$	Junction-Case Thermal Resistance	0.55	$^{\circ}C/W$
$R_{TH(c-s)}$	Case-Heatsink Thermal Resistance	0.2	$^{\circ}C/W$

ELECTRICAL SPECIFICATIONS

STATIC ($T_{\text{case}} = 25^{\circ}\text{C}$)

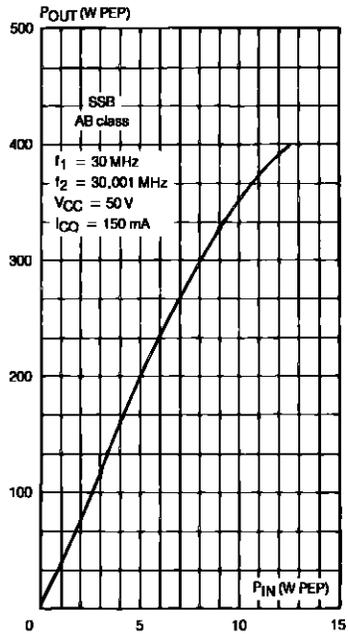
Symbol	Test Conditions		Value			Unit
			Min.	Typ.	Max.	
BV_{CBO}	$I_C = 200 \text{ mA}$	$I_E = 0 \text{ mA}$	110	—	—	V
BV_{CEO}	$I_C = 200 \text{ mA}$	$I_B = 0 \text{ mA}$	55	—	—	V
BV_{EBO}	$I_E = 20 \text{ mA}$	$I_C = 0 \text{ mA}$	4.0	—	—	V
I_{CEO}	$V_{CE} = 30 \text{ V}$	$I_E = 0 \text{ mA}$	—	—	5	mA
I_{CES}	$V_{CE} = 55 \text{ V}$	$I_E = 0 \text{ mA}$	—	—	10	mA
h_{FE}	$V_{CE} = 6 \text{ V}$	$I_C = 10 \text{ A}$	15	—	80	—

DYNAMIC ($T_{\text{heatsink}} = 25^{\circ}\text{C}$)

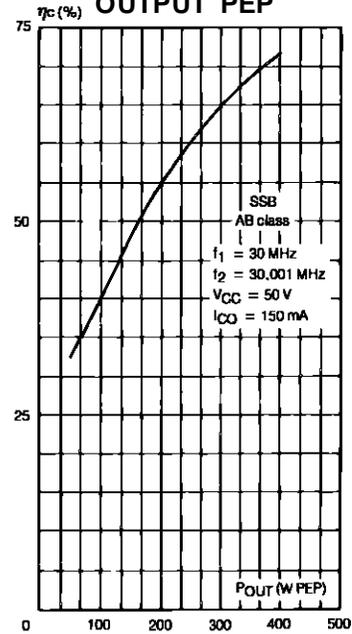
Symbol	Test Conditions			Value			Unit
				Min.	Typ.	Max.	
P_{OUT}	$f = 30 \text{ MHz}$	$V_{CE} = 50 \text{ V}$	$I_{CQ} = 150 \text{ mA}$	220	—	—	W
G_P^*	$P_{OUT} = 220 \text{ W PEP}$	$V_{CE} = 50 \text{ V}$	$I_{CQ} = 150 \text{ mA}$	13	—	—	dB
IMD^*	$P_{OUT} = 220 \text{ W PEP}$	$V_{CE} = 50 \text{ V}$	$I_{CQ} = 150 \text{ mA}$	—	—	-30	dBc
η_c^*	$P_{OUT} = 220 \text{ W PEP}$	$V_{CE} = 50 \text{ V}$	$I_{CQ} = 150 \text{ mA}$	40	—	—	%
C_{OB}	$f = 1 \text{ MHz}$	$V_{CB} = 50 \text{ V}$		—	330	—	pf

TYPICAL PERFORMANCE

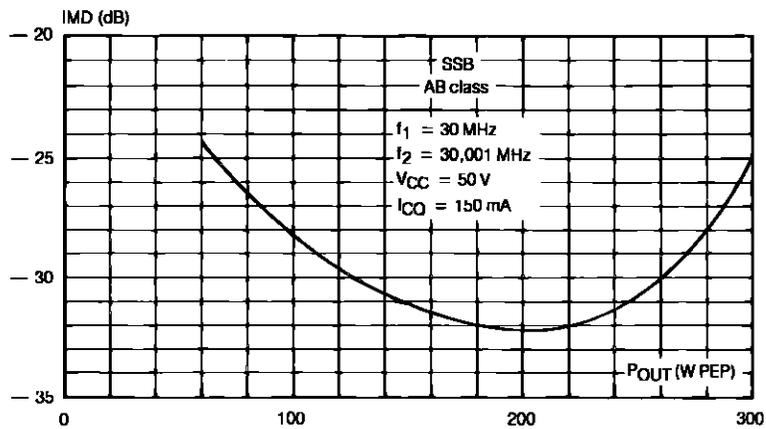
POWER OUTPUT PEP vs POWER INPUT



COLLECTOR EFFICIENCY vs POWER OUTPUT PEP

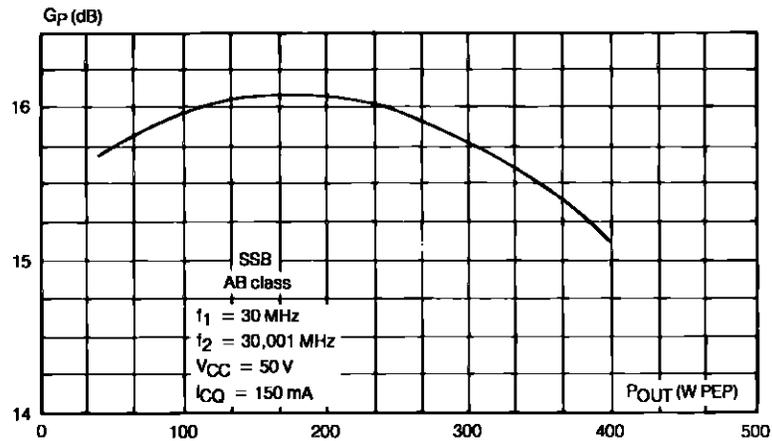


INTERMODULATION DISTORTION vs POWER OUTPUT PEP

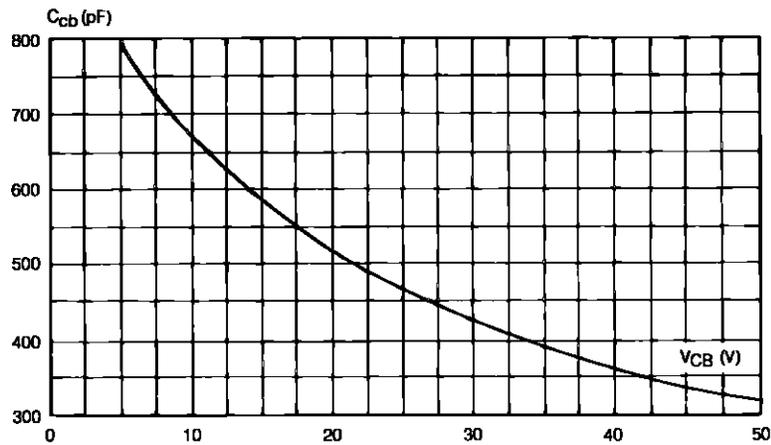


TYPICAL PERFORMANCE

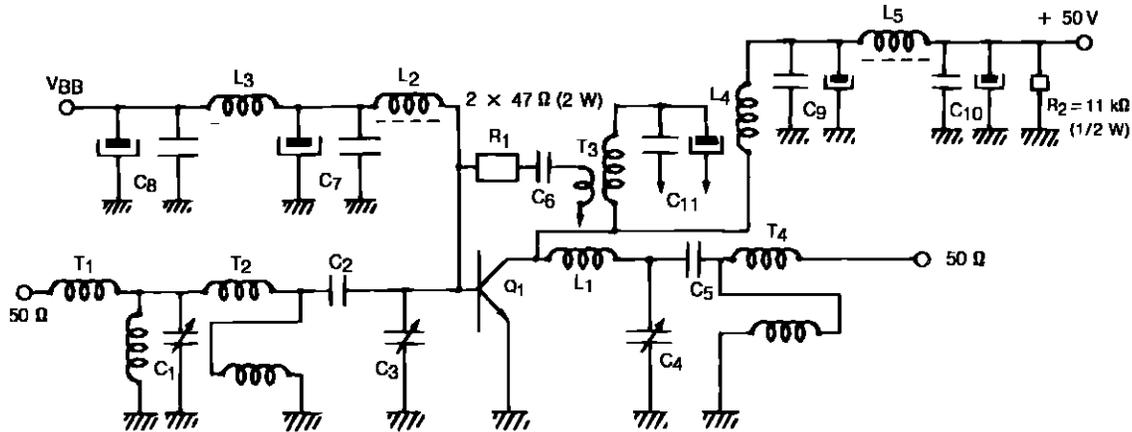
POWER GAIN vs POWER OUTPUT PEP



COLLECTOR BASE CAPACITANCE vs COLLECTOR EMITTER VOLTAGE

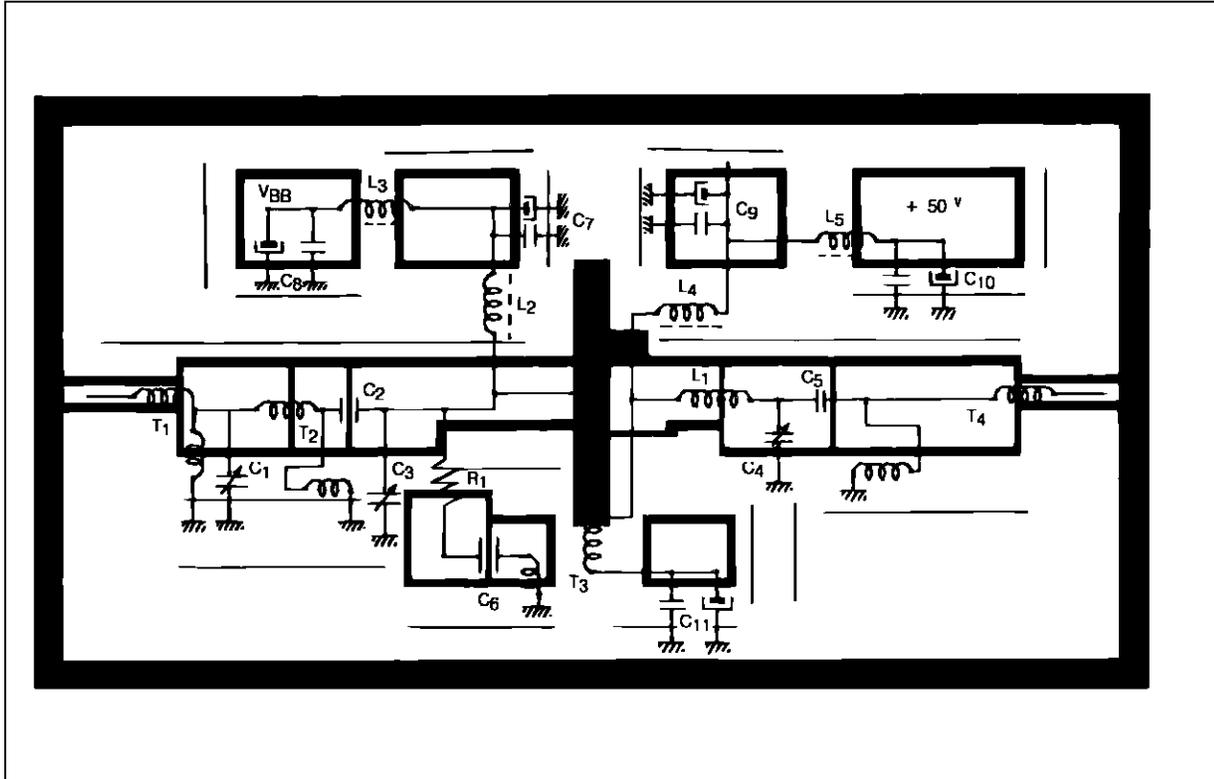


TEST CIRCUIT

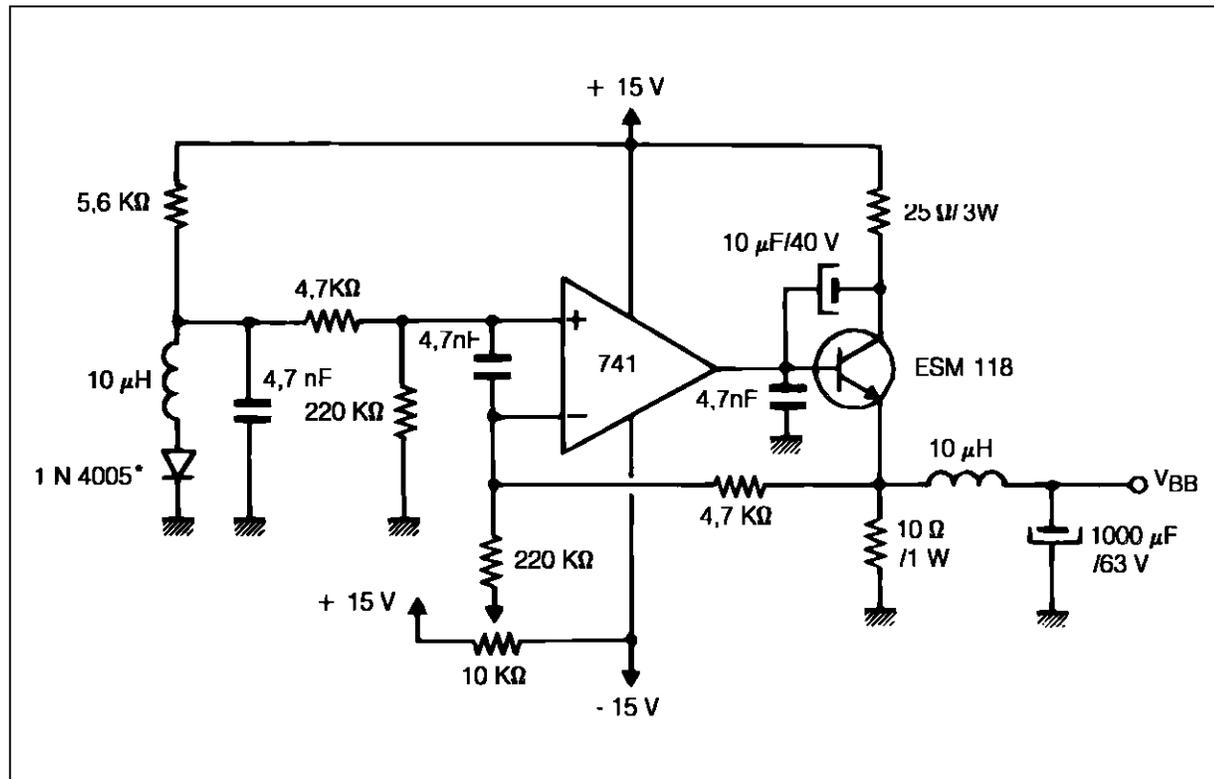


- | | | | |
|----------------------|--|----|--|
| C1 | : Arco 426 + 220pF + 330pF Chips | L4 | : 10 Turns of 1.2mm Enameled Wire, Diameter 8.1mm, Length 20mm |
| C2 | : 2 x 10nF Chips | L5 | : 7 Turns of 1.2mm Enameled Wire on Ferrite Core Phillips 4C6 97180 |
| C3 | : Arco 4615 + 2.2nF + 2 x 1nF LCC + 4.7nF + 560pF Chips | T1 | : 6:3.5 Impedance Transformer on toroid Phillips 4C6 97180 |
| C4 | : Arco 4213 + 330pF Chip | T2 | : Twisted Pair 4:1 Transformer, 4 Turns Made with 1.0mm Enameled on toroid Phillips 4C6 97180 |
| C5 | : 10nF Chip | T3 | : Feedback Transformer
Primary: 2 Turns of 1mm Enameled Wire
Secondary: 8 Turns of 1mm Enameled Wire |
| C6 | : 3 x 10nF Chips | T4 | : Twisted Pair 4:1 Transformer, 4 Turns of bifilar Twisted 1.2mm Wires on Ferrite Core Phillips 4C6 97200 |
| C7, C8, C9, C10, C11 | : 1nF + 10nF + 100nF + 4.7μF, 63V + 100μF, 63V | | |
| L1 | : 3 Turns of 1.2mm Unenameled Wire Diameter, 7.1mm, Length 13mm | | |
| L2, L3 | : 8 Turns of 0.55mm Enameled Wire on Ferrite Core Phillips 4C6 97170 (9 x 6 x 3) | | |

MOUNTING CIRCUIT

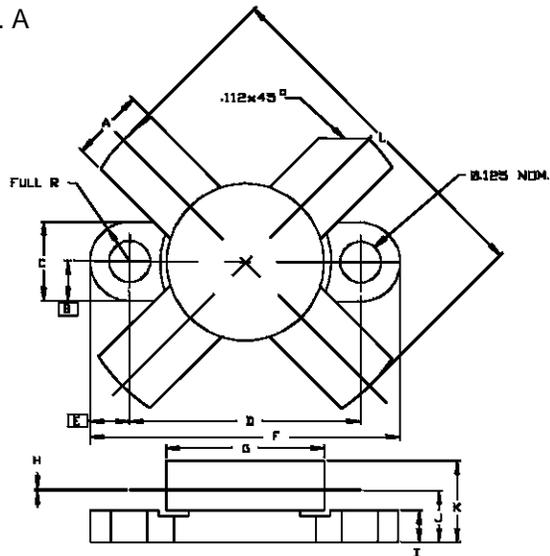


BIAS CIRCUIT



PACKAGE MECHANICAL DATA

Ref.: Dwg. No.12-0174 rev. A



SGS-THOMSON MICROELECTRONICS		CONT'D		
	MINIMUM Inches/mm	MAXIMUM Inches/mm		
A	.220/5,59	.230/5,84	K	.280/7,11
B	.125/3,18		L	1.050/26,67
C	.245/6,22	.255/6,48		
D	.720/18,28	.730/18,54		
E	.125/3,18			
F	.970/24,64	.980/24,89		
G	.495/12,57	.505/12,83		
H	.003/0,08	.007/0,18		
I	.090/2,29	.110/2,79		
J	.160/4,06	.175/4,45		

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