Trident

TGUI9440-3™ GUI ACCELERATOR

Product Brief

Features

Complete Hardware Compatibility

- PCI Rev 2.1 and ISA bus compliant
- 100% IBM VGA compatible on BIOS, register, and hardware level
- 160 pin PQFP package

Highly Integrated Design

- 100% IBM compatible VGA core
- GUI accelerator
- Fully integrated 24 bit True Color DAC with color look-up table
- 256x18 color look-up table with HiColor and True Color bypass mode support
- 108 MHz programmable clock synthesizers for memory and video clocks
- Two wire interface to EEPROM or VESA DDC2B
- 32K integrated ROM BIOS; also allows external ROM

Accelerated Graphics Functions

- Optimized graphic functions for BitBLTs, line drawing, short stroke vectors, rectangle fills, and text transfer
- 256 Raster Operations (ROPs) for 8 bit pixel (pseudo color) and 15/16 bit pixel (HiColor) graphic modes
- Accelerated color expansion modes
- Hardware cursor (64x64x2 or 32x32x2)
- Built-in pattern register

Multimedia Support

- Video overlays through Feature Connector (FC); supports both input and output
- Palette snooping

Software Support

- Virtual screen utility

Extended Display Resolution

- High resolution display through 1280x1024-256, 1024x768-256, 1024x768-64K, and 800x600-64K colors, or 640x480-16M colors
- Extended text modes (80 or 132 columns by 25, 30, 43, or 60 rows)

Simple Bus Interface Support

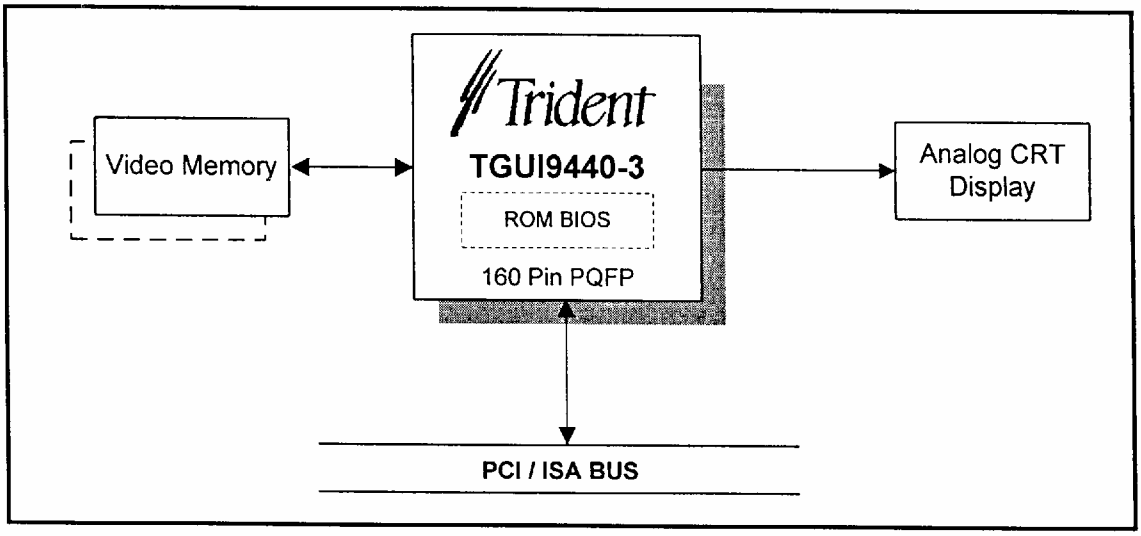
- Flexible Bus Interface Unit supports "glueless" connections to PCI and ISA buses with no additional TTL
- Linear display memory addressing
- Zero-wait state host write buffer and read cache
- PCI burst mode support

Flexible Display Memory Interface

- 1/2 MB, 1 MB, or 2 MB display memory configuration with memory densities of 256Kx4, 256Kx8, and 256Kx16
- Requires only one 256Kx16 DRAM for a 1024x768-16 color SVGA solution
- 32 bit memory bus interface with programmable DRAM timing up to 80 MHz

"Deep Green PC" Power Management

- VESA Display Power Management Signaling (DPMS) compatible
- Simple RAMDAC power down and clock idle register interface



TGUI9440-3 Application Diagram

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Overview

The Trident Graphic User Interface (GUI) TGUI9440-3 accelerator is a highly integrated, DRAM-based, graphic CRT controller for PCI and ISA bus interfaces. It provides a flexible, low cost, high performance solution for a diverse range of color depth, CRT resolution, and display memory configurations. Its highly innovative system design and full acceleration graphics engine dramatically improves GUI functions and significantly enhances overall system operation. Advanced system features such as Display Power Management Signaling (DPMS), 24 bit True Color DAC, dual clock synthesizer, minimal DRAM configuration, and extended color and text modes allow operation at peak performance levels. The TGUI9440-3 also supports standard BIOS modes, VESA palette snooping, and programmable DRAM timing. Additionally, its highly integrated design allows easy hardware connection for efficient development of high performance integrated video subsystems.

The 160 pin package and "glueless" interface makes the TGUI9440-3 well suited for motherboard applications and high-level add-on cards. The TGUI9440-3's enhanced feature set and flexible system configuration can be tailored for a wide range of design applications, making it an ideal solution for low to mid-range PCs running Microsoft® Windows® 3.1 and Windows 95, IBM®, OS/2™, and similar operating systems.

Accelerated Graphics Functions

The graphics engine of the TGUI9440-3 significantly boosts graphics performance through specialized hardware that accelerates the most frequently used GUI operations. Functions directly supported in hardware include BitBLT, image and text transfer, line draw, short stroke vector draw, and rectangle fills. Graphic functions are optimized further by a faster hardware cursor operation (64x64x2 or 32x32x2 pixel image) which offloads the CPU for other data manipulation jobs. The graphics engine also supports 256 Raster Operations (ROPs) for 8 and 16 bit pixel (HiColor) graphic modes. These advanced functions combine to allow performance increases up to five times greater than Super VGA designs, providing outstanding graphics acceleration in graphic intensive environments such as Microsoft Windows®.

Enhanced Display Capability

Display enhancements dramatically improve CRT resolution, providing sharp, high color images. These enhancements include support of 1280x1024-256, 1024x768-256, 1024x768-64K, 800x600-64k, or 640x480-16M colors for "full spectrum" color. Extended text modes of 80/132 columns by 25/30/43/60 rows provide an extended graphics area frequently used in many spreadsheet and database applications. The VESA Display Data Channel (VDDC) selects the most appropriate refresh rate for the monitor. A two (2) wire VESA DDC2B standard interface is provided as well, for easy graphics system configuration. Trident's Virtual Screen Utility provides panning and zooming to support virtual desktops. In addition, extended graphics and text modes are supported by software application drivers that provide a "ready-to-go" solution, minimizing the need for additional driver development.

A few of the many applications supported are listed below:

Windows 3.1	CADKEY™
Windows 95	Autoshade™
SCO X-Windows™	AutoCAD™
OS/2™ Warp	3D Studio V1, V2
Wordstar® V5.5-7.0	

Highly Integrated Design

The TGUI9440-3 is highlighted by a design integration consisting of four main elements: a RAMDAC which supports 24 bit True Color; a PLL based 108 MHz programmable clock synthesizer; a fully integrated GUI accelerator; and an on-chip BIOS for the add-on card market. The GUI accelerator includes a 256x18 color look-up table with high color and True Color bypass mode support, as well as a dual loop memory/video clock.

Since no TTL support is needed for the system bus or the display memory interface, this highly integrated design offers a "no-TTL" solution for simple, efficient, and cost-effective graphic subsystem designs, while simultaneously providing high performance for the IBM PC and compatible systems.

An additional feature is its integrated 32K mask ROM that can be disabled to interface with an external ROM.

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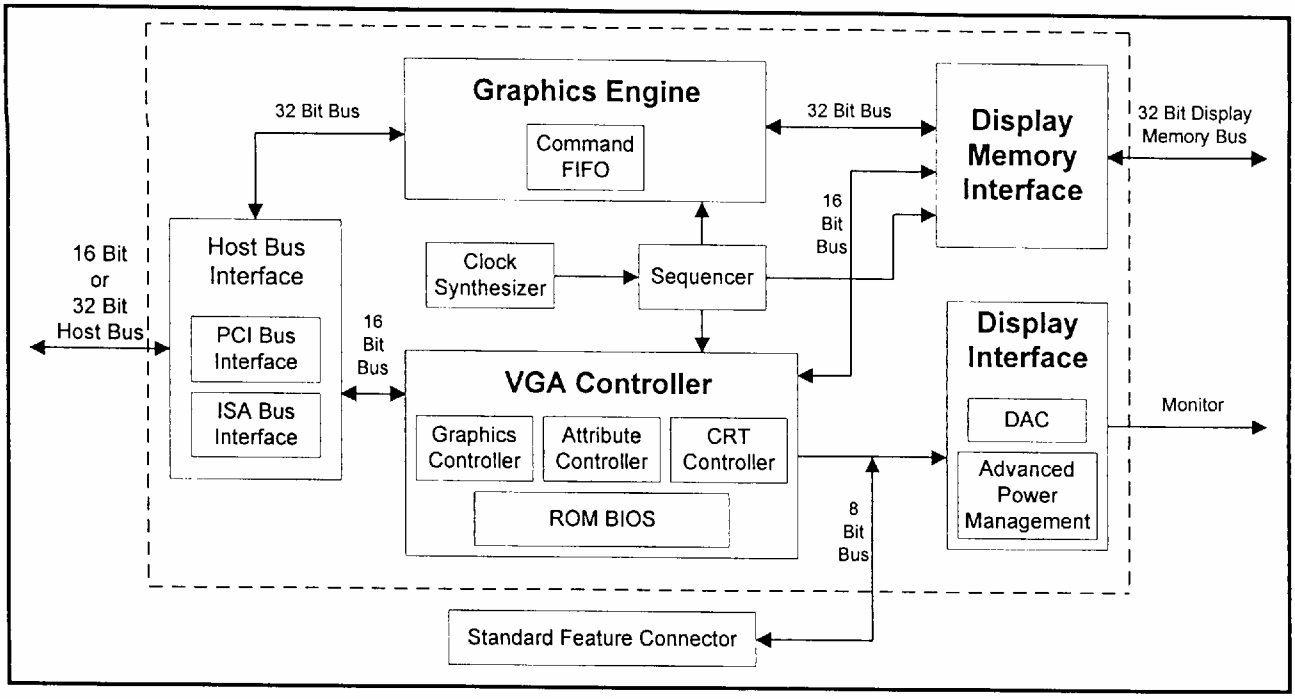

TGUI9440-3 Block Diagram

Optimized System Features

Compared with other devices in its class, the TGUI9440-3 offers many advanced features that optimize overall system operation such as linear display memory addressing, zero-wait state host write buffer, and read cache. All of these increase operating speeds and contribute to peak performance levels. Also, signature analysis performs system level test operations upon startup to verify interface connections to ensure correct system functionality. Graphics system throughput is further enhanced by a command FIFO, allowing maximum bus transfer speed for applications such as Microsoft Windows® or AutoCAD™ that directly access video memory.

Complete System Bus Support

A flexible Bus Interface Unit (BIU) supports ISA and 32 bit PCI bus interfaces and provides a low cost, single chip solution for all IBM PC and compatibles (PCI 2.1 bus speeds up to 33 MHz). Combined with "glueless" connections, the BIU allows an efficient design path for quick and easy integration to future generation PCs.

Multimedia Support

A built-in IBM Feature Connector port interfaces with the TGUI9440-3 DAC to support video overlay on graphics, or graphics output in video, by interfacing with chips such as the Trident PCView+. The TGUI9440-3 also supports palette snooping which is ideal for multimedia applications.

"Green PC" Power Management

The TGUI9440-3 supports VESA Display Power Management Signaling (DPMS), which decreases energy consumption when the device is in a temporary idle state. VESA DPMS power-down states (ready, standby, suspend, and off) specify HSYNC, VSYNC, clock and DAC operation through the DPMS BIOS interface and the utility software supplied by Trident.

Flexible Display Memory Interface

The TGUI9440-3 offers display memory configurations from ½ MB to 2 MB and supports a range of DRAM configurations from 256Kx4 to 512Kx16. A 32 bit memory bus interface and programmable DRAM timing provides a flexible interface that maximizes timing for increased performance. Additionally, a nominal DRAM interface requirement of one 256Kx16 DRAM for 1024x768-16 color SVGA minimizes chip count, system cost, and board space for cost-effective design solutions. The display memory interface also supports symmetrical or asymmetrical configurations and a Dual CAS/Dual WE DRAM configuration. Plus, a conventional "Fast Page" mode or "Fast Page mode with Extended Data Out" DRAM feature improves system performance by offering CPU access to the display memory at maximum bus bandwidth.