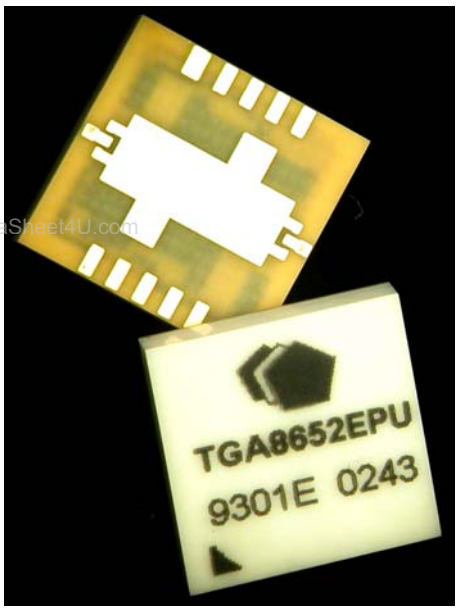
TriQuint SEMICONDUCTOR

Product Data Sheet
June 14, 2005

9.9-12.5Gb/s Optical Modulator Driver TGA8652-EPU-SL

OC-192 Metro and Long Haul Applications
Surface Mount Package



Key Features and Performance

- DC - 12 GHz Linear BW
- DC - 16 GHz Saturated Power BW
- 16 dB small signal gain
- Wide Drive Range (4V to 8V)
- 25 ps Edge Rates (10/90)
- Low Power Dissipation (1.4W at Vo=8V)
- Package size: .350 x .350 x .084 inches.
- Evaluation Board Available.

Primary Applications

- Mach-Zehnder Modulator Driver
- Pre-Driver
- Receiver AGC

Description

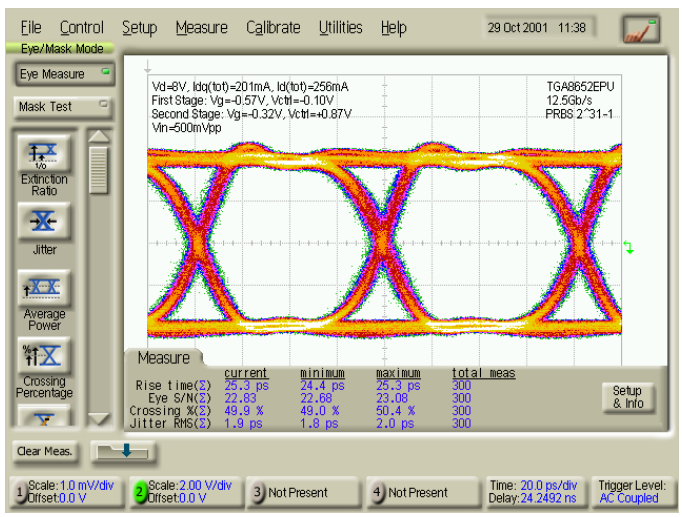
The TriQuint TGA8652-EPU is a medium power wideband AGC amplifier combined with off chip circuitry assembled in a Surface Mount Package. The TGA8652-EPU typically provides 16dB small signal gain with 6dB AGC range. Typical input and output return loss is <10dB. Typical Noise Figure is 2.5dB at 3GHz. Typical saturated output power is 25dBm. Small signal 3dB BW is 12GHz with saturated power performance to 16GHz. RF ports are DC coupled enabling the user to customize system corner frequencies. Applications include OC192 12.5GBit/s NRZ MZ Modulator Driver and receive AGC amplifier.

Drain bias may be applied thru the on-chip drain termination resistor for low drive applications or thru the RF output port for high drive applications. A cascaded pair demonstrated 8Vpp output voltage swing with 500mVpp at the input when stimulated with 10GBit/s. 2^31-1prbs. NRZ data.

The TGA8652-EPU is available on an evaluation board.

Measured Performance

Cascaded 8652 Evaluation Boards
12.5 Gb/s Performance
Output = 8 Vpp, Input = 500 mVpp
Scale: 2 V/div, 20 ps/div



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

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MAXIMUM RATINGS

SYMBOL	PARAMETER 1/	VALUE	NOTES
	POSITIVE SUPPLY VOLTAGE		
V^+	Drain bias applied thru on-chip termination	12 V	
Vd(RFout)	Drain bias applied at RF output using bias T	10 V	
	POSITIVE SUPPLY CURRENT		
V^+	Drain bias applied thru on-chip termination	110 mA	2/
Id	Drain bias applied at RF output using bias T	250 mA	
P_d	POWER DISSIPATION	2.4 W	3/
	NEGATIVE GATE		
Vg	Voltage	0 V to –3 V	
Ig	Gate Current	5 mA	
	CONTROL GATE		
Vctrl	Voltage	Vd/2 to –3 V	4/
Ictrl	Gate Current	5 mA	
	RF INPUT		
P_{IN}	Sinusoidal Continuous Wave Power	23 dBm	
T_{CH}	OPERATING CHANNEL TEMPERATURE	150 ^{0}C	5/ 6/
T_{STG}	STORAGE TEMPERATURE	-40 to 125 ^{0}C	

Notes:

1/ These ratings represent the maximum operable values for the device.

2/ Assure the combination of Vd and Id does not exceed maximum power dissipation rating.

3/ When operated at this bias condition with a base plate temperature of 80 ^{0}C, the Mean Time to Failure (MTTF) is reduced from 2.6E+7 to 1E+6 hours.

4/ Assure Vctrl never exceeds Vd during bias on and off sequences, and normal operation.

5/ These ratings apply to each individual FET.

6/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

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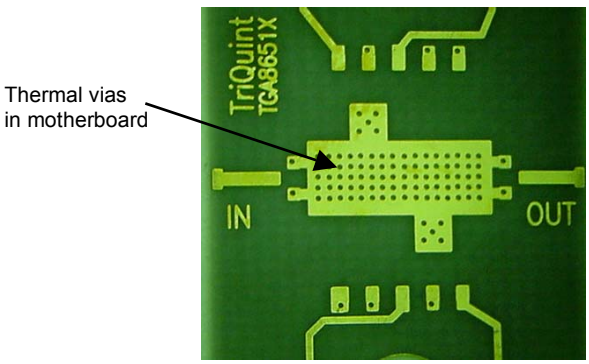
THERMAL INFORMATION*

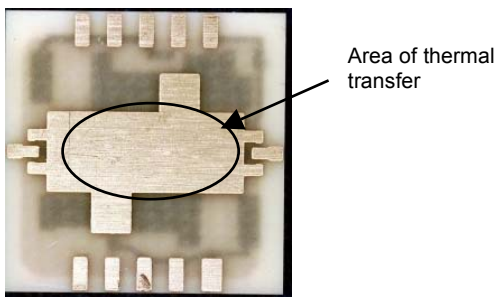
Parameter	Test Condition	T_{CH} (°C)	$R_{\theta JC}$ (°C/W)	MTTF (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of package)	Vd(RF out) = 6.5 V, Vctrl = 1 V, Id = 170 mA ± 5%, T_{base} = 80 °C	114.70	31.40	2.6E+7

NOTE: Thermal transfer is conducted thru the bottom of the TGA8652-EPU package into the motherboard. Design the motherboard to assure adequate thermal transfer to the base plate. An array of filled thermal vias is recommended as shown in the example below.

* This information is a result of a thermal model.



Motherboard



Bottom View TGA8652-EPU

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RF SPECIFICATIONS

(T_A = 25°C Nominal)

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL SIGNAL BW			12		GHz
	SATURATED POWER BW			16		GHz
1/, 2/	SMALL-SIGNAL GAIN MAGNITUDE	2 and 4 GHz	15	16		dB
		6 GHz	13	15		
		10 GHz	13	14		
		14 GHz	10	13		
		16 GHz	10	13		
	SMALL SIGNAL AGC RANGE	Midband		15		dB
1/, 2/	INPUT RETURN LOSS MAGNITUDE	2, 4, 6, and 10 GHz	9	10		dB
		14 and 18 GHz	8	10		
1/, 2/	OUTPUT RETURN LOSS MAGNITUDE	2, 4, 6, and 10 GHz	10	10		dB
		14 and 18 GHz	8	10		
6/, 7/	SATURATED OUTPUT POWER	2, 4, 6, 8, and 10 GHz	25			dBm
3/, 4/	EYE AMPLITUDE	Vd (RFout) = 7 V	8.0			Vpp
		Vd (RFout) = 6 V	7.0			
		Vd (RFout) = 5 V	6.0			
		Vd (RFout) = 4.5 V	5.5			
3/, 4/, 5/	ADDITIVE JITTER (p-p)			5		ps
3/, 4/	RISE TIME (10/90)			25		ps

Notes:

1/ Verified at package level RF probe.

2/ Package Probe Bias: V^+ = 8 V, adjust Vg1 to achieve Id = 87 mA, Vctrl = +1 V

3/ Verified by design, TGA8652EPU assembled onto a demonstration board shown on page 7 then tested using the application circuit and bias procedure detailed on pages 8 and 9.

4/ Vin = 2 V, Data Rate = 12.5 Gb/s, Vctrl and Vg are adjusted for maximum output.

5/ Computed using RSS Method where Jpp_additive = SQRT(Jpp_out^2 - Jpp_in^2)

6/ Verified at die level on-wafer probe.

7/ Power Bias Die Probe: VDT=8 V, adjust Vg to achieve Id = 175 mA+/-5%, Vctrl = 1.5 V
Note: At the die level, drain bias is applied thru the RF output port using a bias tee, voltage is at the DC input to the bias tee.

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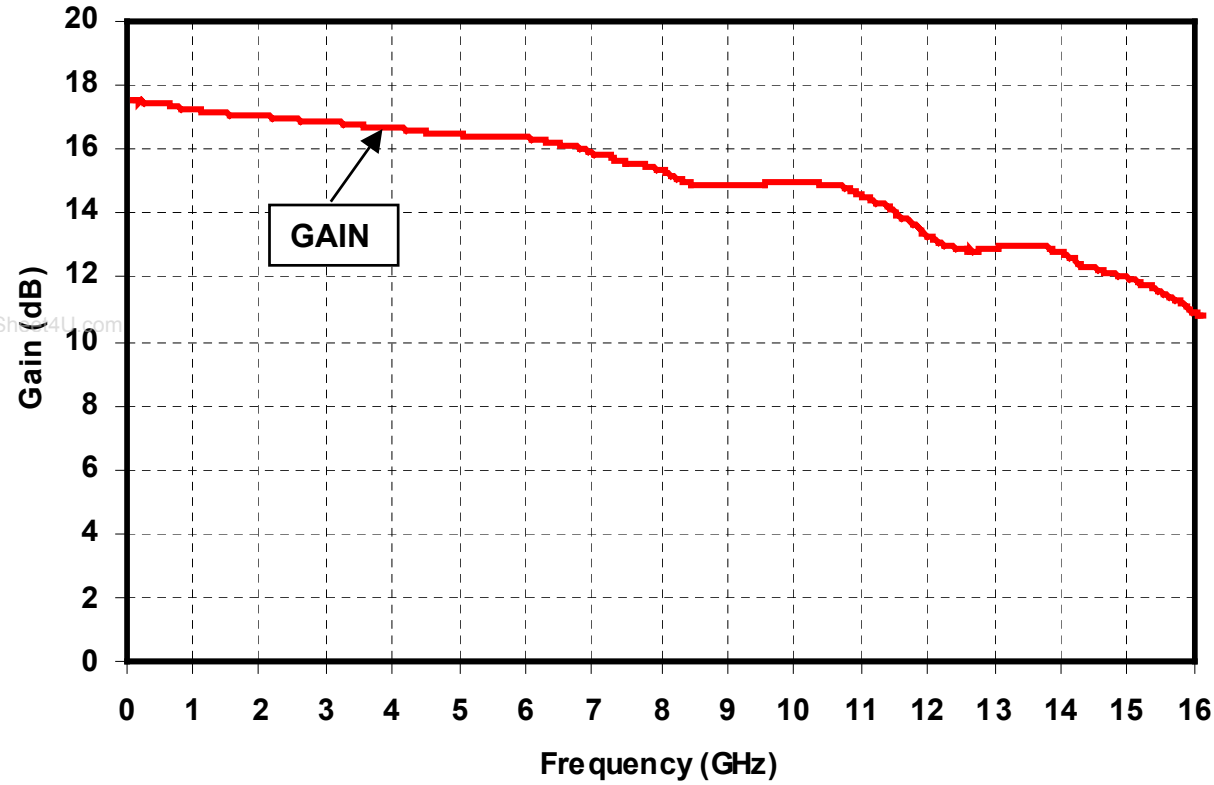
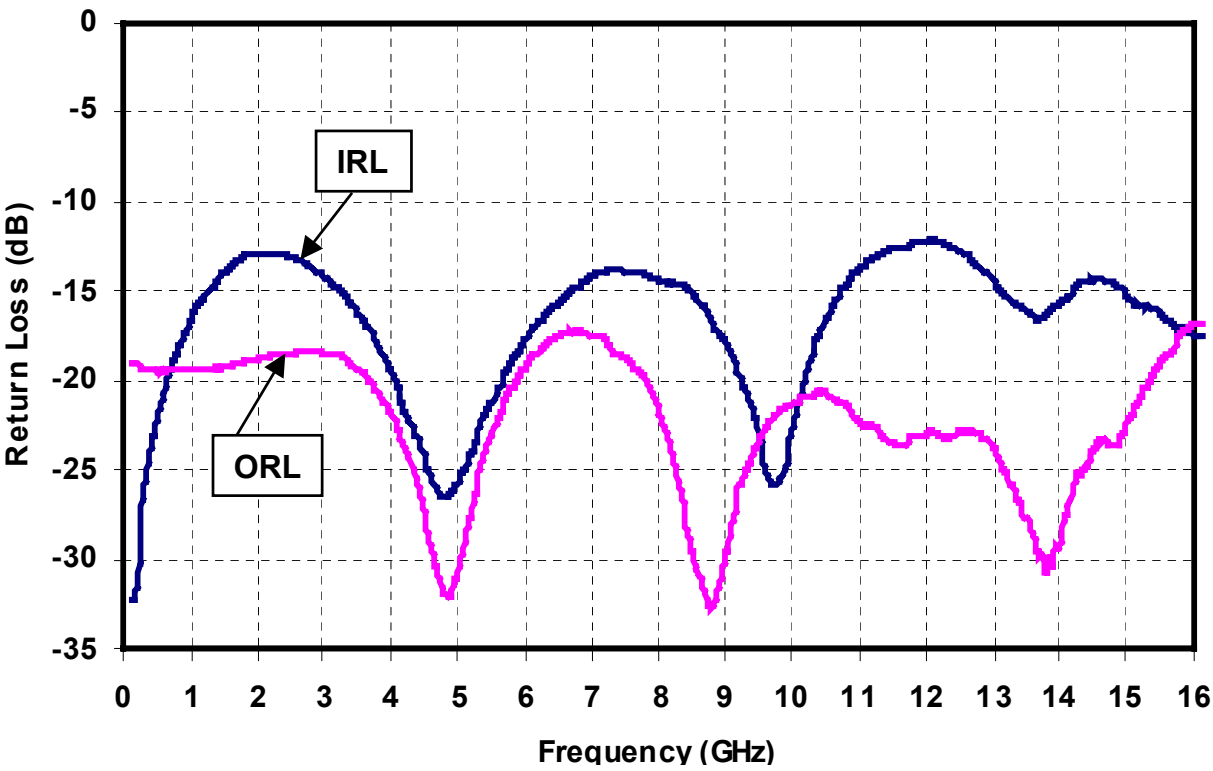
Typical Measured S-parameters





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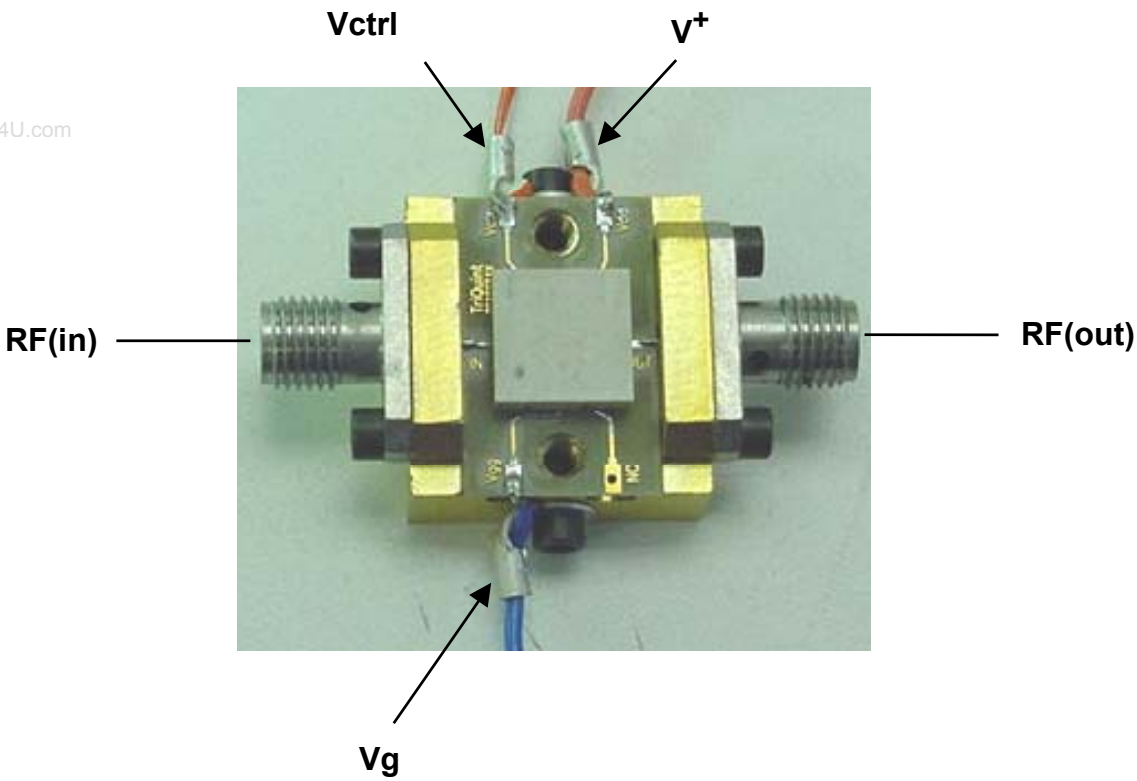
Demonstration Board



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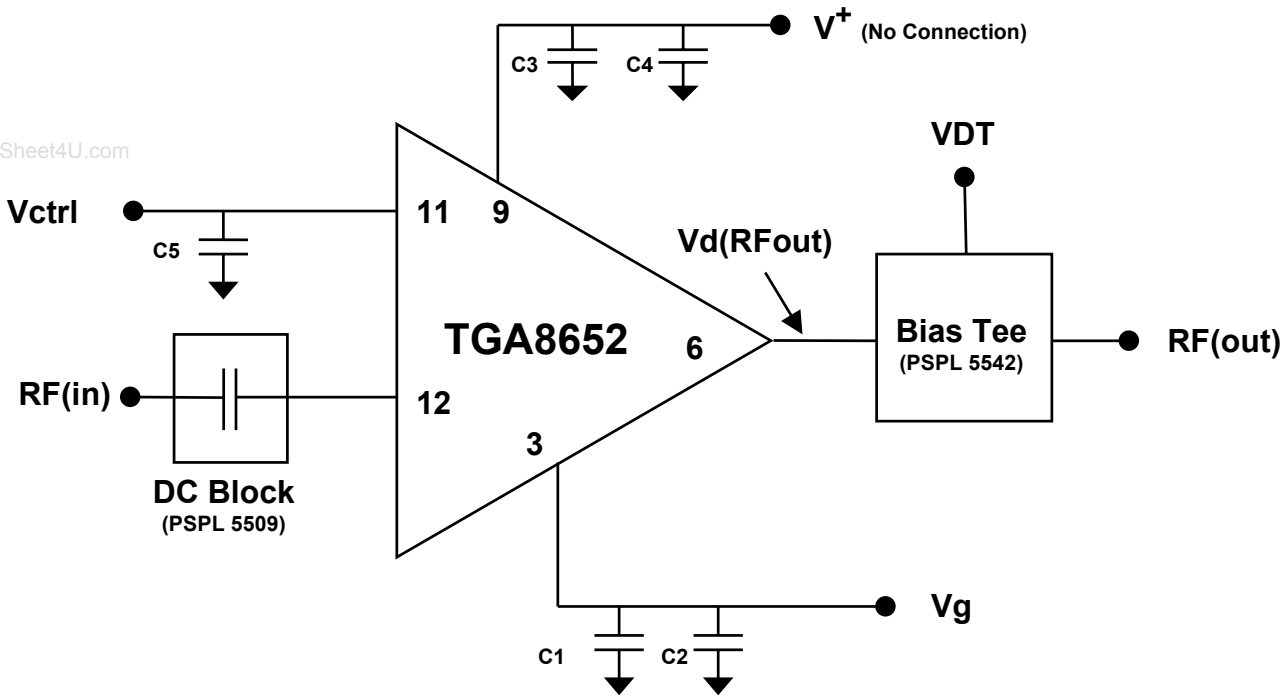
Application Circuit for 4-8V Driver Application



Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C3	1uF Capacitor MLC Ceramic	AVX	0603YC105KAT
C2, C4	10 uF Capacitor MLC Ceramic	AVX	0603YC106KAT
C5	0.01 uF Capacitor MLC	AVX	0603YC103KAT

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

Bias Procedure for 4-8V Driver Application

Bias ON

1. Disable the PPG source
2. Set Vdt = 0V Vctrl = 0V and Vg = 0V
3. Set Vg =-1.5 V
4. Increase Vdt to 8V observing Id.
   - Assure Id = 0mA
5. Set Vctrl = +1.0 V
   - Id should still be 0 mA
6. Make Vg more positive until **Idd = 175mA**.
   - Typical value for **Vg is -0.3 V**
7. Enable the PPG source
   - Vin = 2 Vpp
8. Adjust Vctrl for Vo = 8Vpp
9. Adjust Vg for 50% crossover

Bias OFF

1. Disable the output of the PPG
2. Set Vctrl = 0V
3. Set Vdt = 0V
4. Set Vg = 0V

Notes:

1. Assure Vctrl never exceeds Vd during Bias ON and Bias OFF sequences and during normal operation.

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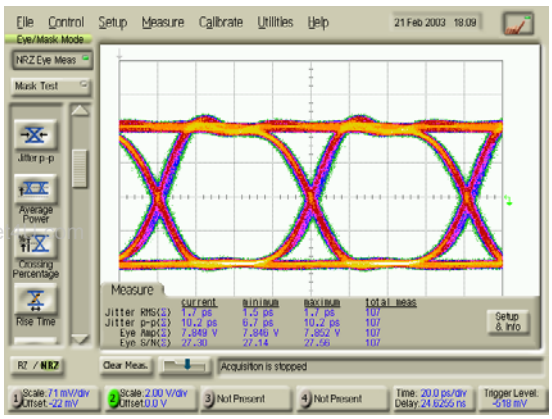
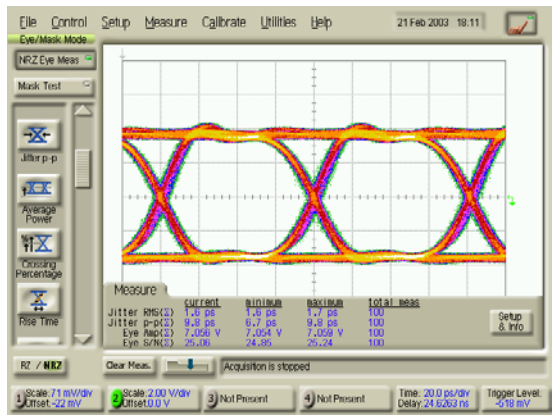
Typical Measured Performance on Demonstration Board
12.5Gb/s 2^31-1, Vd(RFout) = 7 V
CPC = 50%

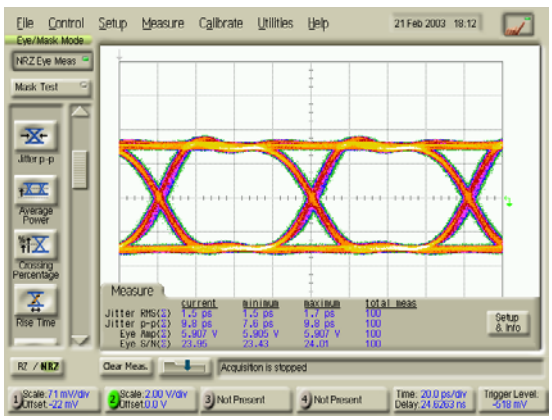
Vo=8 V



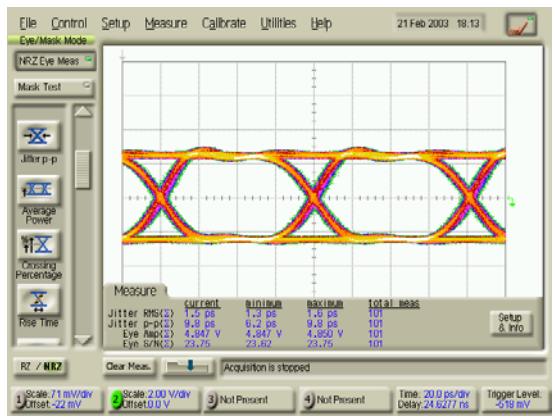
Vo=7 V



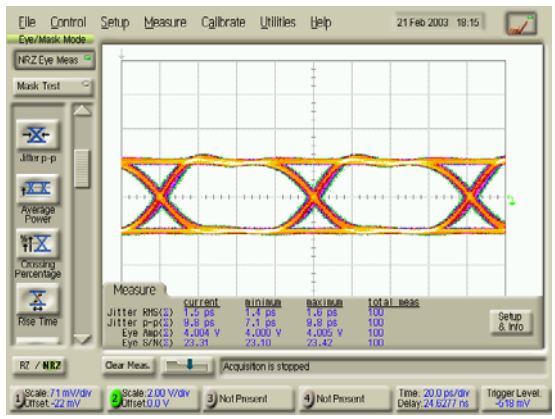
Vo=6 V



Vo=5 V



Vo = 4 V



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Typical Bias Conditions
Vd(RFout) = 7 V

Vo(V)	Vg(V)	Id(mA)	Vctrl
8	-0.23	194	0.87
7	-0.31	173	0.63
6	-0.40	144	0.37
5	-0.48	117	0.16
4	-0.54	97	0.02

Notes:
1. Vd(RFout)=7 V
2. Vin =2 Vpp
3. 50% CPC
4. Actual bias points may be different.

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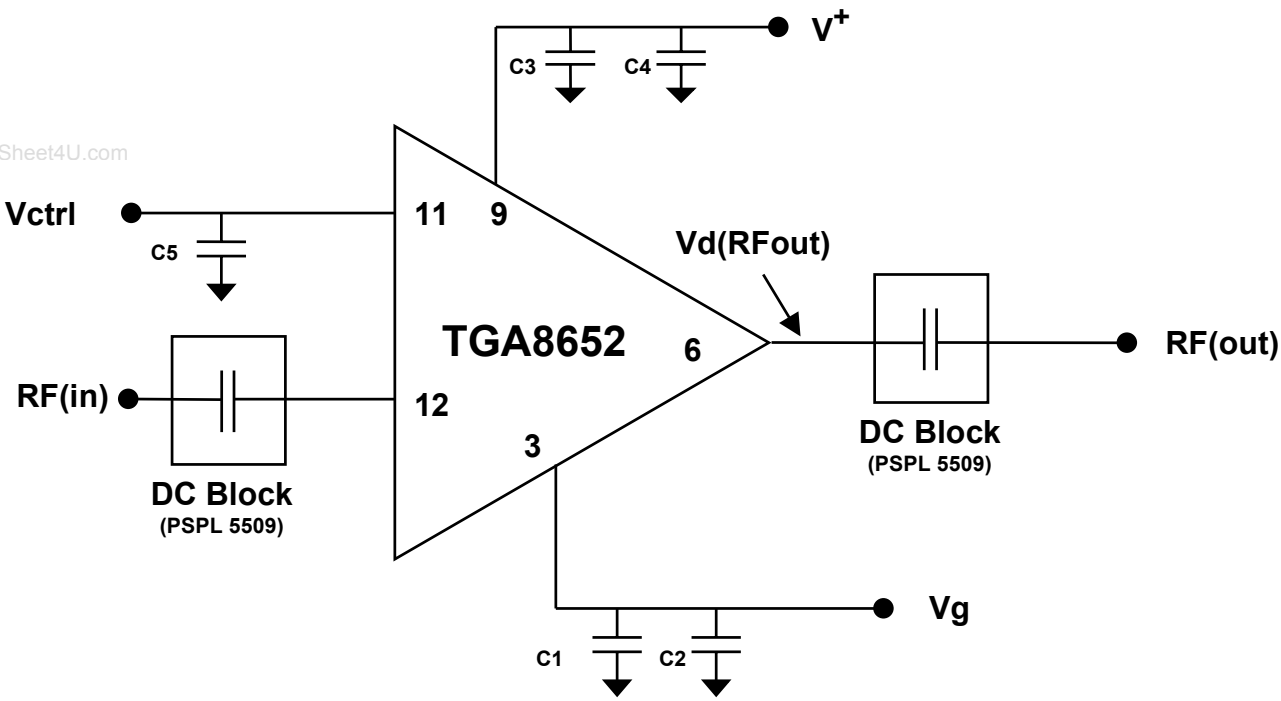
Application Circuit for Pre-Driver and Receive Application



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C5	0.01 uF Capacitor MLC	AVX	0603YC103KAT

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Bias Procedure for Pre-Driver and Receive Application

Bias ON

1. Disable the PPG source
2. Set **V+** = 0 V, Vctrl = 0 V and Vg = 0 V
3. Set Vg = -1.5 V, Set Vctrl = -0.1V
4. Increase **V+** to 8 V observing Id.
   - Assure Id = 0 mA
5. Make Vg more positive until **Idd = 70 mA**.
   - Typical value for **Vg is -0.5 V**
7. Enable the PPG source
   - Set Vin = 500 mV (amplitude)

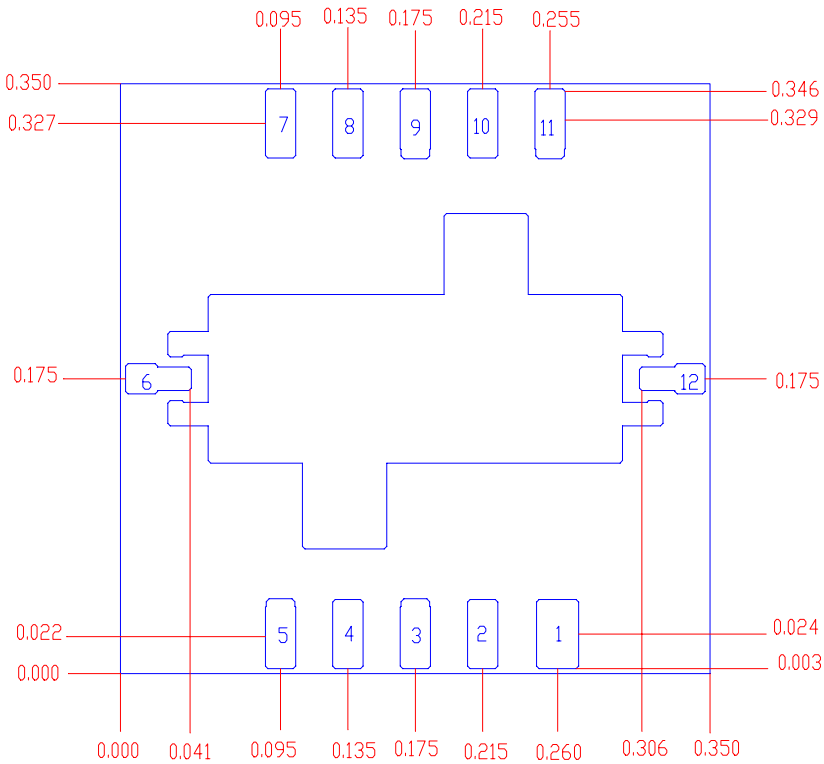
Bias OFF

1. Disable the output of the PPG
2. Set Vctrl = 0V
3. Set Vdt = 0V
4. Set Vg = 0V

Notes:

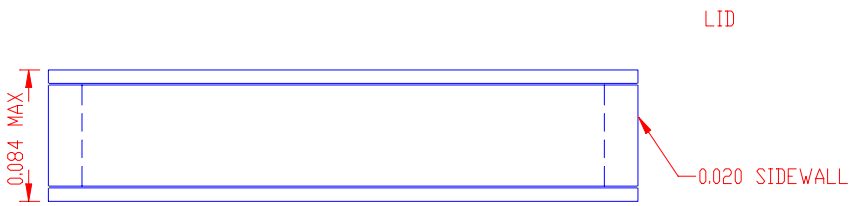
1. Assure Vctrl never exceeds Vd during Bias ON and Bias OFF sequences and during normal operation.

Mechanical Drawing



PIN	FUNCTION	
1	NC	
2	NC	
3	Vg	(0.018 x 0.041)
4	NC	
5	NC	
6	OUT	(0.039 x 0.018)

PIN	FUNCTION	
7	NC	
8	NC	
9	V+	(0.018 x 0.041)
10	NC	
11	Vctrl	(0.018 x 0.041)
12	IN	(0.039 x 0.018)



Notes:

1. Dimensions: Inches. Tolerance: Length and Width: +/-.003 inches.
   Height +/-.006 inches. Adjacent pad to pad spacing: +/- .0002 inches.
   Pad Size: +/- .001 inches.
2. Surface Mount Interface:
   Material: RO4003 (thickness=.008 inches), 1/2oz copper (thickness=.0007 inches)
   Plating Finish: 100-350 microinches nickel underplate, with 5-10 microinches flash gold overplate.

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Assembly of a TGA8652-EPU Surface Mount Package onto a Motherboard

Manual Assembly for Prototypes

1. Clean the motherboard with Acetone and rinse with alcohol and DI water. Allow the motherboard to fully dry.

2. Using a standard SN63 solder paste, such as Kester SN63 R-560, dispense solder paste dots of 5 to 15 mil in diameter to the motherboard as shown in the example motherboard in Figure 1 below. Assure that there is a minimum of 5 mils and a maximum of 10 mils between the edge of each solder paste area and the closest edge of the ground pad.

3. Manually place a TGA8652-EPU on the motherboard with correct orientation and good alignment. The alignment can be determined manually by centering the package on the motherboard. The RF traces (pin 6 and pin 12) are located along the center horizontal axis of the package. DC traces pin 3 and pin 9 are located along the center vertical axis of the package. (Fig. 2)

4. Reflow the assembly on a hot plate with the surface temperature of the plate near 230 °C for 5 to 6 seconds.

5. Let the assembly completely cool down. *This package has little or no tendency to self- align during the reflow.*

6. Clean the assembly with acetone and rinse with alcohol and DI water.

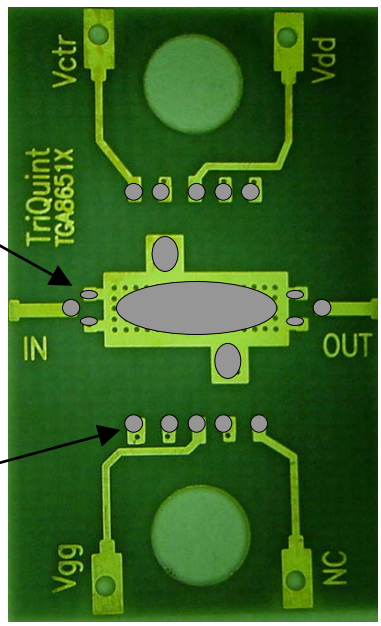

Figure 1: Solder paste dispensing pattern used on the evaluation board motherboard.

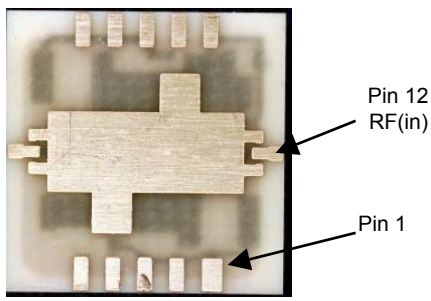

Figure 2: Bottom View
[TGA8652-EPU]

High Volume Assembly of the Package

The TGA8652-EPU is a standard surface mount component compatible with standard high volume assembly processes using standard SN63 solder paste, such as Kester R560. Refer to Kester R560 manufacture data sheet for recommended reflow profile, cleaning, and handling. Dispense solder paste using standard solder printing techniques such as stencil solder printing. Pick-and-place using a standard machine such as MRSI machine. Perform solder reflow using a Sikama Reflow System. Recommended solder stencil and motherboard interface layout are available upon request.

CAUTION: The TGA8652-EPU contains GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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