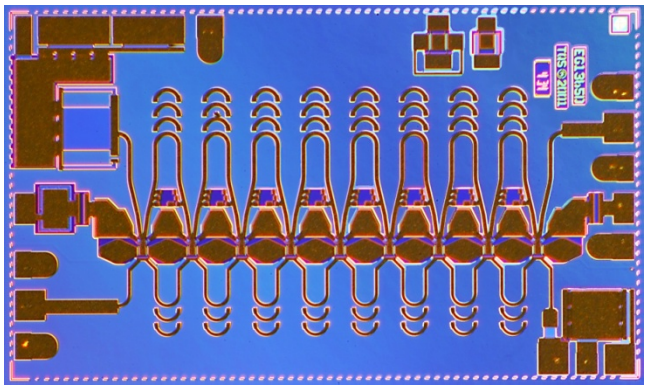
DC – 35 GHz MPA with AGC



Key Features and Performance

- 0.25um pHEMT Technology
- DC - 23GHz Linear BW
- DC - 35GHz Saturated Power BW
- 14dB Small Signal Gain
- 10ps Edge Rates (20/80)
- 7Vpp 43Gb/s NRZ PRBS
- Amplitude and Symmetry Control
- Chip Dimensions 3.3mm x 2.0mm

Primary Applications:

- 43Gb/s NRZ Modulator Driver

Description

The TriQuint TGA4801 is a medium power wideband AGC amplifier that typically provides 10dB saturated midband gain with 6dB AGC range. Typical input and output return loss is >10dB. Typical Noise Figure is 2.5dB at 6GHz. Typical saturated output power is 24dBm at 20GHz. Small signal 3dB BW is 25GHz with saturated power performance to 35GHz. RF ports are DC coupled enabling the user to customize system corner frequencies.

The TGA4801 is an excellent choice for 43Gb/s NRZ applications. The TGA4801 is capable of driving a Lithium Niobate Optical Modulator with electrical Non-Return-to-Zero (NRZ) data.

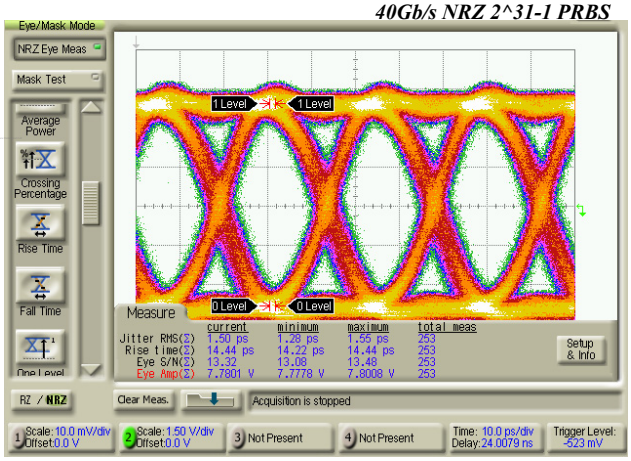
Drain bias may be applied thru the output port for best efficiency or thru the on-chip drain termination. A cascade consisting of three TGA4803's followed by a TGA4801 demonstrated greater than 7V(amplitude) output voltage swing with 350mV at the input when stimulated with 43GB/s 2^31-1 PRBS NRZ data. Output eye patterns shown to the right.

The TGA4801 requires off-chip decoupling and blocking components. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in chip form.

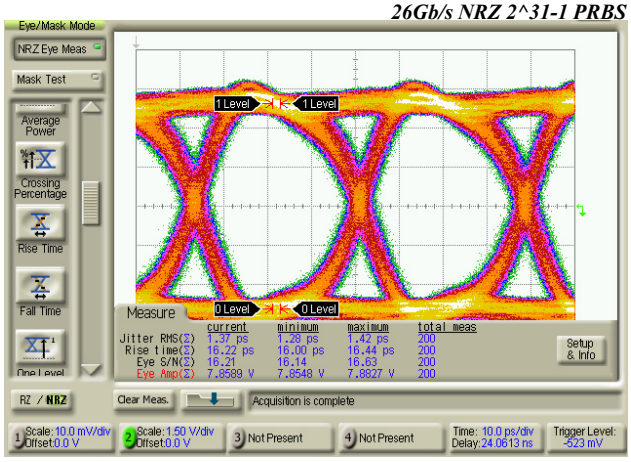
Lead-free and RoHS compliant

Measured Data:

40Gb/s NRZ 2^31-1 PRBS



26Gb/s NRZ 2^31-1 PRBS



Datasheet subject to change without notice

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MAXIMUM RATINGS

SYMBOL	PARAMETER 6/	VALUE	NOTES
	POSITIVE SUPPLY VOLTAGE		
V^+	Biased thru On-chip Drain Termination	12 V	
Vd(fet)	Biased thru the RF Output Port using a Bias Tee	10 V	
	POSITIVE SUPPLY CURRENT		1/
I^+	Biased thru On-chip Drain Termination	220 mA	
Id	Biased thru the RF Output Port using a Bias Tee	220 mA	
P_D	POWER DISSIPATION	1.5 W	2/
	NEGATIVE GATE		
Vg	Voltage	0V to -3V	
Ig	Gate Current	5 mA	
	CONTROL GATE		
Vctl	Voltage	Vd/2 to -3V	3/
Ictl	Gate Current	5 mA	
	RF INPUT		
P_{IN}	Sinusoidal Continuous Wave Power	18dBm	
Vin	43Gb/s PRBS Input Voltage Peak to Peak	4 Vpp	
T_{CH}	OPERATING CHANNEL TEMPERATURE	200 °C	4/ 5/
	MOUNTING TEMPERATURE (30 SECONDS)	320 °C	
T_{STG}	STORAGE TEMPERATURE	-65 to 150 °C	

Notes:

1/ Assure the combination of Vd and Id does not exceed maximum power dissipation rating.
2/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is 3.8E6 hours
3/ Assure Vctl never exceeds Vd during bias up and down sequences. Also, assure Vctl never exceeds 1.5V during normal operation.
4/ These ratings apply to each individual FET.
5/ Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
6/ These ratings represent the maximum operable values for the device.

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RF SPECIFICATIONS
(T_A = 25°C ± 5°C)

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL SIGNAL BW			25		GHz
	SATURATED POWER BW			35		GHz
1/	SMALL-SIGNAL GAIN MAGNITUDE	2.5GHz		14		dB
	AGC RANGE	Midband		6		dB
	NOISE FIGURE	6GHz		2.5		dB
	SATURATED OUTPUT VOLTAGE (EYE AMPLITUDE)	43Gb/s with Vin=2.5Vpp		7.5		V
1/	SATURATED OUTPUT POWER	DC-20GHz		24		dBm
1/	INPUT RETURN LOSS MAGNITUDE	DC-20GHz		-12		dB
1/	OUTPUT RETURN LOSS MAGNITUDE	DC-20GHz		-12		dB
	GROUP DELAY	DC-20GHz		+/- 20		ps
	RISE TIME	20/80%		10		ps

Notes:
1/ Verified at RF on-wafer probe.

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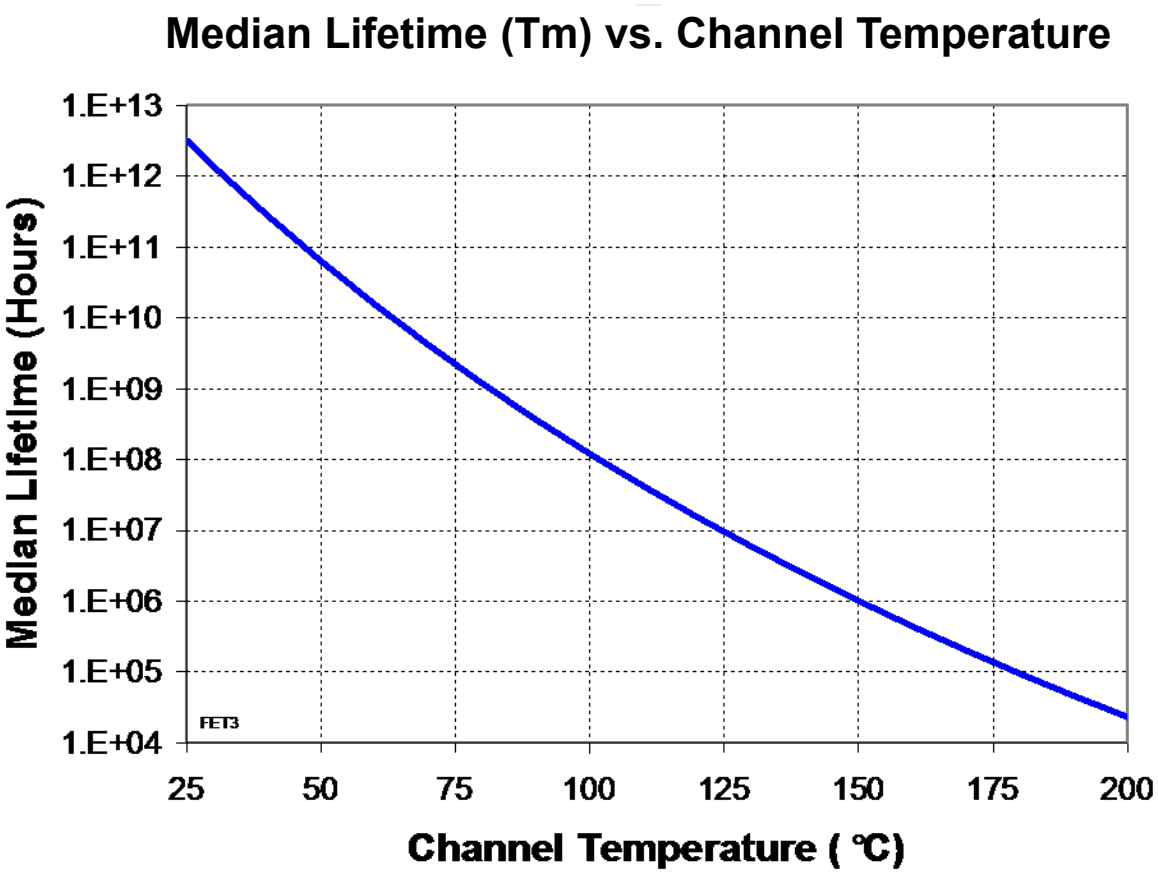
THERMAL INFORMATION

Parameter	Test Condition	T_{CH} (°C)	θ_{JC} (°C/W)	Tm (HRS)
θ_{JC} Thermal Resistance (channel to backside of carrier)	Vd(fet) = 7V, V_{ctrl} = 1.5 V, I_D = 170mA	120	43	1.5E+7

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.



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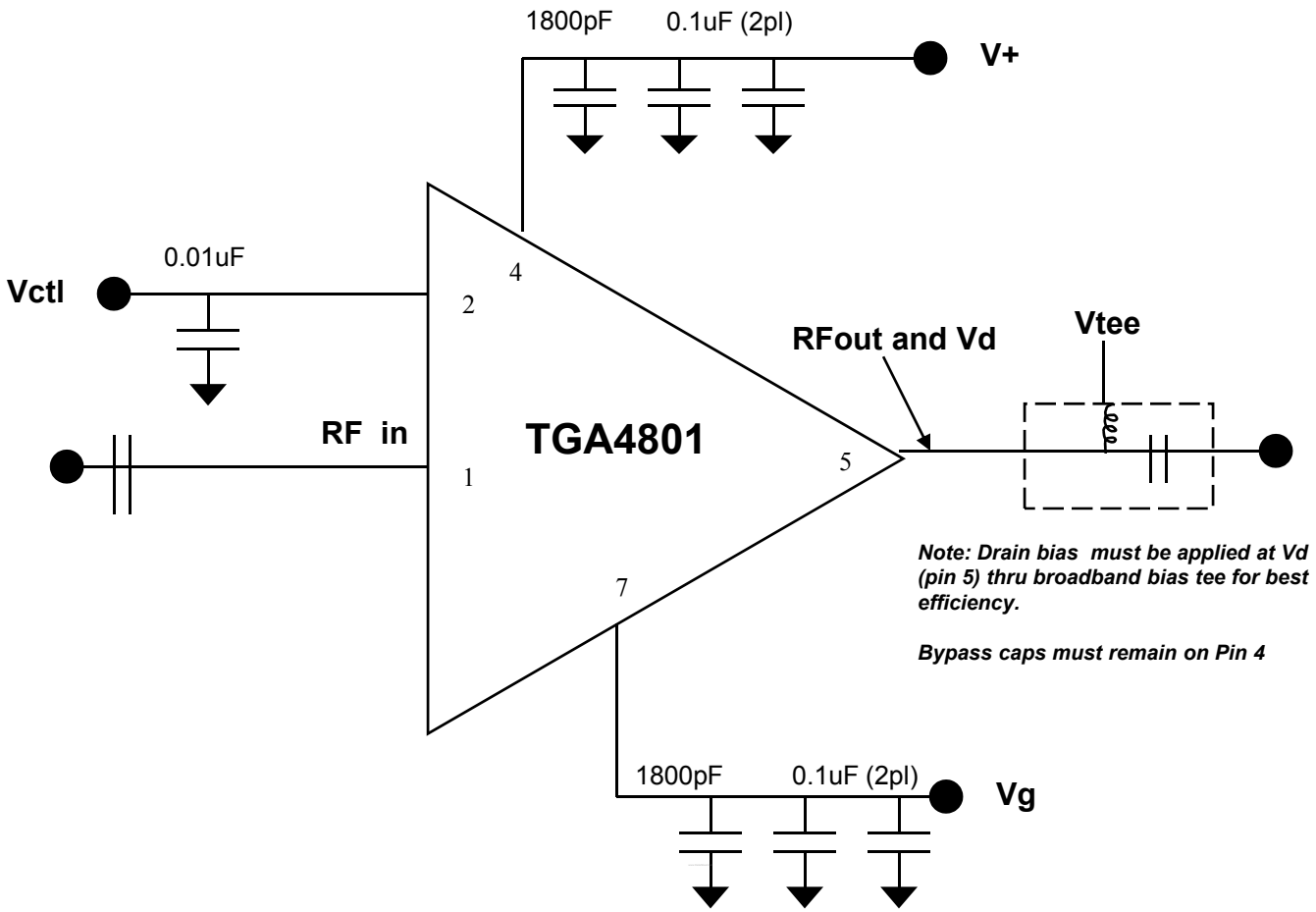
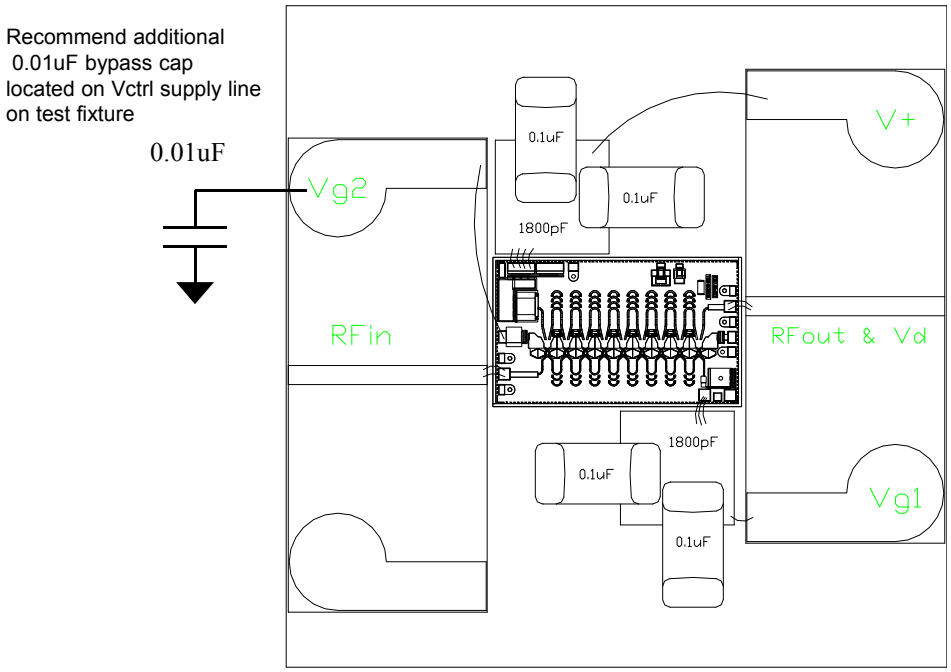


Bias Procedure:

1. Make sure no RF power is applied to the device before continuing.
2. Pinch off device by setting Vg to –1.5V.
3. Raise Vd to 6.5V while monitoring drain current. Current should be zero.
4. Raise Vctl to 1V (no greater than 2.5V).
5. Adjust Vg more positive until drain current reaches 160mA.
6. Apply Vin=2.5Vpp 40Gb/s NRZ 2^31-1 PRBS.
7. Adjust Vctl for amplitude and Vg for symmetry.

Note:

1. Assure Vctl never exceeds Vd during bias up and down sequences. Also, assure Vctl never exceeds 2.5V during normal operation.



Reflow process assembly notes:

- AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
- alloy station or conveyor furnace with reducing atmosphere
- no fluxes should be utilized
- coefficient of thermal expansion matching is critical for long-term reliability
- storage in dry nitrogen atmosphere

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200°C

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.