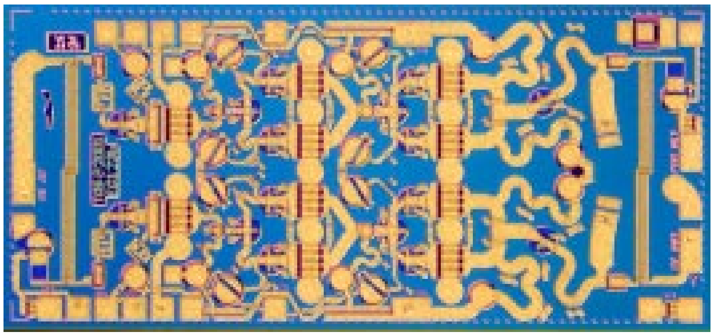
K Band High Power Amplifier

TGA4502-SCC



Key Features

- 17-27 GHz Application Frequency Range
- 22 dB Nominal Gain
- 29 dBm Nominal P1dB
- 37dBm Nominal OTOI
- 15 dB Nominal Return Loss
- 0.25 um pHEMT 2MI Technology
- Bias 7V @ 760 mA
- Chip Dimensions 1.52 x 3.29 x .1mm

Primary Applications

- K Band Sat-Com
- Point-to-Point Radio
- Point-to-Multipoint Communications

Product Description

The TriQuint TGA4502-SCC is a compact High Power Amplifier MMIC for K-band applications. The part is designed using TriQuint's proven standard 0.25 um gate power pHEMT production process.

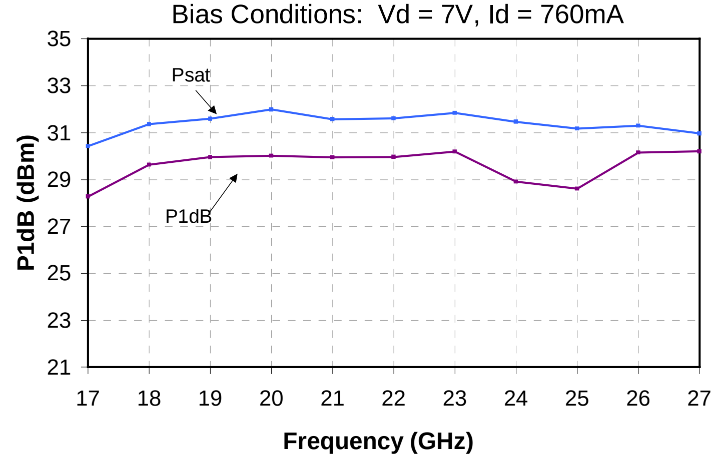
The TGA4502-SCC provides a nominal 29 dBm of output power at 1 dB gain compression from 17-27 GHz with a small signal gain of 22 dB.

The part is ideally suited for low cost emerging markets such as K-band Satellite Communications, Point-to-Point Radio, and Point-to-Multi Point Communications.

The TGA4502-SCC is 100% DC and RF tested on-wafer to ensure performance compliance.

Fixtured Measured Performance

Bias Conditions: Vd = 7V, Id = 760mA



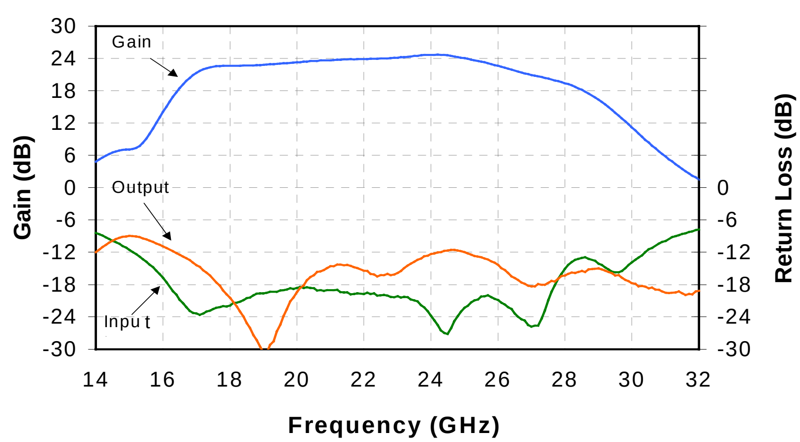


TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V^+	Positive Supply Voltage	8 V	2/
V^-	Negative Supply Voltage Range	-5V TO 0V	
I^+	Positive Supply Current	880 mA	2/
$\lvert I_G \rvert$	Gate Supply Current	28 mA	
P_{IN}	Input Continuous Wave Power	26 dBm	2/
P_D	Power Dissipation	5.3 W	2/, 3/
T_{CH}	Operating Channel Temperature	150 °C	4/, 5/
T_M	Mounting Temperature (30 Seconds)	320 °C	
T_{STG}	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Current is defined under no RF drive conditions. Under RF drive, the supply current may rise to 1100 mA without damage. Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ When operated at this power dissipation with a base plate temperature of 70 °C, the median life is 1 E+6 hours.

4/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

5/ These ratings apply to each individual FET.

TABLE II
DC PROBE TEST
(T_A = 25 °C, Nominal)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$I_{dss, Q1}$	Saturated Drain Current	60	282	mA
$G_{m, Q1}$	Transconductance	132	318	mS
$V_{p, Q1,2, 3\text{-}6, 7\text{-}10}$	Pinch-off Voltage	-1.5	-0.5	V
$V_{BVGD, Q1\text{-}10}$	Breakdown Voltage Gate-Drain	-30	-13	V
$V_{BVGS, Q1,2,3\text{-}6,7\text{-}10}$	Breakdown Voltage Gate-Source	-30	-13	V

Note: Q1 & Q2 are 600 um FETs. Q3-6 & Q7-10 are 2400 um FETs. Q1-10 is a 6000 um FET.

TABLE III
RF CHARACTERIZATION TABLE
(T_A = 25 °C, Nominal)
Vd = 7V, Id = 760 mA

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNITS
			MINIMUM	TYPICAL	MAXIMUM	
Gain	Small Signal Gain	F = 17 – 18 GHz F = 17.5, 18 GHz F = 20, 22, 24 GHz F = 26.5 GHz F = 27 GHz	-- 17 18 17 --	22 -- 23 -- 20	-- -- -- -- --	dB
IRL	Input Return Loss	F = 17 – 27 GHz F = 17.5, 18, 20, 22, 24 GHz F = 26.5 GHz	-- -- --	20 -- --	-- 12 10	dB
ORL	Output Return Loss	F = 17 – 27 GHz F = 17.5, 18, 20, 22, 24 GHz F = 26.5 GHz	-- -- --	15 -- --	-- 12 10	dB
P_{1dB}	Output Power @ 1dB Gain Compression	F = 17 – 27 GHz F = 18, 26.5 GHz	-- 27	30	-- --	dBm
OTOI *	Output Third Order Intercept	F = 17 – 27 GHz F = 18, 26 GHz	-- 34.5	37 --	-- --	dBm

* Pin/tone = -7dBm, Separation = 0.010 GHz

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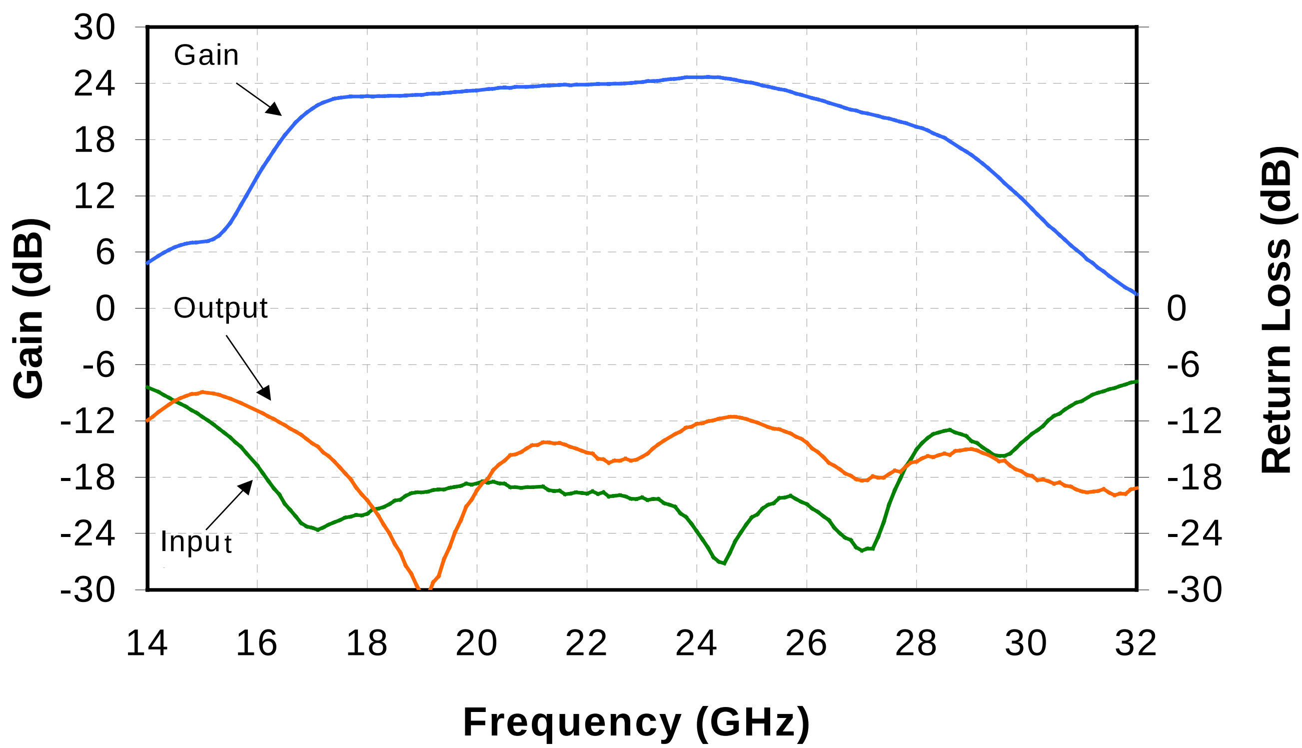
TABLE IV
THERMAL INFORMATION

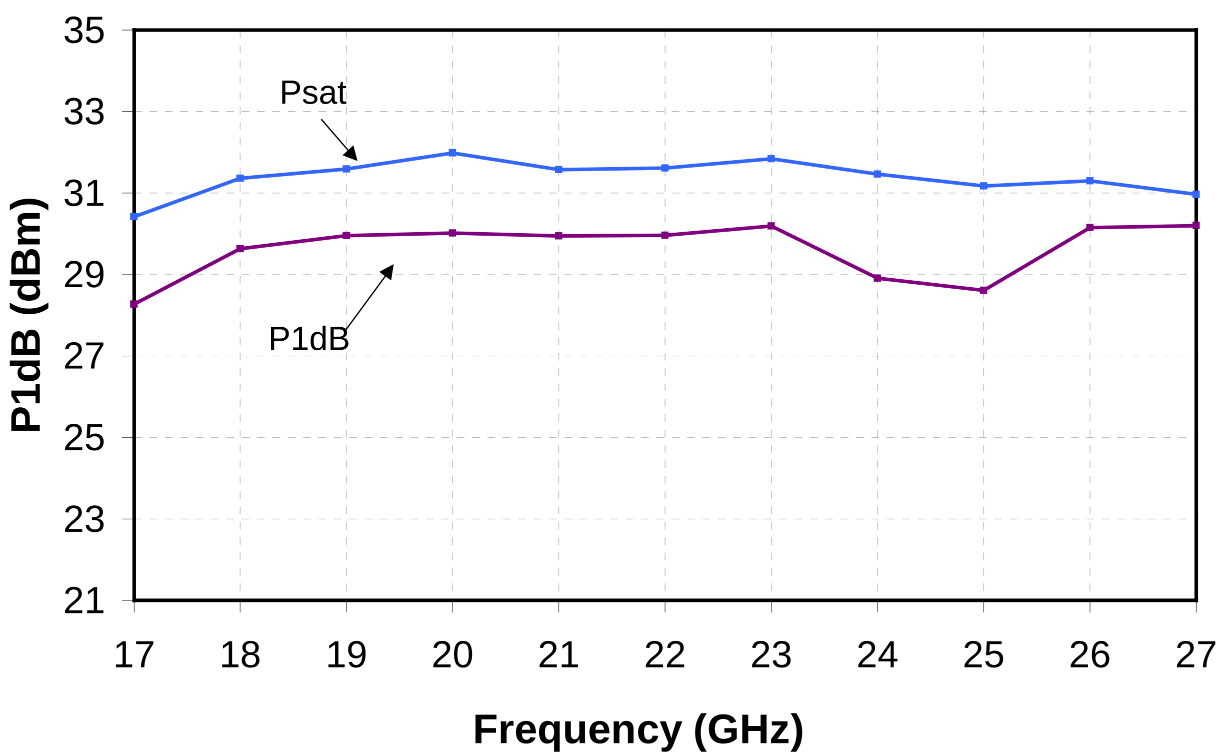
Parameter	Test Conditions	T_{CH} (°C)	$R_{\theta JC}$ (°C/W)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd = 7 V Id = 760 mA Pdiss = 5.3 W	150	15.1	1 E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

Measured Fixtured Data

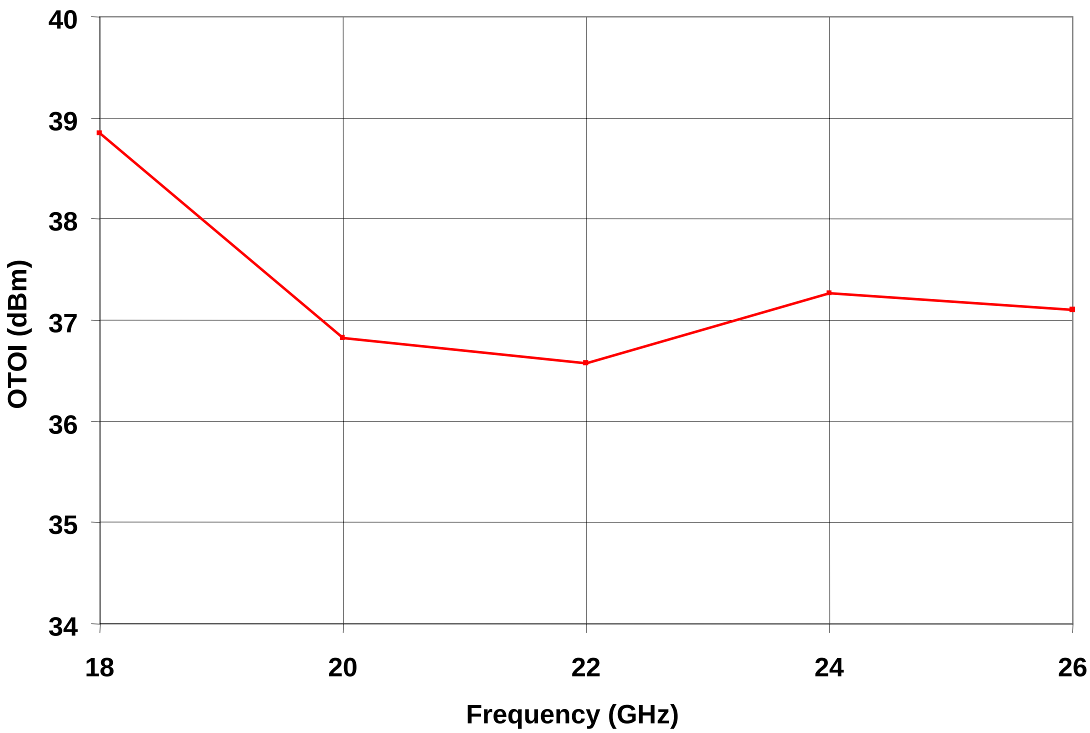
Bias Conditions: Vd = 7V, Id = 760mA

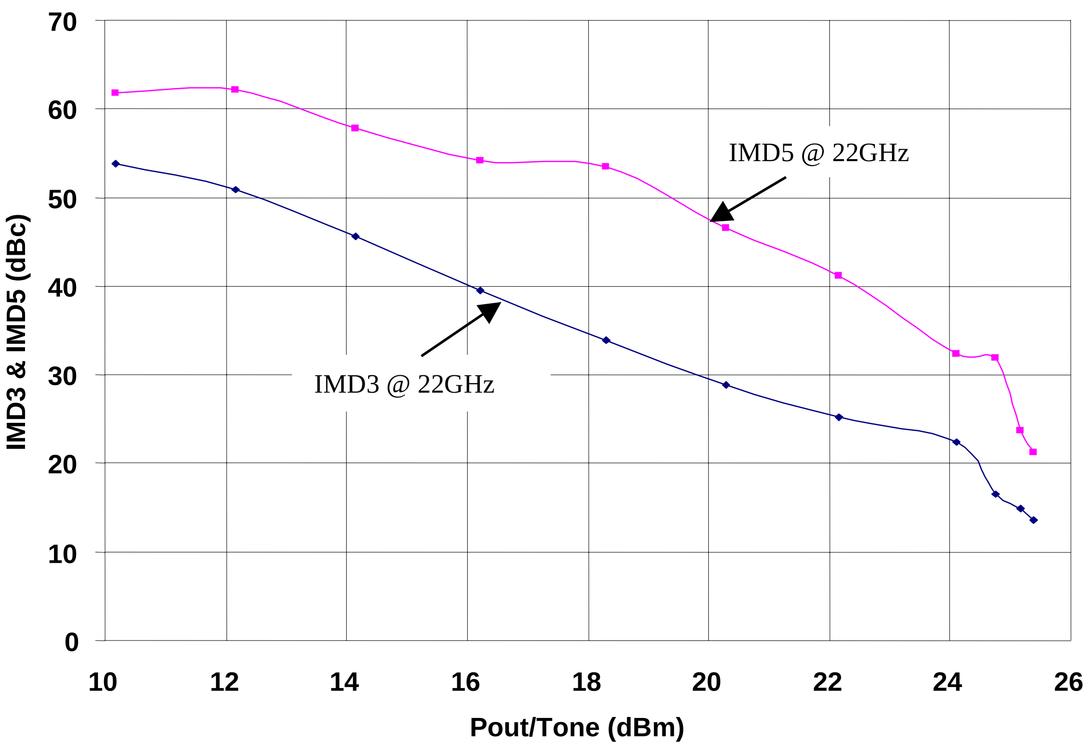




Measured Fixtured Data

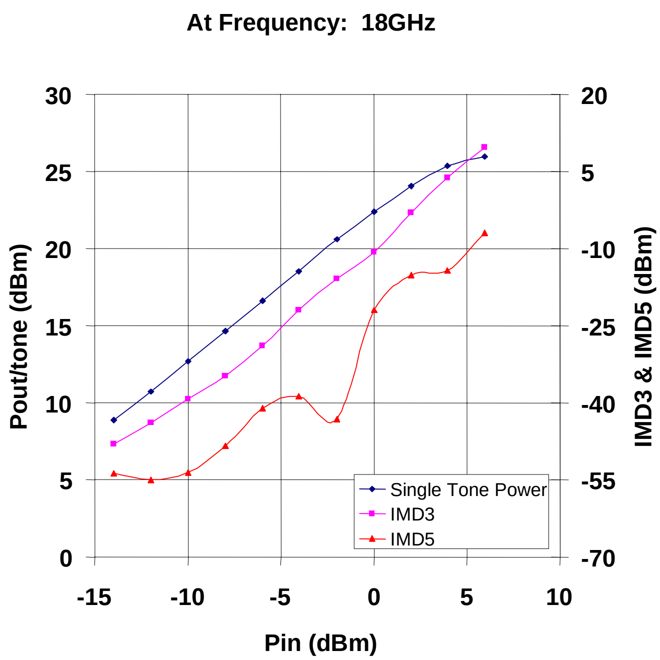
Bias Conditions: Vd = 7V, Id = 760mA

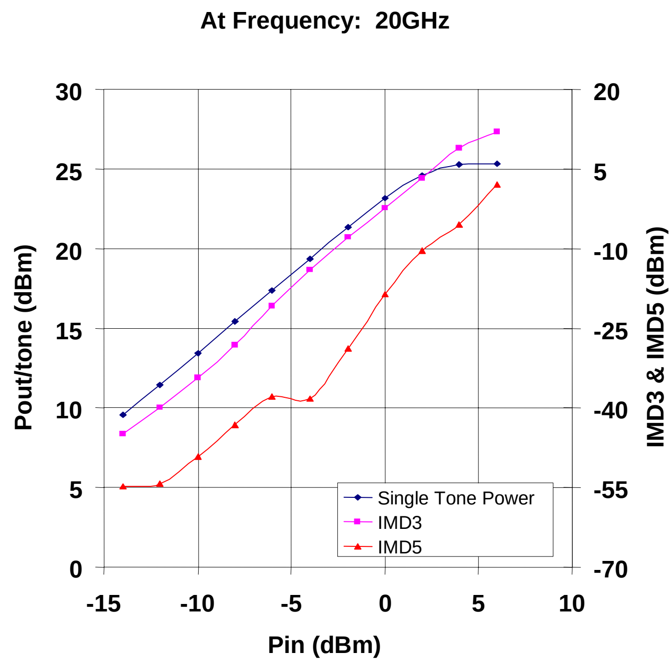


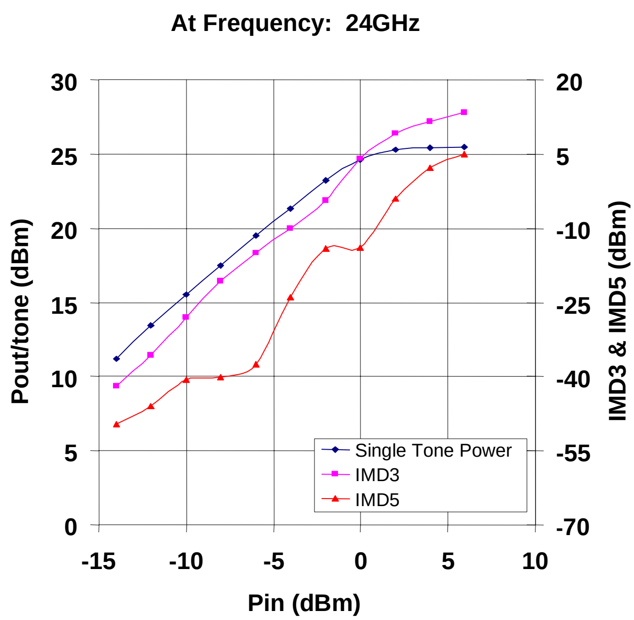


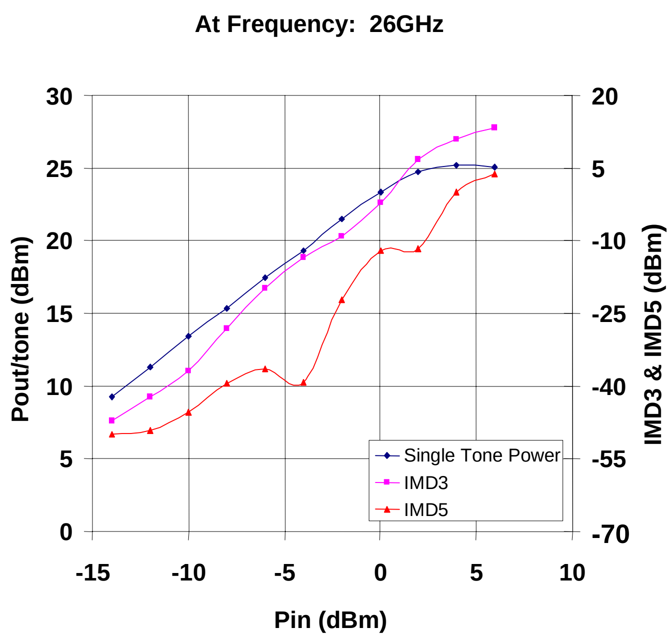
Measured Fixtured Data

Bias Conditions: Vd = 7V, Id = 760mA

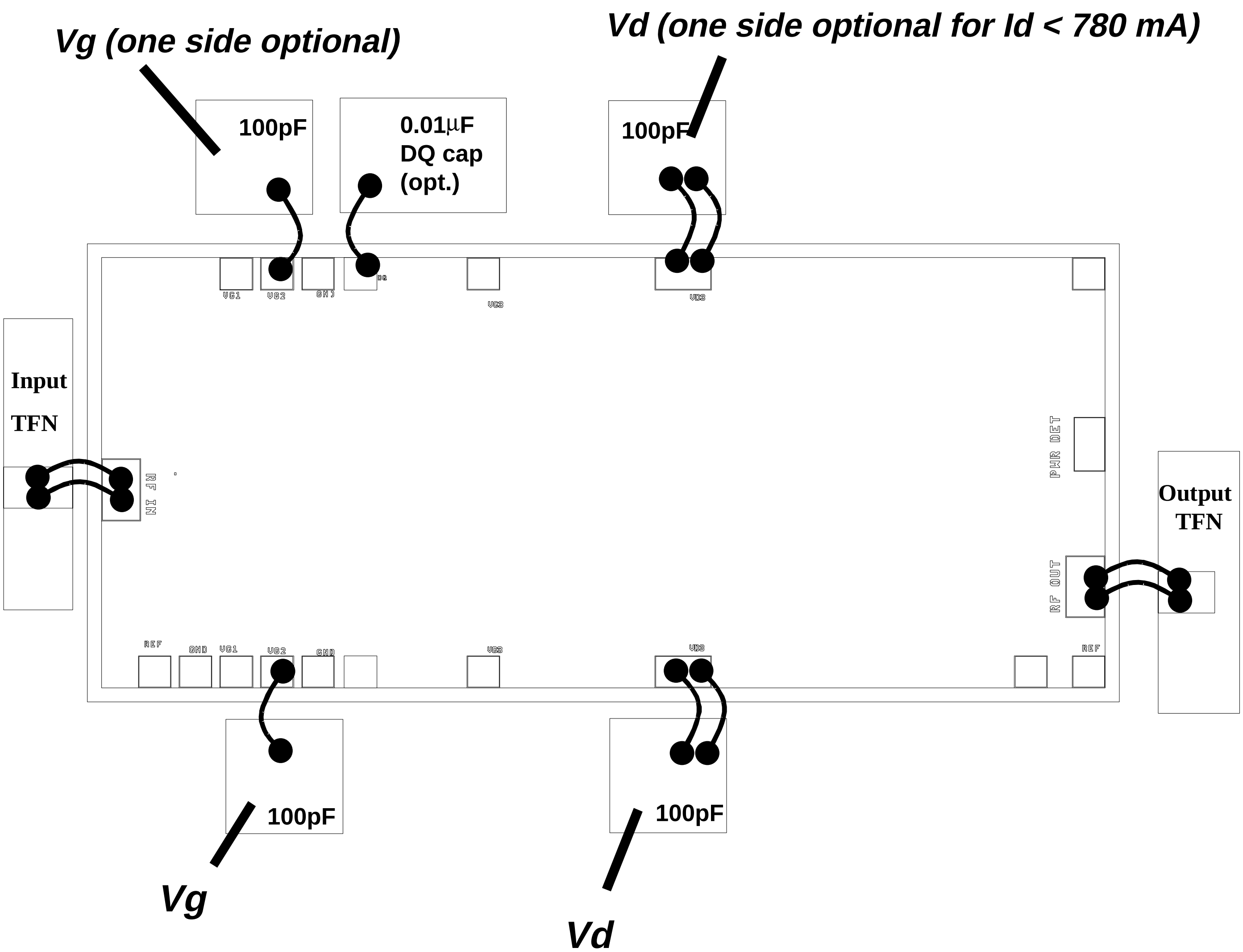








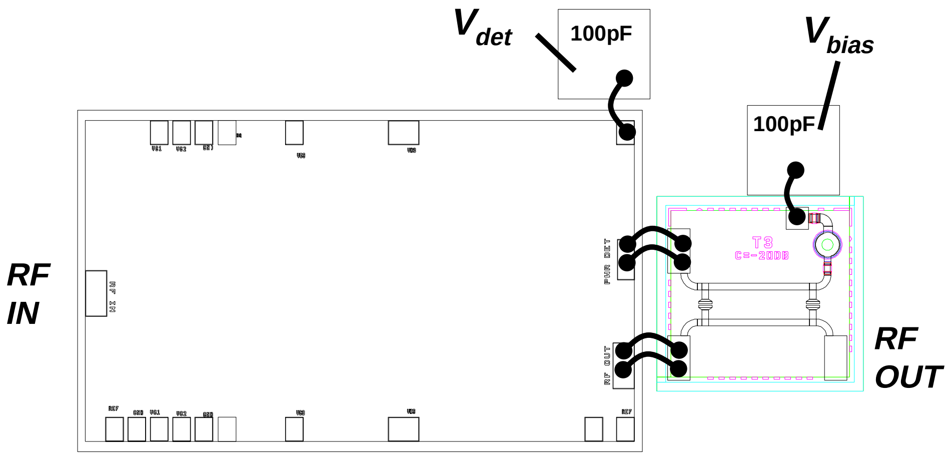
Recommended Assembly Diagram



Notes:
1. Connection to power det, ref diode not shown.
2. 0.1µF cap on gate, drain lines not shown but required.
3. For high power operation, gate voltage is recommended from both sides.
4. Drain voltage is required from both sides for Id > 780mA.

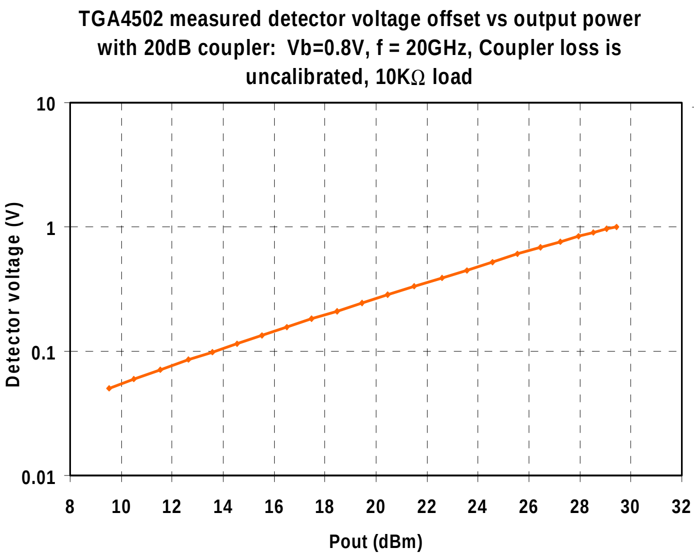
GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

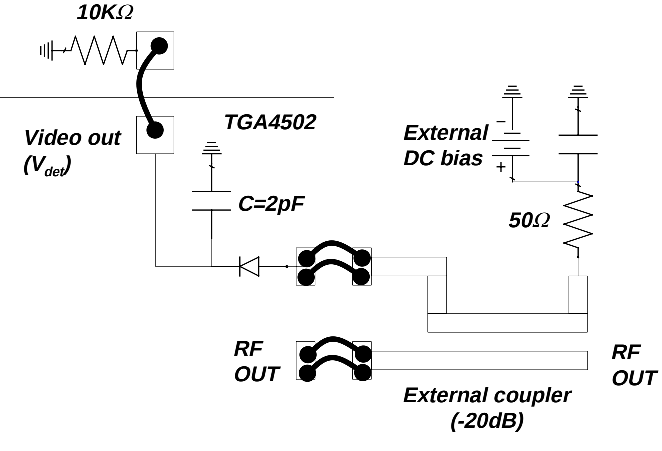
TGA4502 built-in power detector



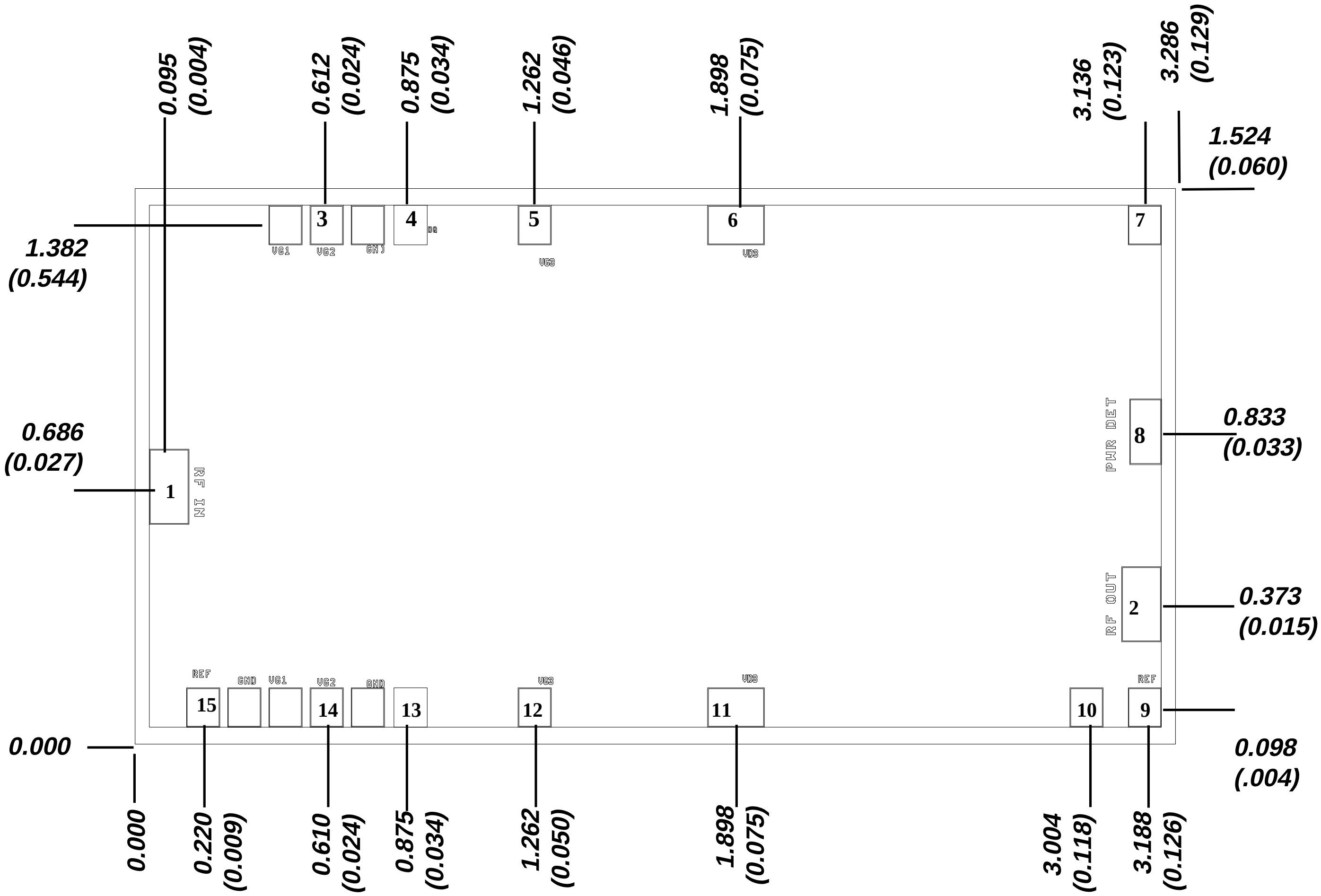
TGA4502 with external test coupler
(amplifier bias connections not shown)

On-chip diode functions as envelope detector
External coupler and DC bias required





Mechanical Drawing



Units: Millimeters (inches)
Thickness: 0.100 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance +/- 0.051 (0.002)
GND IS BACKSIDE OF MMIC

Bond pad #1	(RF Input)	0.200 x 0.100 (0.008 x 0.004)
Bond pad #2	(RF Output)	0.200 x 0.100 (0.008 x 0.004)
Bond pad #3	VG2	0.100 x 0.100 (0.004 x 0.004)
Bond pad #4	DQ	0.100 x 0.100 (0.004 x 0.004)
Bond pad #5	VG3	0.100 x 0.100 (0.004 x 0.004)
Bond pad #6	VD3	0.180 x 0.100 (0.007 x 0.004)
Bond pad #7	DET OUT	0.100 x 0.100 (0.004 x 0.004)
Bond pad #8	PWR DET	0.175 x 0.100 (0.007 x 0.004)
Bond pad #9	REF2	0.100 x 0.100 (0.004 x 0.004)
Bond pad #10	REF1	0.100 x 0.100 (0.004 x 0.004)
Bond pad #11	VD3	0.180 x 0.100 (0.007 x 0.004)
Bond pad #12	VG3	0.100 x 0.100 (0.004 x 0.004)
Bond pad #13	DQ	0.100 x 0.100 (0.004 x 0.004)
Bond pad #14	VG2	0.100 x 0.100 (0.004 x 0.004)
Bond pad #15	REF3	0.100 x 0.100 (0.004 x 0.004)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C (for 30 sec max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

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Die are shipped in H20-074149 waffle packs.