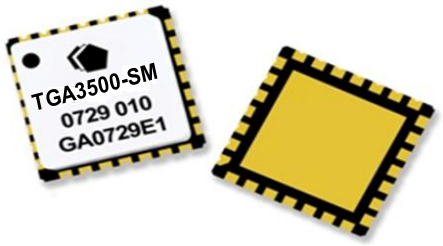
TGA3500-SM

2-12 GHz Driver Amplifier

Applications

- General Purpose

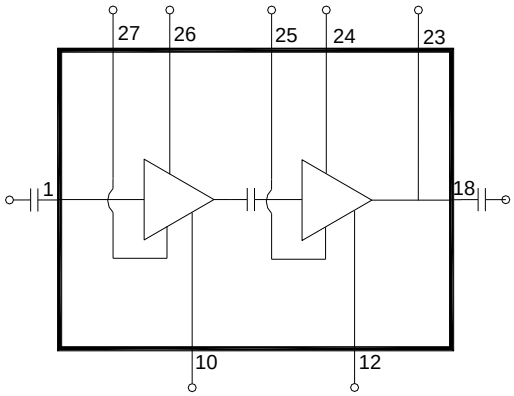


QFN 8x8mm 28L

Product Features

- Frequency Range: 2 – 12 GHz
- Power: 23 dBm P_{SAT}
- Gain: 34 dB
- Output TOI: 29 dBm
- Noise Figure: 3 dB
- Bias: V_D = 5 V, I_D = 200 mA, V_{G1} = -0.7 V, V_{G2} = -0.6 V Typical
- VSWR: 5 to 6
- Package Dimensions: 8.0 x 8.0 x 2.1 mm

Functional Block Diagram



General Description

TriQuint's TGA3500-SM is a variable gain amplifier capable of supporting a variety of applications. The TGA3500-SM operates from 2 to 12 GHz and is designed using proven TriQuint's 0.15um pHEMT production process.

The TGA3500-SM typically provides 23 dBm of linear power with 34 dB of small signal gain and 29 dBm of output TOI. The Noise Figure is typically 3 dB.

The TGA3500-SM is available in a low-cost, surface mount 28 lead 8x8 AIN QFN package base with an Air cavity ceramic Lid. The TGA3500-SM is ideally suited to support both commercial and defense related applications.

Lead-free and RoHS compliant.

Evaluation Boards are available upon request.

Pad Configuration

Pad No.	Symbol
1-4, 6-9, 11,13-17, 19-22, 28	No Connection
5	RF IN
10	V_{G1}
12	V_{G2}
18	RF OUT
23	V_{D2T}
24	V_{D2}
25	V_{CTRL2}
26	V_{D1}
27	V_{CTRL1}

Ordering Information

Part	ECCN	Description
TGA3500-SM	EAR99	2-12 GHz Gain Driver Amp

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_{D1}, V_{D2})	6 V
Drain to Gate Voltage (V_{D1}-V_{G1}, V_{D2}-V_{G2})	11 V
Drain to Control Voltage (V_{D1}-V_{CTRL1}, V_{D2}-V_{CTRL2})	7 V
Gate Voltage Range (V_{G1}, V_{G2})	-5 to 0 V
Control Voltage (V_{CTRL1}, V_{CTRL2})	(V_D-7) to 5 V
Drain Current (I_{D1}, I_{D2})	192 mA, 192 mA
Gate Current (I_{G1}, I_{G2})	-3.6 to 101 mA
Control Current (I_{CTRL1}, I_{CTRL2})	-2.7 to 76 mA
Power Dissipation (P_{DISS})	3.8 W
RF Input Power, CW, 50 Ω, T = 25 °C (P_{IN})	+25 dBm
Channel Temperature (T_{CH})	200 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	5 V
Drain Current (I_{D1})	40 mA
Total Drain Current (I_{D2T})	200 mA
Gate Voltage (V_{G1})	-0.7 V (Typ.)
Gate Voltage (V_{G2})	-0.6 V (Typ.)
Control Voltage (V_{CTRL1})	-0.6 V
Control Voltage (V_{CTRL2})	+0.2 V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, V_D = 5 V, I_{D2T} = 200 mA (I_{D1} = 40 mA, I_{D2} = 160 mA), V_{CTRL1} = -0.6 V, V_{CTRL2} = +0.2 V, V_{G1} = -0.7 V, V_{G2} = -0.6 V

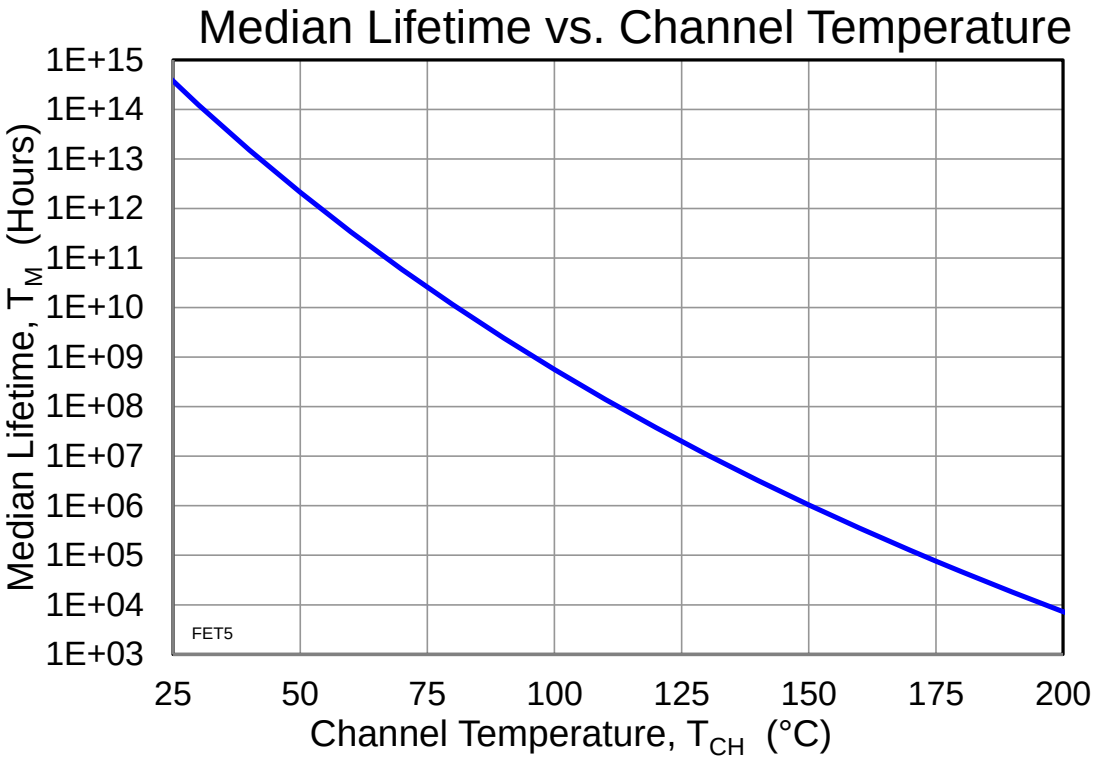
Parameter	Min	Typical	Max	Units
Operational Frequency Range	2		12	GHz
Gain		34		dB
Input Return Loss		15		dB
Output Return Loss		14		dB
Output Power at Saturation		23		dBm
Output TOI		29		dBm
Noise Figure		3		dB
Gain Temperature Coefficient		-0.016		dB/°C
Power Temperature Coefficient		-0.002		dB/°C

Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC}	Tbaseplate = 85 °C	33	ºC/W
Channel Temperature, T_{CH} (Without RF Drive)	Tbaseplate = 85 °C, V_D = 5 V, I_{DQ} = 200 mA, P_{DISS} = 1 W	111	°C
Median Lifetime, T_M (Without RF Drive)		1.2 x 10^8	Hrs
Channel Temperature, T_{CH} (Under RF Drive)	Tbaseplate = 85 °C, V_D = 5 V, P_{DISS} = 1 W, I_{DD} = 227 mA, P_{OUT} = 22 dBm	117	°C
Median Lifetime, T_M (Under RF Drive)		5.5 x 10^7	Hrs

Notes: Thermal resistance measured to back of package.

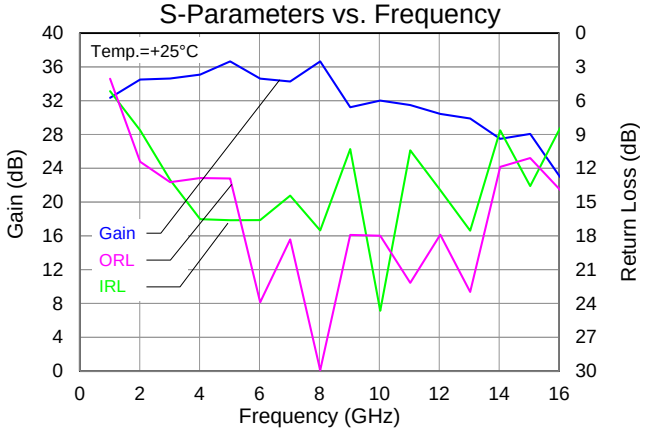
Median Lifetime



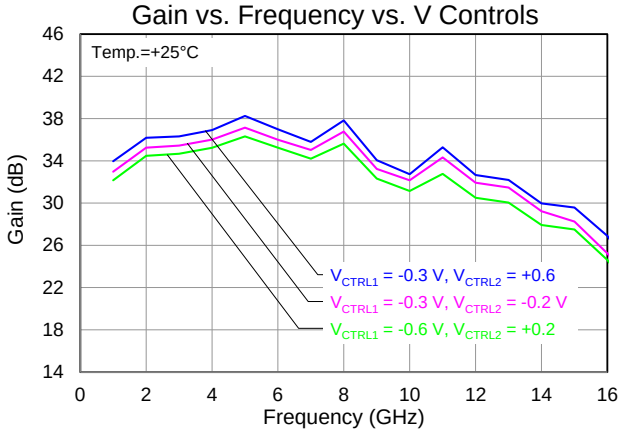
Typical Performance

Conditions unless otherwise specified: V_{D1} = V_{D2T} = 5 V, I_{D1} = 40 mA, I_{D2T} = 200 mA, V_{G1} = -0.7 V, V_{G2} = -0.6 V Typ., V_{CTRL1} = -0.6 V, V_{CTRL2} = +0.2 V

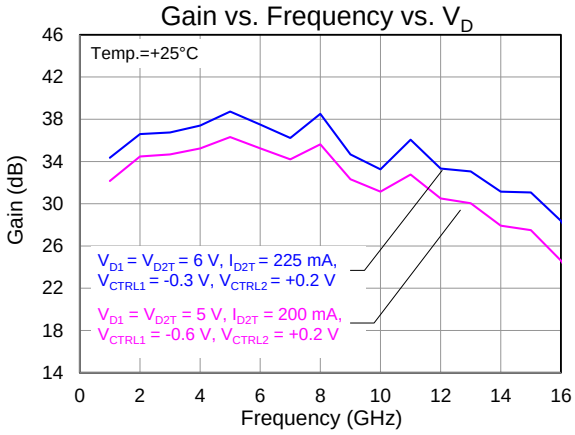
S-Parameters vs. Frequency



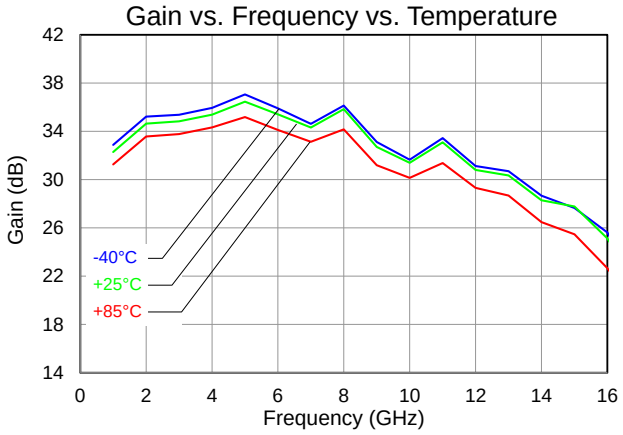
Gain vs. Frequency vs. V Controls



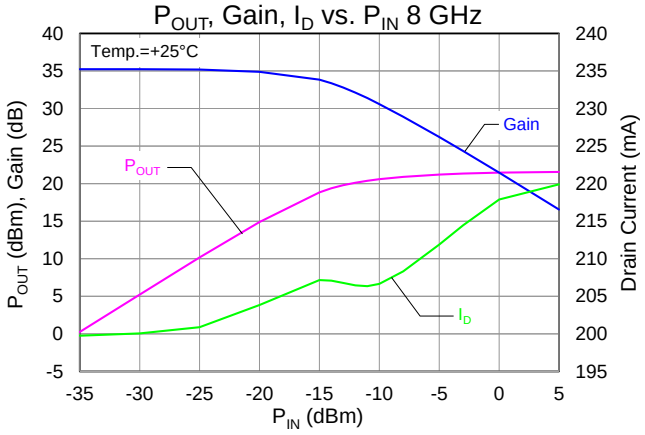
Gain vs. Frequency vs. V_D



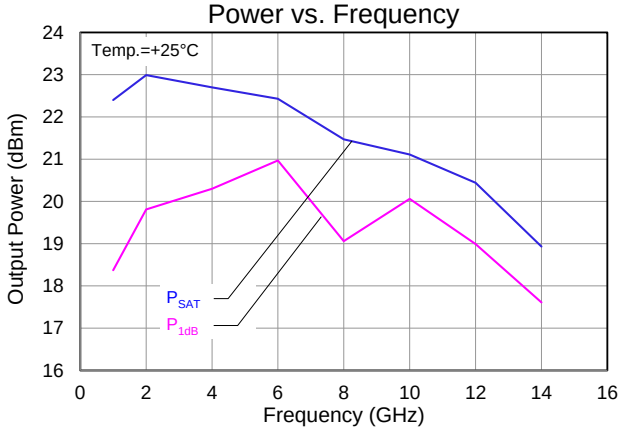
Gain vs. Frequency vs. Temperature



P_{OUT}, Gain, I_D vs. P_{IN} 8 GHz



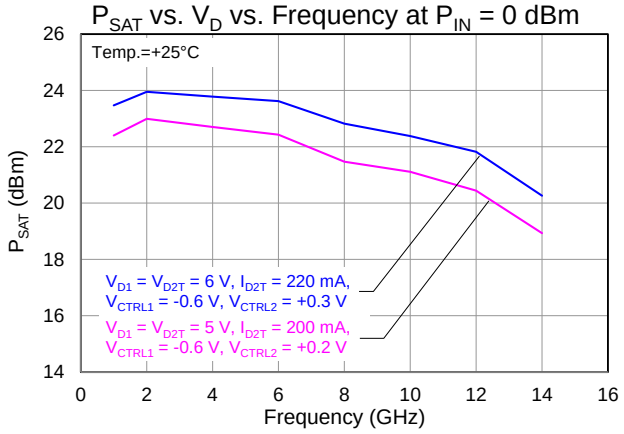
Power vs. Frequency



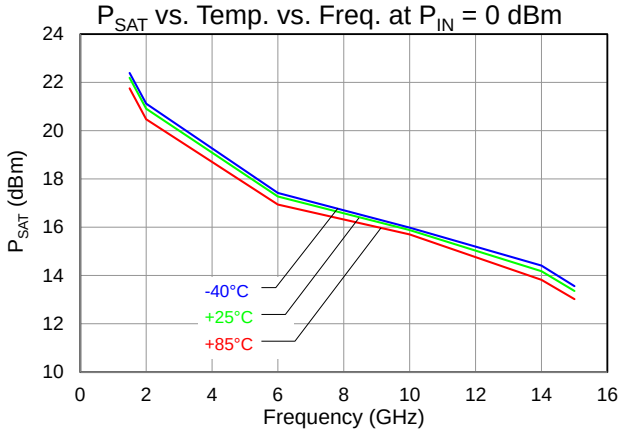
Typical Performance

Conditions unless otherwise specified: V_{D1} = V_{D2T} = 5 V, I_{D1} = 40 mA, I_{D2T} = 200 mA, V_{G1} = -0.7 V, V_{G2} = -0.6 V Typ., V_{CTRL1} = -0.6 V, V_{CTRL2} = +0.2 V

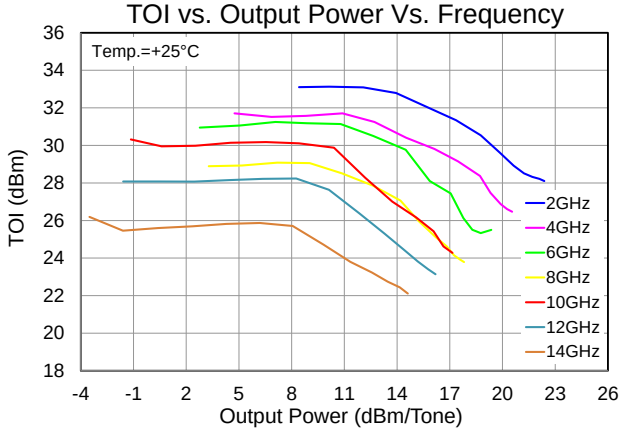
P_{SAT} vs. V_D vs. Frequency at P_{IN} = 0 dBm



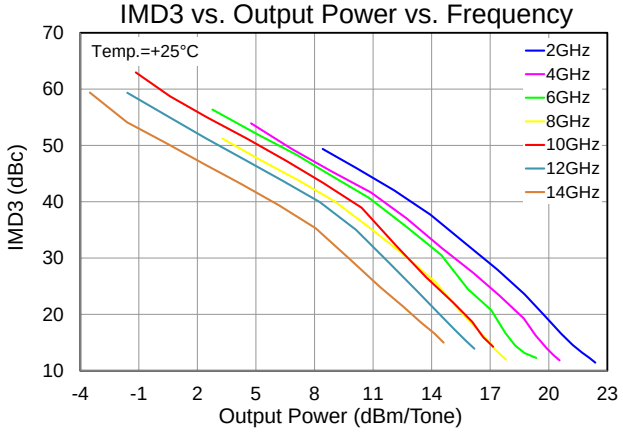
P_{SAT} vs. Temp. vs. Freq. at P_{IN} = 0 dBm



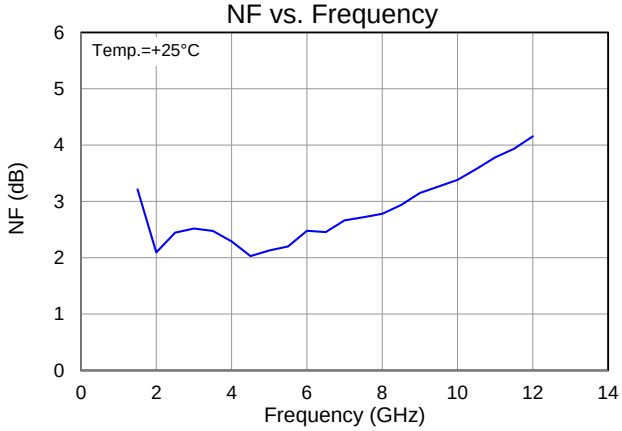
TOI vs. Output Power Vs. Frequency



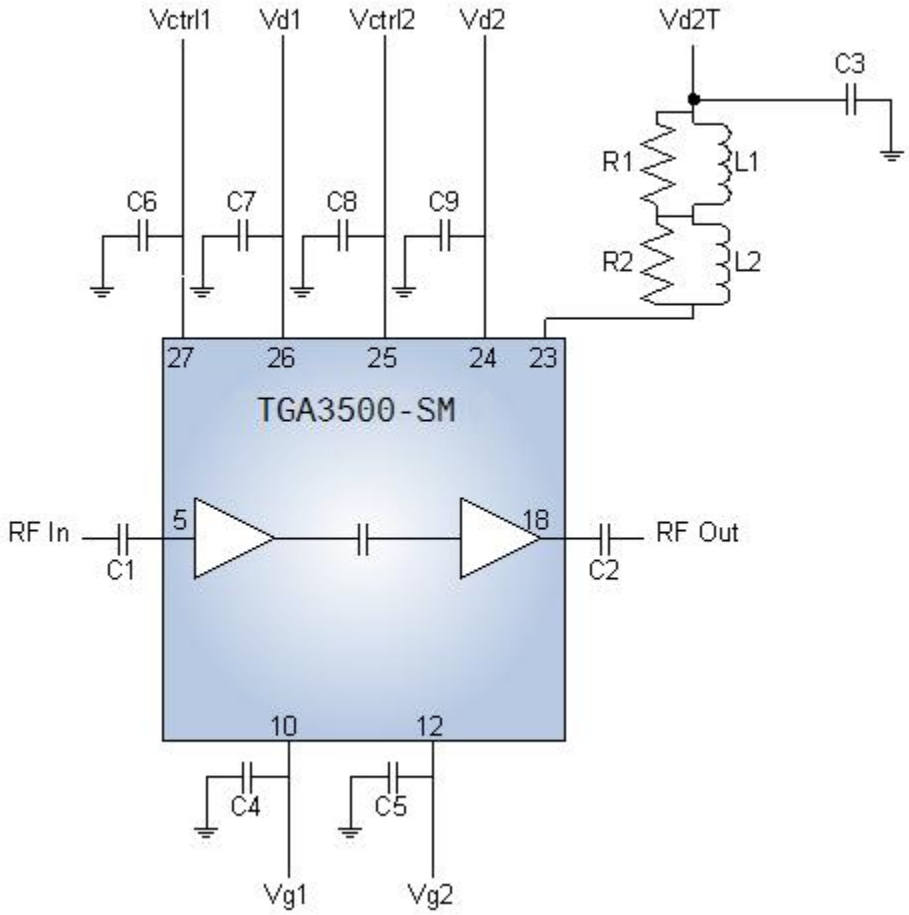
IMD3 vs. Output Power vs. Frequency



NF vs. Frequency



Application Circuit



Notes: To prevent damage to the device due to overshoot or oscillation issues, we recommend that current limits for all power supplies are set properly for each power supply before applying the voltage. The following are recommended current limits for each power supply:

Set 10 mA current limit to V_{G1} and V_{G2}
Set 20 mA current limit to V_{CTRL1} and V_{CTRL2}
Set 300 mA current limit to V_{D1} and V_{D2T}

Bias-up Procedure

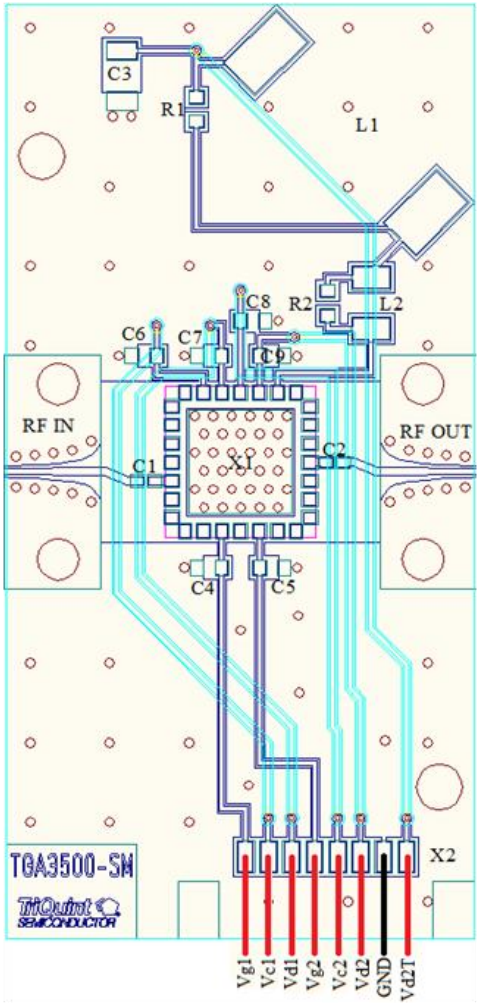
1. Apply -1.5 V V_{G1} andV_{G2}.
2. Apply -0.6 V to V_{CTRL1}.
3. Apply +0.2 V to V_{CTRL2}.
4. Apply 5 V to V_{D1} and V_{D2T}.
5. Adjust V_{G1} until I_{D2T} = 40 mA (V_{G1} ~ -0.7 V Typ.).
6. Adjust V_{G2} until I_{D2T} = 200 mA (V_{G2} ~ -0.6 V Typ.).
7. Turn on RF power.

Bias-down Procedure

1. Turn off RF supply.
2. Reduce V_{G2} and V_{G1} to -1.5 V.
3. Set V_{CTRL2} to 0 V.
4. Set V_{CTRL1} to 0 V.
5. Set V_{D1} and V_{D2T} to 0 V.
6. Set V_{G2} to 0 V.
7. Set V_{G1} to 0 V.

Recommended Board Layout Assembly

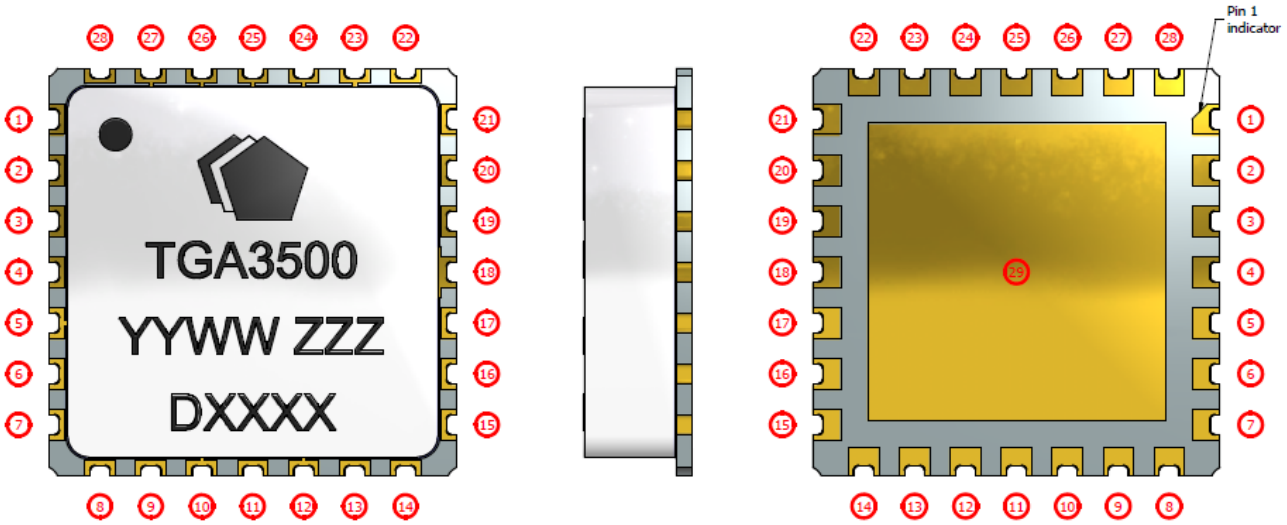
Top dielectric material is R40030 0.008 inch thickness with 0.5 oz. copper, and bottom dielectric material is FR4 0.008 inch.



Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
L1	220 uH	Fixed inductor CHOKE COIL	Panasonic	ELL-CTV221M
L2	330 uH	Fixed Inductor	Panasonic	ELJ-FAR33MF2
R1, R2	270 Ohms	Resistor, 0603 (SMD)	Panasonic	ERJ-3GEYJ271V
C1, C2	2.2 pF	Cap, 0402, 50V, 5% (SMD/SMT)	Murata	GJM1555C1H2R2WB01D
C3	10 uF	Cap, Tantalum, 16V, 10% (SMD)	AVX	TAJA106K016R
C4, C5, C7, C9	10 uF	Cap, 0603, 6.3V, 20 %, X5R	Murata	GRM188R60J106ME47D
C6, C8	0.1 uF	Cap, 0603, 16V, 20% (SMT/SMD)	AVX	0603YG104ZAT2A

Pin Layout



Pin Description

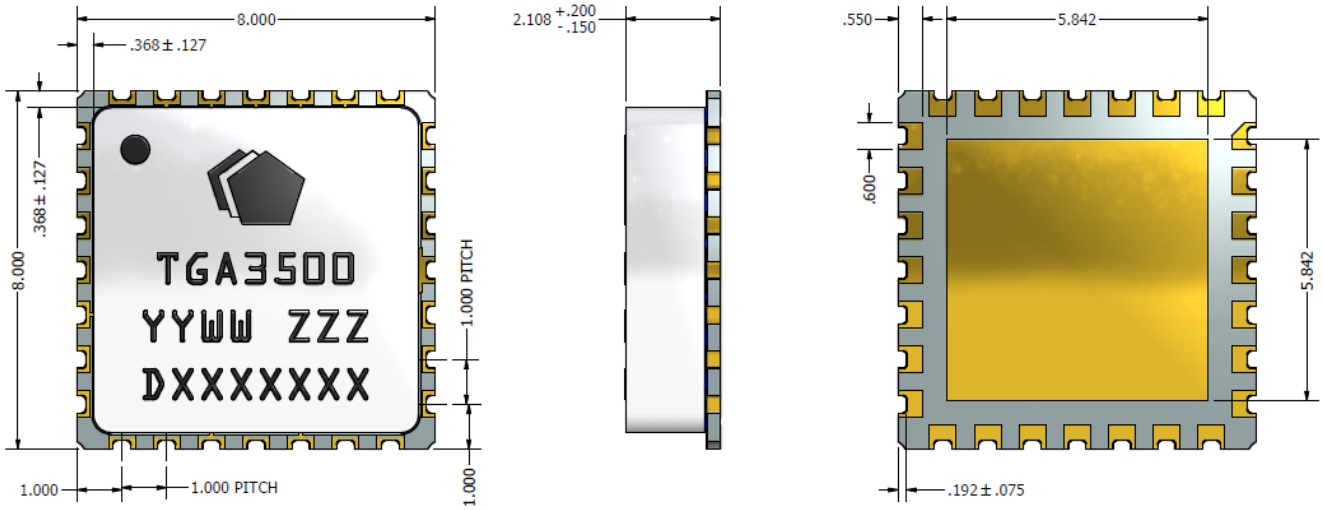
Pin	Symbol	Description
1-4, 6-9, 11, 13, 19-22, 28	N/C	No internal connection; must be grounded on PCB.
5	RF IN	RF input.
10	V_{G1}	Gate voltage. Bias network is required. (1)
12	V_{G2}	Gate voltage. Bias network is required. (1)
18	RF OUT	RF output.
23	V_{D2T}	Drain voltage. Bias network is required. (1)
24	V_{D2}	Drain voltage. Left unconnected.
25	V_{CTRL2}	Control voltage. Bias network is required. (1)
26	V_{D1}	Drain voltage. Bias network is required. (1)
27	V_{CTRL1}	Control voltage. Bias network is required. (1)
29	GND	Backside paddles; must be grounded on PCB. Multiple vias should be employed to minimize inductance and thermal resistance. (2)

Notes:

1. See Application Circuit on page 6 as an example.
2. See Mounting Configuration on page 9 for suggested footprint.

Mechanical Information

All dimensions are in millimeters. Unless specified otherwise, tolerances: ± 0.100 mm.



Marking: Part number – TGA3500
Year/week code – YYWW
Serial No. – ZZZ
Batch ID – DXXXX

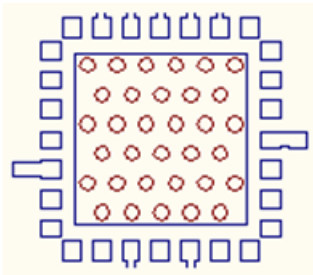
Package Materials:

Base	Aluminum Nitride (AIN)
Lid	White Alumina Al_2O_3

Contact Pin Plating:

Electroless Gold (Au)	0.5 – 1.0 µm
over	
Electroless Nickel (Ni)	2.0 µm min.

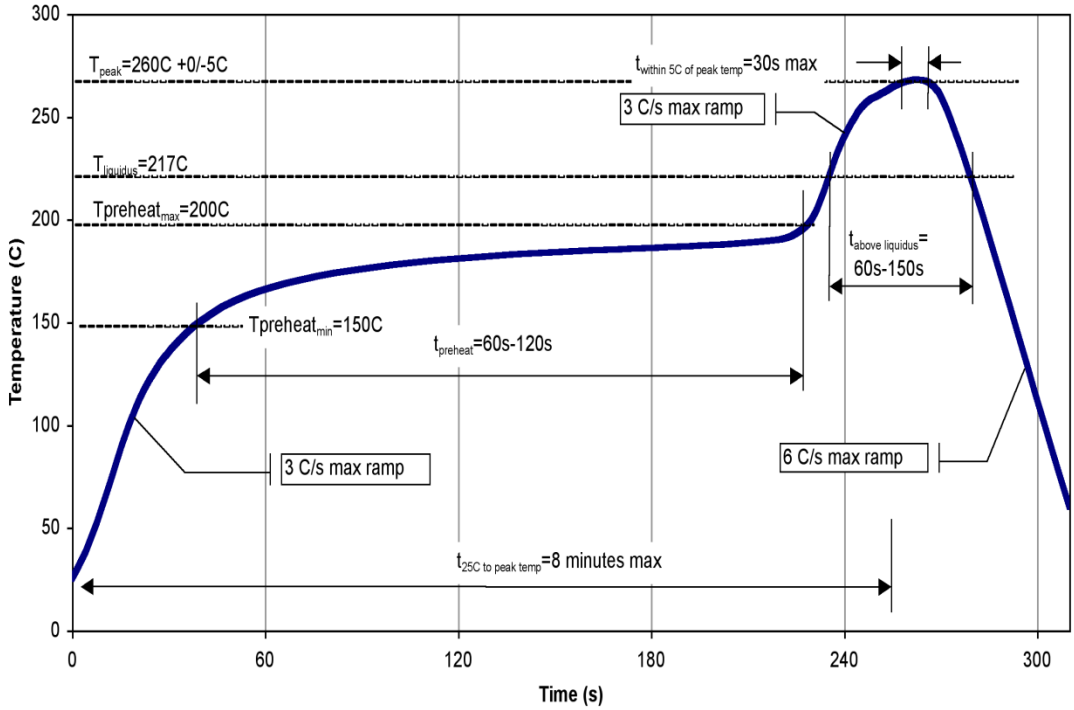
PCB Mounting Pattern



The pad pattern shown above has been developed and tested for optimized assembly at TriQuint. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.0008 in. diameter drill, and they are solid filled, copper plated shut or silver filled paste with over plating.

Recommended Soldering Temperature Profile



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: 1B
Value: (500 – 1000 V)
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

Level 1 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

ECCN

US Department of Commerce: EAR99

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°C

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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For technical questions and application information: **Email:** info-products@triquint.com

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