

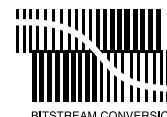


# TEA685X

## DSP-based radio tuner one-chip

Rev. 1.8 — 18 October 2013

Preliminary data sheet



## 1. General description

The TEA685X is a single-chip AM/FM tuner family with software-defined radio signal processing. The family succeeds the industry-proven TEF662X tuner family, with improved performance and increased feature set.

The devices are available in HVQFN packages occupying only smallest PCB real estate and are suitable for dual- to multi-layer PCBs.

The radio receiver includes the FM/AM front-ends, tuning synthesizer, channel filtering, demodulation, FM stereo decoding, weak signal processing, noise blanking and DARC (TEA6852, TEA6853) support.

Stereo audio is provided in digital format on the I<sup>2</sup>S (TEA6853) outputs and on the audio DAC outputs.

The TEA6853 supports the HD Radio and Digital Radio Mondiale (DRM) digital radio standards when used with NXP Semiconductors' digital radio coprocessors such as SAF356X and SAF360X.

## 2. Features and benefits

- Alignment free digital receiver including tuner and software-defined radio processing
- Command based high-level user interface combining high control flexibility with ease of control
- Read information with device and tuning status, reception quality and RDS data
- FM receiver with a tuning range of 76 MHz to 108 MHz covering Japan, Europe and US bands (TEA6850)
- FM receiver with a tuning range of 65 MHz to 108 MHz covering Japan, Europe, US and Eastern Europe bands (OIRT) (TEA6851, TEA6852, TEA6853)
- AM receiver covering LW, MW and full SW (TEA6853)
- Fully integrated tuning system with low phase noise and fast tuning
- FM LNA with AGC
- FM mixer for frequency conversion to a low IF complex signal
- AM LNA with AGC, matching active and passive antenna applications
- AM mixer for frequency conversion to a low IF complex signal, AM SW (TEA6853)
- High dynamic range IF ADC



- Digital IF signal processing including decimation, shift to baseband, AGC control, I/Q correction, variable IF bandwidth filtering (PACS) and demodulation
- FM stereo decoding
- Baseband I<sup>2</sup>S output supporting HD Radio and DRM<sup>1</sup> with external digital radio coprocessor (TEA6853)
- Blending function for HD Radio reception (TEA6853)
- AM and FM noise blanking, Signal quality detection and weak signal processing
- Advanced RDS and RBDS demodulation and decoding (TEA6852, TEA6853)
- MPX output supporting DARC demodulator (TEA6852, TEA6853)
- One I<sup>2</sup>S input and one I<sup>2</sup>S output (TEA6853)
- Two mono audio DACs
- Single 3.3 V supply voltage
- Fast mode I<sup>2</sup>C-bus (400 kHz)
- Configurable GPIO pins for RDS (TEA6852, TEA6853), and generic I<sup>2</sup>C-bus controlled I/O

### 3. Applications

The TEA685X is a single tuner AM/FM receiver for aftermarket and consumer applications and supports analog AM/FM and HD/DRM reception (HD/DRM is supported in TEA6853 only).

1. DRM includes DRM30 and DRM+ (band I and II)

## 4. Functionality

Table 1. Feature set

Features	TEA6850	TEA6851	TEA6852	TEA6853
<b>Standard</b>				
Digital to Analog converters (stereo audio DAC)	1	1	1	1
Audio I <sup>2</sup> S input/output	-	-	-	Yes
HD Radio	-	-	-	Yes
DRM	-	-	-	Yes
FM (US, Japan, Europe)	Yes	Yes	Yes	Yes
OIRT FM	-	Yes	Yes	Yes
LW - MW	Yes	Yes	Yes	Yes
SW	-	-	-	Yes
MPX output	-	-	Yes	Yes
<b>Standard Radio features</b>				
RDS demodulator and decoder	-	-	Yes	Yes
FM PACS	Yes	Yes	Yes	Yes
AM and FM soft mute	Yes	Yes	Yes	Yes
AM and FM high cut	Yes	Yes	Yes	Yes
AM and FM stereo blend	Yes	Yes	Yes	Yes
<b>Advanced Radio features</b>				
Enhanced Multipath Suppression (EMS)	-	Yes	Yes	Yes
AM and FM noise blanking	Yes	Yes	Yes	Yes

## 5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA6850HN/V102	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm <sup>[1]</sup>	SOT617-3
TEA6851HN/V102			
TEA6852HN/V102			
TEA6853HN/V102			

[1] Wettable sides to allow for optical inspection.

## 6. Block diagram

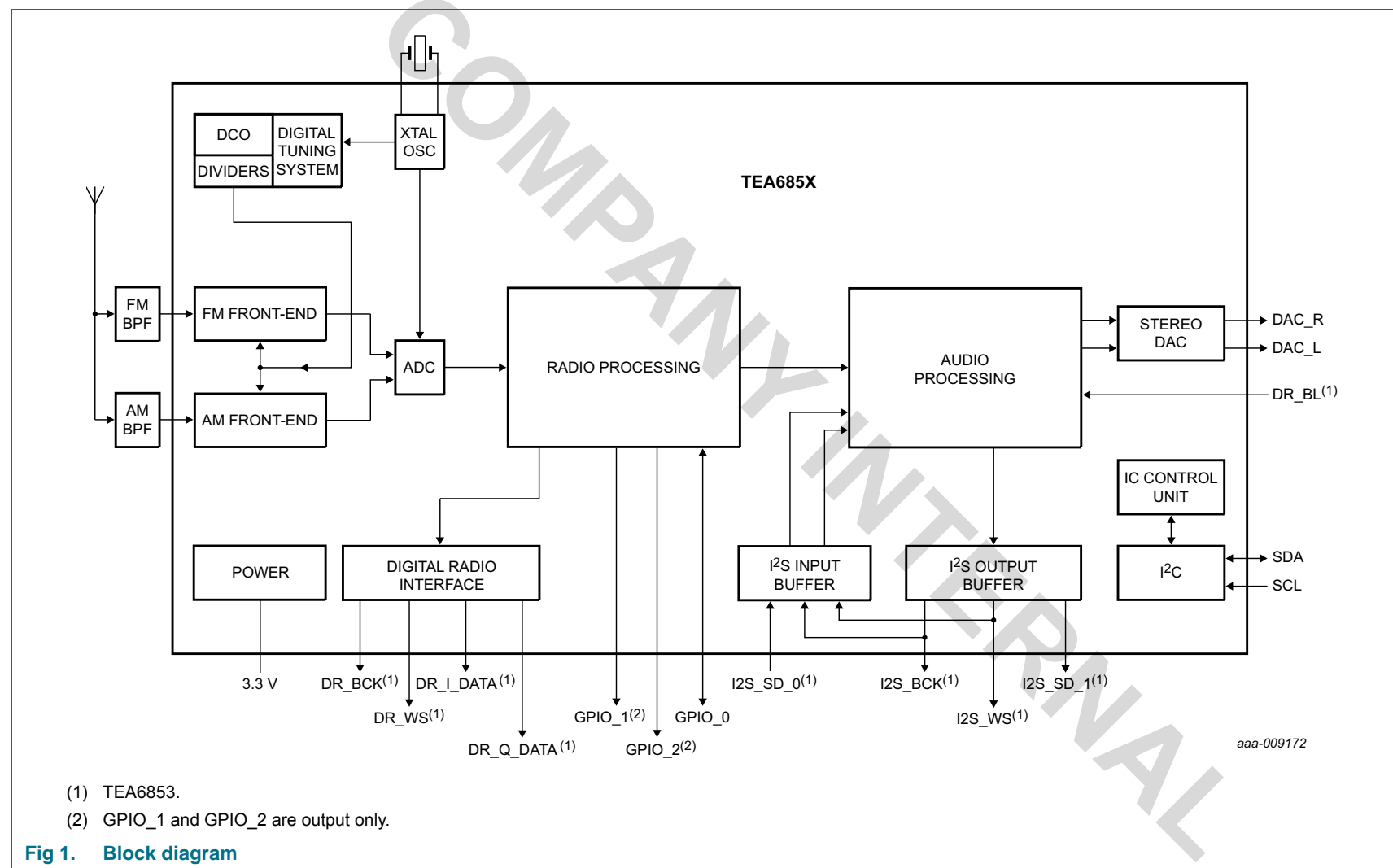
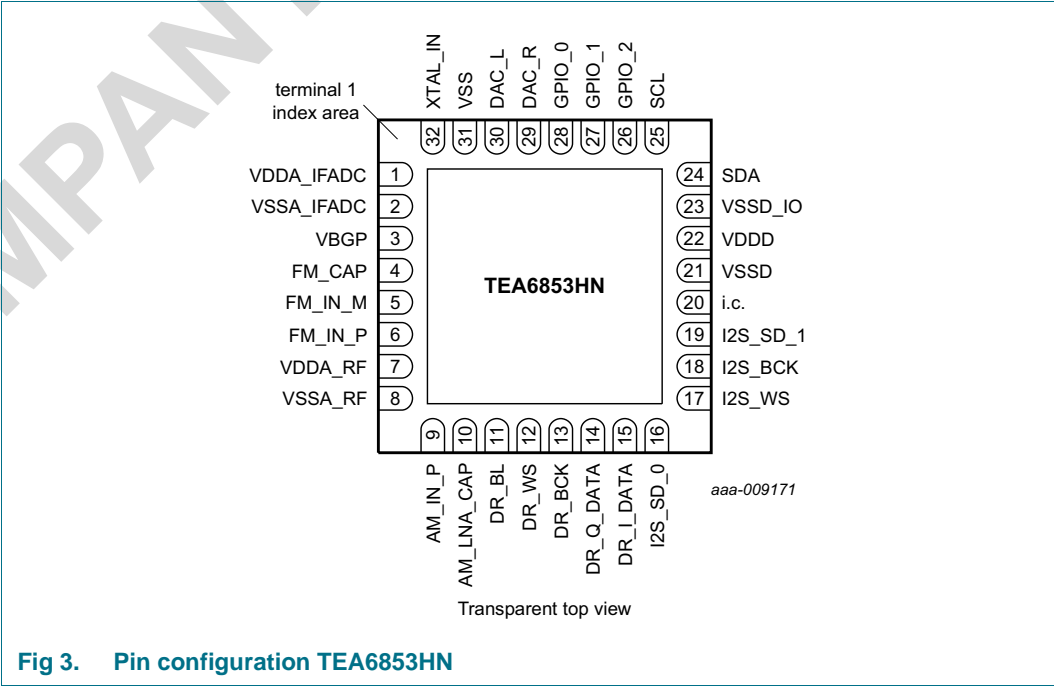
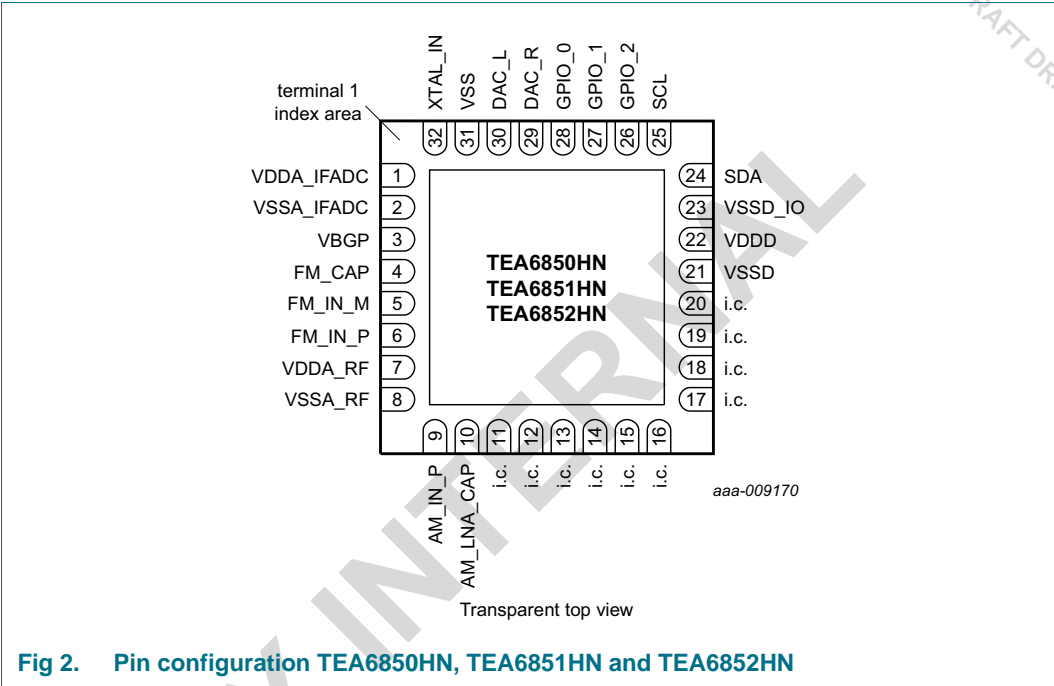


Fig 1. Block diagram

7. Pinning information



## 7.1 Pin description

Table 3. Pin description

Symbol	TEA6850 TEA6851 TEA6852 Pin	TEA6853 Pin	Pull-up or pull-down	Type <sup>[1]</sup>	Description
VDDA_IFADC	1	1	-	AP	IF ADC analog supply voltage
VSSA_IFADC	2	2	-	AG	IF ADC analog ground supply voltage
VBGP	3	3	-	AR	bandgap reference voltage decoupling
FM_CAP	4	4	-	AI	FM AGC capacitor
FM_IN_M	5	5	-	AI	negative FM RF input
FM_IN_P	6	6	-	AI	positive FM RF input
VDDA_RF	7	7	-	AP	RF analog supply voltage
VSSA_RF	8	8	-	AG	RF analog ground supply voltage
AM_IN_P	9	9	-	AI	positive AM LNA input
AM_LNA_CAP	10	10	-	AI	AM LNA AGC capacitor
i.c.	11	-	-	-	internally connected, leave open
DR_BL	-	11	-	I	HD Radio signal FM blend
i.c.	12	-	-	-	internally connected, leave open
DR_WS	-	12	-	O	digital radio word select output
i.c.	13	-	-	-	internally connected, leave open
DR_BCK	-	13	-	O	digital radio bit clock output
i.c.	14	-	-	-	internally connected, leave open
DR_Q_DATA	-	14	-	O	serial data output for digital radio quadrature-phase data
i.c.	15	-	-	-	internally connected, leave open
DR_I_DATA	-	15	-	O	serial data output for digital radio in-phase data
i.c.	16	-	-	-	internally connected, leave open
I2S_SD_0	-	16	D	I/O	I <sup>2</sup> S data
i.c.	17	-	-	-	internally connected, leave open
I2S_WS	-	17	D	I/O	I <sup>2</sup> S word select input/output <sup>[2]</sup>
i.c.	18	-	-	-	internally connected, leave open
I2S_BCK	-	18	D	I/O	I <sup>2</sup> S bit clock input/output <sup>[2]</sup>
i.c.	19	-	-	-	internally connected, leave open
I2S_SD_1	-	19	D	I/O	I <sup>2</sup> S data
i.c.	20	20	-	-	internally connected, leave open
VSSD	21	21	-	G	3.3 V digital ground supply voltage
VDDD	22	22	-	P	3.3 V digital supply voltage
VSSD_IO	23	23	-	G	digital input/output ground connection
SDA	24	24	U	I <sup>2</sup> C	I <sup>2</sup> C-bus serial data input and output
SCL	25	25	U	I <sup>2</sup> C	I <sup>2</sup> C-bus serial clock input
GPIO_2	26	26	-	O	General Purpose output

Table 3. Pin description ...continued

Symbol	TEA6850 TEA6851 TEA6852 Pin	TEA6853 Pin	Pull-up or pull-down	Type <sup>[1]</sup>	Description
GPIO_1	27	27	-	O	General Purpose output
GPIO_0	28	28	-	I/O	General Purpose Input/Output
DAC_R	29	29	-	AO	right channel audio Output
DAC_L	30	30	-	AO	left channel audio Output
VSS	31	31	-	G	ground connection
XTAL_IN	32	32	-	AI	crystal oscillator input

[1] The pin types are defined in [Table 4](#).

[2] Pins are either both inputs or both outputs.

Table 4. Pin type description

Type	Description
AI	analog input pin
AG	analog ground pin
AO	analog output pin
AP	analog power pin
AR	analog reference pin
G	ground pin
I	input
I/O	input or output
I <sup>2</sup> C	I <sup>2</sup> C-bus pin; 3.3 V tolerant
O	output
P	power supply pin

## 8. Functional description

### 8.1 FM front-end to IF ADC input

The RF input signal from the antenna is filtered by an external wideband band-pass RF filter. The RF filter passes the complete FM band of interest and provides impedance transformation for the antenna impedance matching.

The RF filter output signal is applied to the high dynamic range FM LNA. The LNA gain is controlled by the integrated AGC loop. The AGC range is seven steps of 6 dB. The input impedance of the LNA remains constant over the first five AGC steps and is reduced for the last two AGC steps.

The signal from the LNA is converted to a low IF using a complex mixer which includes image rejection. The IF signal from the mixer is amplified and filtered before the IF signal is digitized by the IF ADC.

## 8.2 AM front-end to IF ADC input

The RF input signal from the antenna is filtered by an external high-pass filter and an FM frequency band reject filter. The high-pass filter attenuates 50 Hz/60 Hz signals from power supply lines. The band reject filter or FM intrusion filter attenuates the FM signals before entering the AM LNA, preventing intermodulation from two FM signals degrading AM reception.

After filtering, the RF signal is applied to the AM LNA. The gain of the AM LNA can be controlled with up to ten 6 dB steps by the integrated AGC loop. The input capacitance of the AM LNA is constant over the first seven steps of AGC range and is reduced for the last three AGC steps.

In AM LW and MW mode, the LNA output signal is filtered before being applied to the IF ADC. The lack of frequency conversion eliminates performance limitations due to reception of image and harmonic local oscillator frequencies.

In AM SW mode (TEA6853), the LNA output signal is filtered and applied to a complex image reject mixer for frequency conversion to low IF. This IF signal is amplified and filtered before it is digitized by the IF ADC.

## 8.3 Tuning system

The PLL tuning system provides the LO signal to drive the AM-SW (TEA6853) and FM mixer for frequency conversion to low IF. The tuning system is capable of tuning to the US, European, Japan, and OIRT FM bands (TEA6851, TEA6852 and TEA6853) and the full AM SW band (TEA6853). The tuning system combines low phase noise with fast tuning times.

## 8.4 IF ADC

The IF signal is digitized by a high dynamic range sigma-delta IF ADC. Due to the high dynamic range, there is no need for narrowband IF filtering. The IF ADC provides two bitstreams (I and Q data) to the radio processing block.

## 8.5 Radio processing

Radio processing performs the following functions:

- Decimation of the IF ADC bit streams
- Shift to baseband
- AGC compensation
- Linear AGC detection and control
- I/Q error detection and correction
- Interface to terrestrial digital radio processor for HD Radio signals or DRM reception (TEA6853)
- Channel filtering
- AM/FM demodulation
- Ignition noise detection and correction
- FM stereo decoding
- Programmable de-emphasis



- Quality detection
- Weak signal handling
- RDS/RBDS demodulation, decoding and error correction (TEA6852, TEA6853)

The output of the radio processing block is a left and right digital audio signal.

### 8.5.1 AM mode features

The channel filter rejects adjacent channels. The bandwidth of this channel filter can be programmed.

Ignition noise pulses are suppressed by the AM noise blanker, consisting of an IF noise blanker in front of the channel filter and an audio noise blanker after AM demodulation.

The following quality detectors are used to measure the quality of the signal reception:

- RSSI or field strength detection (level)
- Frequency offset detection
- AM modulation detection

The signal quality in weak reception conditions is improved by the AM weak signal handling consisting of:

- Soft mute controlled by level
- High-cut controlled by level

### 8.5.2 FM mode features

The TEA6851, TEA6852 and TEA6853 offer the premium feature Enhanced Multipath Suppression. The Enhanced Multipath Suppression algorithm reduces the audibility of multipath distortions.

Adjacent channels are rejected by the channel filter. The bandwidth of the channel filter is variable and is dynamically controlled by the FM PACS algorithm. The bandwidth depends on the adjacent channel conditions and properties of the desired signal such as modulation and signal strength.

Ignition noise pulses are detected and suppressed by the noise blanker

The following quality detectors are used to measure the quality of the signal reception:

- RSSI or field strength detection (level)
- Frequency offset detection
- Multipath and adjacent channel detection by USN detection
- Multipath detection by WAM detection
- Frequency deviation by modulation detection
- Stereo pilot detection

The signal quality under weak signal and multipath conditions is improved by the FM weak signal handling, consisting of:

- Soft mute controlled by level, USN and WAM
- HighCut controlled by level, USN and WAM

- Stereo Blend controlled by level, USN and WAM

### 8.5.3 RDS/RBDS

An RDS demodulator and RDS decoder in the TEA6852 and TEA6853 processes the data received from RDS and RBDS transmissions with excellent RDS sensitivity.

#### 8.5.3.1 RDS demodulator

The RDS demodulator includes optimized filtering and linear signal processing that allows very good RDS sensitivity. The MPX signal is filtered for selection of the 57 kHz RDS signal and data shaping. The RDS demodulator data is fed into the RDS decoder for further processing. To support available software stacks the RDS demodulator data can also be read directly via the I<sup>2</sup>C-bus or GPIO pins.

#### 8.5.3.2 RDS decoder

The RDS decoder provides synchronization to the block and group structure of the demodulated RDS data stream. When synchronized, the decoder delivers data in a fixed ABCD group order for easy software handling. In the background, synchronization search continues for fast correction on bit slip or other synchronization errors. Extended error detection and correction is included.

An I<sup>2</sup>C register indicates the availability of a new group. An interrupt signal 'data available' can be provided on a GPIO pin.

'Data available' is indicated whenever a new group is received (that is at reception of block D). For fast PI code reception, at synchronization start 'data available' is flagged on reception of the first PI code, such as block A or block C'.

### 8.5.4 Digital radio interface

For HD Radio and DRM reception (TEA6853), the baseband signal is output to an external digital radio coprocessor, such as the NXP Semiconductors' SAF356X or SAF360X. The baseband I<sup>2</sup>S output includes a Bit Clock (BCK), Word Select (WS) and the in-phase and quadrature-phase data signals (I-data and Q-data).

## 8.6 Audio input

One I<sup>2</sup>S audio input (TEA6853) is available supporting sample rates 44.1 kHz and 48 kHz.

## 8.7 Audio processing

The audio processing block has the following features:

- Volume control including mute
- HD Radio blending (TEA6853)

## 8.8 Audio output

The audio output includes two mono DACs and one I<sup>2</sup>S audio output (TEA6853) supporting sample rates 44.1 kHz and 48 kHz.

## 8.9 Crystal oscillator

In a stand-alone AM/FM application, that is the digital radio interface is not used, the reference clock for the TEA685X system is provided by a crystal oscillator with a frequency of 4.000 MHz, 9.216 MHz or 12.000 MHz. In a system using digital radio coprocessors SAF356X or SAF360X, the crystal for the TEA6853 must be 9.216 MHz or 12.000 MHz.

## 8.10 I<sup>2</sup>C-bus interface

The TEA685X is controlled by means of the I<sup>2</sup>C-bus interface. The I<sup>2</sup>C-bus interface supports the fast mode of 400 kbit/s according the I<sup>2</sup>C-bus specification.

The I<sup>2</sup>C address selection is defined by the voltage levels on GPIO\_2 pin during power up. The I<sup>2</sup>C address is C8h (default) or can be configured to be CAh. The I<sup>2</sup>C address selection table is defined in the application note [Ref. 6](#)

A logic 0 requires a 10 kΩ pull-down resistor to ground, whereas for a logic 1 the pin must be connected to the 3.3 V supply voltage by a 10 kΩ pull-up resistor.

# 9. I<sup>2</sup>C-bus protocol

The user manual [Ref. 7](#) describes the software control interface for the TEA685X.

## 9.1 Write mode

Standard write transmissions consist of an I<sup>2</sup>C-bus start condition and an 8-bit hardware device address for write as defined by the I<sup>2</sup>C-bus standard. Next, an 8-bit module identifier for FM, AM, audio, system and other parts. Control is indicated by an 8-bit command identifier and an 8-bit parameter index, followed by one or more 16-bit parameters.

Writing data to inactive modules is supported and this data is stored. Stored data is used upon activation of the module.

## 9.2 Read mode

Standard read transmissions consist of writing a read request followed by the actual read transmission to obtain data.

**Remark:** The I<sup>2</sup>C-bus standard does not allow read addressing within a read transmission.

Received data or status information is read using special Get commands that include an index setting similar to Write definitions which are required for reading large data blocks and for future extendability.

A command with index 0 returns the module and command value. These commands are useful to allow for instances where requested data cannot be returned in time due to internal data handling delays.

In special cases, Get commands with index 0 or 1 require data to be read from the start. Read data with index is useful to read data blocks of a particular size, in case read buffers have limited size.

## 10. Overview of commands

Table 5. Write commands overview

Module	Command number	Command name	Parameter 1	Parameter 2	Parameter 3	Parameter 4
FM/AM	1	Tune_To	mode	frequency (kHz)	-	-
FM	2	Set_Tune_Options	afu_bw mode	afu_bandw (kHz)	mute_time (ms)	sample_time (ms)
FM/AM	10	Set_Bandwidth	mode	bandwidth (kHz)	sensitivity (%)	lo_sensitivity (%)
FM/AM	11	Set_RFAGC	start (dB $\mu$ V)	-	-	-
AM	12	Set_Antenna	attenuation (dB)	-	-	-
FM	20	Set_MphSuppression <sup>[1]</sup>	mode	-	-	-
FM/AM	23	Set_NoiseBlanker	mode	sensitivity (%)	-	-
AM	24	Set_NoiseBlanker_Audio	mode	sensitivity (%)	-	-
FM/AM	30	Set_DigitalRadio <sup>[2]</sup>	mode	-	-	-
FM	31	Set_Deemphasis	timeconstant ( $\mu$ s)	-	-	-
FM/AM	38	Set_LevelStep	step1 (dB)	step2 (dB)	step3 (dB)	step4 (dB)
FM/AM	39	Set_LevelOffset	offset (dB)	-	-	-
FM/AM	40	Set_SoftMute_Time	slow_attack (ms)	slow_decay (ms)	fast_attack (ms)	fast_decay (ms)
FM/AM	42	Set_SoftMute_Level	mode	start (dB $\mu$ V)	slope (dB)	-
FM	43	Set_SoftMute_Noise	mode	start (%)	slope (%)	-
FM	44	Set_SoftMute_Mph	mode	start (%)	slope (%)	-
FM/AM	45	Set_SoftMute_Max	mode	limit (dB)	-	-
FM/AM	50	Set_HighCut_Time	slow_attack (ms)	slow_decay (ms)	fast_attack (ms)	fast_decay (ms)
FM/AM	52	Set_HighCut_Level	mode	start (dB $\mu$ V)	slope (dB)	-
FM	53	Set_HighCut_Noise	mode	start (%)	slope (%)	-
FM	54	Set_HighCut_Mph	mode	start (%)	slope (%)	-
FM/AM	55	Set_HighCut_Max	mode	limit (Hz)	-	-
FM/AM	56	Set_HighCut_Min	mode	limit (Hz)	-	-
FM/AM	58	Set_LowCut_Min	mode	limit (Hz)	-	-
FM/AM	59	Set_HighCut_Options	mode	-	-	-
FM	60	Set_Stereo_Time	slow_attack (ms)	slow_decay (ms)	fast_attack (ms)	fast_decay (ms)
FM	62	Set_Stereo_Level	mode	start (dB $\mu$ V)	slope (dB)	-
FM	63	Set_Stereo_Noise	mode	start (%)	slope (%)	-
FM	64	Set_Stereo_Mph	mode	start (%)	slope (%)	-
FM	66	Set_Stereo_Min	mode	limit (dB)	-	-
FM/AM	80	Set_Scaler	gain (dB)	-	-	-
FM	81	Set_RDS <sup>[3]</sup>	mode	restart	interface	-
FM/AM	82	Set_QualityStatus	mode	interface	-	-
FM/AM	83	Set_DR_Blend <sup>[2]</sup>	mode	in_time (ms)	out_time (ms)	gain (dB)

## NXP Semiconductors

# TEA685X

### DSP-based radio tuner one-chip

**Table 5. Write commands overview ...continued**

Module	Command number	Command name	Parameter 1	Parameter 2	Parameter 3	Parameter 4
FM/AM	84	Set_DR_Options <sup>[2]</sup>	samplerate	-	-	-
FM/AM	85	Set_Specials <sup>[4]</sup>	ana_out	-	-	-
AUDIO	10	Set_Volume	volume (dB)	-	-	-
AUDIO	11	Set_Mute	mode	-	-	-
AUDIO	12	Set_Input <sup>[5]</sup>	source	-	-	-
AUDIO	21	Set_Ana_Out	signal	mode	-	-
AUDIO	22	Set_Dig_IO <sup>[2]</sup>	signal	mode	format	operation
			samplerate	-	-	-
AUDIO	23	Set_Input_Scaler <sup>[2]</sup>	source	gain (dB)	-	-
AUDIO	24	Set_WaveGen <sup>[6]</sup>	mode	offset	amplitude1	frequency1
			amplitude2	frequency2	-	-
APPL	1	Set_OperationMode	mode	-	-	-
APPL	3	Set_GPIO	pin	module	feature	-

[1] TEA6851, TEA6852 and TEA6853 only.

[2] TEA6853 only.

[3] TEA6852 and TEA6853 only.

[4] DARC is available in TEA6852 and TEA6853. Digital radio is available in TEA6853.

[5] I2S input only available in TEA6853.

[6] For test purposes only.

**Table 6. Read commands overview**

Module	Command number	Command name	1	2	3	4
FM/AM	128	Get_Quality_Status	status	level	usn	warn
			offset	bandwidth	modulation	-
FM/AM	129	Get_Quality_Data	status	level	usn	warn
			offset	bandwidth	modulation	-
FM	130	Get_RDS_Status <sup>[1]</sup>	status	a_block	b_block	c_block
			d_block	dec_error	-	-
FM	131	Get_RDS_Data <sup>[1]</sup>	status	a_block	b_block	c_block
			d_block	dec_error	-	-
FM/AM	132	Get_AGC	input_att	feedback_att	-	-
FM/AM	133	Get_Signal_Status	status	-	-	-
FM/AM	134	Get_Processing_Status	softmute	highcut	stereo	-
FM/AM	135	Get_Interface_Status <sup>[2]</sup>	samplerate	-	-	-
APPL	128	Get_Operation_Status	status	-	-	-
APPL	129	Get_GPIO_Status	status	-	-	-

## NXP Semiconductors

# TEA685X

### DSP-based radio tuner one-chip

**Table 6.** Read commands overview ...continued

Module	Command number	Command name	1	2	3	4
APPL	130	Get_Identification	device	hw_version	sw_version	-
APPL	131	Get_LastWrite	size/module parameter	cmd/index parameter	parameter parameter	parameter parameter

[1] TEA6852 and TEA6853 only.

[2] TEA6853 only.

## 11. Limiting values

**Table 7.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(RF)(3V3)}$	RF analog supply voltage (3.3 V)	on pin VDDA_RF	-0.5	+3.9	V
$V_{DDA(IF)(3V3)}$	IF analog supply voltage (3.3 V)	on pin VDDA_IFADC	-0.5	+3.9	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	on pin VDDD	-0.5	+3.9	V
$\Delta V_{DD(3V3-3V3)}$	supply voltage difference between two 3.3 V supplies	between pins VDDA_IFADC and VDDA_RF	-0.3	+0.3	V
$V_n$	voltage on any other pin		-0.5	+ $V_{DDD(3V3)} + 0.3$	V
$I_{lu}$	latch-up current	all supply voltages below the maximum value	-100	+100	mA
$V_{lu}$	latch-up voltage		-	$1.5 \times V_{DDD(3V3)}$	V
$T_{stg}$	storage temperature		-40	+150	°C
$T_{amb}$	ambient temperature		-20	+85	°C
$T_j$	junction temperature		-	+125	°C
$V_{ESD}$	electrostatic discharge voltage	human body model	[1] -2000	+2000	V
		charged-device model			
		corner pins	-750	+750	V
		other pins	-500	+500	V
$P_{tot}$	total power dissipation	$V_{DDA(RF)(3V3)} = 3.5$ V; $V_{DDA(IF)(3V3)} = 3.5$ V; $V_{DDD(3V3)} = 3.5$ V	-	700	mW

[1] In accordance with JESD22-A114 Class 2.

## 12. Thermal characteristics

**Table 8.** Thermal characteristics

The performance parameters are specified with center pin soldered to the board

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVQFN32 dual-layer board	[1] 50	K/W

[1] Simulation result assuming a dual layer board with a copper thickness of 35 µm; size: 50 × 50 mm; exposed die pad soldered to thermal landing pattern; thermal landing pattern connected to a large ground plane on the bottom layer by multiple thermal vias; copper coverages 25 % (top layer) and 90 % (bottom layer).

## 13. Static characteristics

**Table 9. Voltage and current characteristics**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply voltage</b>						
$V_{DDA(RF)(3V3)}$	RF analog supply voltage (3.3 V)	on pin VDDA_RF	3.0	3.3	3.5	V
$V_{DDA(IF)(3V3)}$	IF analog supply voltage (3.3 V)	on pin VDDA_IFADC	3.0	3.3	3.5	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	on pin VDD_DIGITAL	3.0	3.3	3.5	V
<b>Current in FM mode</b>						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF	33	37	42	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC	81	94	110	mA
$I_{DDD}$	digital supply current	on pin VDDD	37	38	48	mA
<b>Current in AM - MW/LW mode</b>						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF	34	40	48	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC	63	74	86	mA
$I_{DDD}$	digital supply current	on pin VDDD	33	34	46	mA
<b>Current in Standby mode</b>						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF	0	0.3	2	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC	25	37	45	mA
$I_{DDD}$	digital supply current	on pin VDDD	15	24	35	mA

## 14. Dynamic characteristics

**Table 10. Dynamic characteristics for audio processing and audio DAC**

$V_{DDA(RF)(3V3)} = 3.3$  V;  $V_{DDA(IF)(3V3)} = 3.3$  V;  $V_{DDD(3V3)} = 3.3$  V;  $f_s = 44.1$  kHz;  $T_{amb} = 25$  °C; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Audio processing</b>						
$G_{aud}$	audio gain		-60	-	+24	dB
$\alpha_{mute}$	mute attenuation		-	-	-80	dB
<b>Audio DAC</b>						
$V_o$	output voltage	at 0 dBFS digital input; $R_L = 20$ k $\Omega$	870	910	950	mV
		DARC output; $\Delta f = 22.5$ kHz; $f_{AF} = 1$ kHz; $V_{RF} = 60$ dB $\mu$ V	-	150	-	mV
$R_o$	output resistance		-	-	1	k $\Omega$
$\alpha_{o(unb)(ch-ch)}$	output unbalance between channels		-0.2	-	+0.2	dB
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	0 dBFS with unweighted 20 Hz to 20 kHz audio filter; $R_L = 20$ k $\Omega$	-	-	-70	dB
		-60 dBFS with A-weighted audio filter; $R_L = 20$ k $\Omega$	-	-	-27	dB



**Table 10. Dynamic characteristics for audio processing and audio DAC ...continued**

$V_{DDA(RF)(3V3)} = 3.3\text{ V}$ ;  $V_{DDA(IF)(3V3)} = 3.3\text{ V}$ ;  $V_{DDD(3V3)} = 3.3\text{ V}$ ;  $f_s = 44.1\text{ kHz}$ ;  $T_{amb} = 25\text{ °C}$ ; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{n(o)(RMS)}$	RMS output noise voltage	in-band noise on idle channel, A-weighted	-	-	36	$\mu\text{V}$
$\alpha_{cs}$	channel separation		70	-	-	dB
PSRR	power supply ripple rejection	$f_{ripple} = 1\text{ kHz}$ ; $V_{supply(ripple)}/V_{audio(ripple)}$	50	-	-	dB
$R_L$	load resistance		20	-	-	$k\Omega$
$f_{resp}$	frequency response	-3 dB corner frequency related to $f_{AF} = 1\text{ kHz}$	100	-	-	kHz
		low audio	-	-	20	Hz
		high audio	18	-	-	kHz

**Table 11. Dynamic characteristics for tuning system**

$V_{DDA(RF)(3V3)} = 3.3\text{ V}$ ;  $V_{DDA(IF)(3V3)} = 3.3\text{ V}$ ;  $V_{DDD(3V3)} = 3.3\text{ V}$ ; all AC values are RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Crystal oscillator</b>						
$f_{nom}$	nominal frequency	stand alone, digital radio interface not used	[1] -	4.000	-	MHz
			[1] -	9.216	-	MHz
			[1] -	12.000	-	MHz
		digital radio interface enabled	[2] -	9.216	-	MHz
			[2] -	12.000	-	MHz

[1] TEA6850, TEA6851 and TEA6852.

[2] TEA6853.

**Table 12. FM radio characteristics**

$f = 98\text{ MHz}$ ,  $\Delta f = 22.5\text{ kHz}$ ,  $f_{AF} = 1\text{ kHz}$ ,  $50\text{ }\mu\text{s}$  de-emphasis, IEC tuner filter  $75\text{ }\Omega/-6\text{ dB}$  dummy antenna, all signals in RMS at input dummy unless otherwise specified. Analog audio output at pins DAC\_L and DAC\_R

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{RF}$	RF frequency	FM tuning range	[1] 65	-	108	MHz
			[2] 76	-	108	MHz
$V_{i(sens)}$	input sensitivity voltage	$V_{i(RF)}$ for 26 dB SNR; weak signal handling enabled	-	4	-	$\text{dB}\mu\text{V}$
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)} = 50\text{ dB}\mu\text{V}$ to $130\text{ dB}\mu\text{V}$ ; mono	60	-	-	dB
		$V_{i(RF)} = 60\text{ dB}\mu\text{V}$ to $130\text{ dB}\mu\text{V}$ ; stereo	56	-	-	dB
$\alpha_{sup(AM)}$	AM suppression	$m = 30\%$ , $f_{AF} = 1\text{ kHz}$ ; $V_{i(RF)} = 40\text{ dB}\mu\text{V}$ to $120\text{ dB}\mu\text{V}$	58	68	-	dB
THD	total harmonic distortion	$f_{AF} = 1\text{ kHz}$ ; $V_{i(RF)} = 20\text{ dB}\mu\text{V}$ to $130\text{ dB}\mu\text{V}$				
		$\Delta f = 75\text{ kHz}$ ; mono	-	0.01	-	%
		$\Delta f = 67.5\text{ kHz}$ ; stereo; $L_{out}$ only	-	0.1	-	%



## NXP Semiconductors

# TEA685X

### DSP-based radio tuner one-chip

**Table 12. FM radio characteristics ...continued**

$f = 98 \text{ MHz}$ ,  $\Delta f = 22.5 \text{ kHz}$ ,  $f_{AF} = 1 \text{ kHz}$ ,  $50 \mu\text{s}$  de-emphasis, IEC tuner filter  $75 \Omega$ –6 dB dummy antenna, all signals in RMS at input dummy unless otherwise specified. Analog audio output at pins DAC\_L and DAC\_R

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S	selectivity	$V_{RF(wanted)} = 20 \text{ dB}\mu\text{V}$ ; $\Delta f = 22.5 \text{ kHz}$ for 0 dB ref; $f_{RF(unw)} = f_{RF(wanted)} \pm \Delta f_{RF}$ , $\Delta f = 22.5 \text{ kHz}$ ; $f_{AF} = 1 \text{ kHz}$ ; increased $V_{RF(unw)}$ until $\text{SNR} = 26 \text{ dB}$ ; $\text{DS} = V_{RF(unw)} / V_{RF(wanted)}$				
		$\Delta f_{RF} = 100 \text{ kHz}$	-	48	-	dB
		$\Delta f_{RF} = 200 \text{ kHz}$	-	70	-	dB
IP3	third-order intercept point	$f_{RF(unw)1} = \pm 400 \text{ kHz}$ ; $f_{RF(unw)2} = \pm 800 \text{ kHz}$	113	118	-	dB $\mu\text{V}$
IP2	second-order intercept point	$f_{RF(unw)1} = 50 \text{ MHz}$ and $f_{RF(unw)2} = 48 \text{ MHz}$	160	-	-	dB $\mu\text{V}$
$V_{i(RF)AGC(start)}$	start AGC RF input voltage	highest setting	86	-	90	dB $\mu\text{V}$
		lowest setting	86	-	90	dB $\mu\text{V}$
$\alpha_{cr(AGC)}$	AGC control range	internal AGC	-	40	-	dB
$\alpha_{cs}$	channel separation	$\Delta f = 67.5 \text{ kHz}$ ; $f_{AF} = 1 \text{ kHz}$ ; $\Delta f_{pilot} = 7.5 \text{ kHz}$ ; $V_{i(RF)} = 60 \text{ dB}\mu\text{V}$ to $120 \text{ dB}\mu\text{V}$	45	-	-	dB
$S_{RDS}$	RDS sensitivity	$\Delta f_{RDS} = 2 \text{ kHz}$ ; stereo $\Delta f_{FM} = 22.5 \text{ kHz}$ ; $L = R$ ; $f_{AF} = 1 \text{ kHz}$				
		50 % correct blocks without error correction	-	17	19	dB $\mu\text{V}$
		95 % correct blocks without error correction	-	20	22	dB $\mu\text{V}$
$V_o$	output voltage	$\Delta f = 22.5 \text{ kHz}$ ; $f_{AF} = 1 \text{ kHz}$ ; $V_{RF} = 60 \text{ dB}\mu\text{V}$	-	118	-	mV

[1] TEA6850.

[2] TEA6851, TEA6852 and TEA6853.

**Table 13. AM radio characteristics**

$m = 30 \%$ ;  $f_{AF} = 1 \text{ kHz}$ ; IEC tuner filter  $15 \text{ pF}/60 \text{ pF}$  dummy antenna; all signal levels in RMS at input dummy; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{RF}$	RF frequency	AM (LW) tuning range	144	-	288	kHz
		AM (MW) tuning range	522	-	1710	kHz
		AM (SW) tuning range <a href="#">[1]</a>	2.3	-	27.0	MHz
$V_{i(sens)}$	input sensitivity voltage	$\text{S/N} = 26 \text{ dB}$ ; $B_{aud} = 2 \text{ kHz}$ ; $f_{RF} = 990 \text{ kHz}$ ; $m = 30 \%$ ; $f_{AF} = 400 \text{ kHz}$	-	34	-	dB $\mu\text{V}$
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)} = 74 \text{ dB}\mu\text{V}$	60	63	-	dB

## NXP Semiconductors

# TEA685X

### DSP-based radio tuner one-chip

**Table 13. AM radio characteristics ...continued**

$m = 30\%$ ;  $f_{AF} = 1\text{ kHz}$ ; IEC tuner filter  $15\text{ pF}/60\text{ pF}$  dummy antenna; all signal levels in RMS at input dummy; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$V_{i(RF)} = 50\text{ dB}\mu\text{V}$ to $120\text{ dB}\mu\text{V}$				
		$f_{AF} = 1\text{ kHz}$ ; $m = 80\%$	-	0.1	0.3	%
		$f_{AF} = 400\text{ Hz}$ ; $m = 80\%$	-	0.1	0.3	%
		$f_{AF} = 100\text{ Hz}$ ; $m = 80\%$	-	0.1	0.5	%
$S_{\text{stat}}$	static selectivity	single signal; $\Delta f_{RF} = 10\text{ kHz}$ ; $f_{\text{tune}} \pm 10\text{ kHz}$	70	-	-	dB
		single signal; $\Delta f_{RF} = 20\text{ kHz}$ ; $f_{\text{tune}} \pm 20\text{ kHz}$	80	-	-	dB
IP3	third-order intercept point	$f_{RF(\text{unw})1} = 40\text{ kHz}$ ; $f_{RF(\text{unw})2} = 80\text{ kHz}$	-	133	-	dB $\mu\text{V}$
		$f_{RF(\text{unw})1} = 300\text{ kHz}$ ; $f_{RF(\text{unw})2} = 600\text{ kHz}$	-	133	-	dB $\mu\text{V}$
IP2	second-order intercept point	$f_{RF(\text{wanted})} = 1400\text{ kHz}$ ; $f_{RF(\text{unw})1} = 600\text{ kHz}$ ; $f_{RF(\text{unw})2} = 800\text{ kHz}$	160	170	-	dB $\mu\text{V}$
$V_o$	output voltage	$m = 30\%$ ; $f_{AF} = 1\text{ kHz}$ ; $V_{RF} = 60\text{ dB}\mu\text{V}$	-	100	-	mV

[1] Only applicable for TEA6853.

## 15. Application information

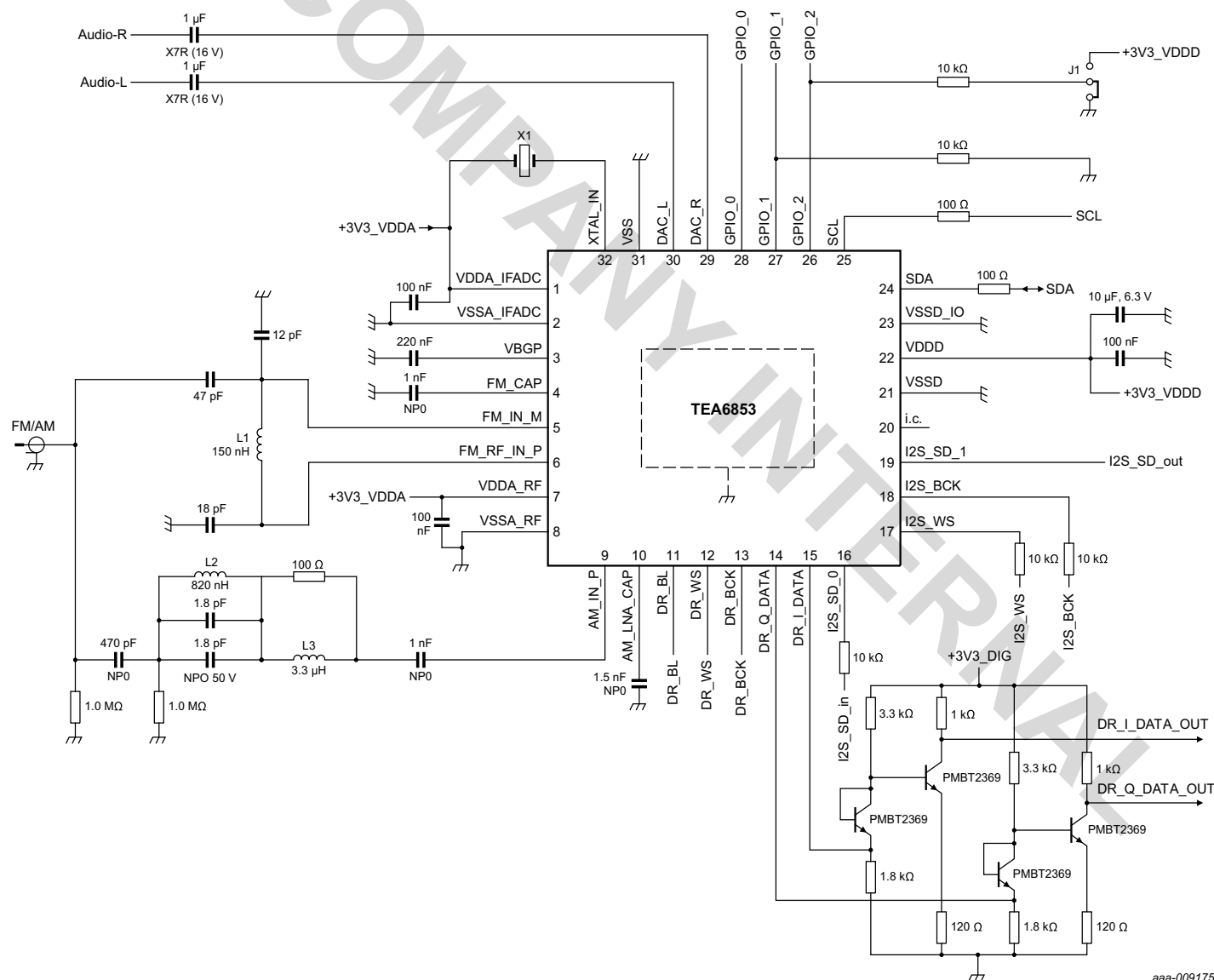
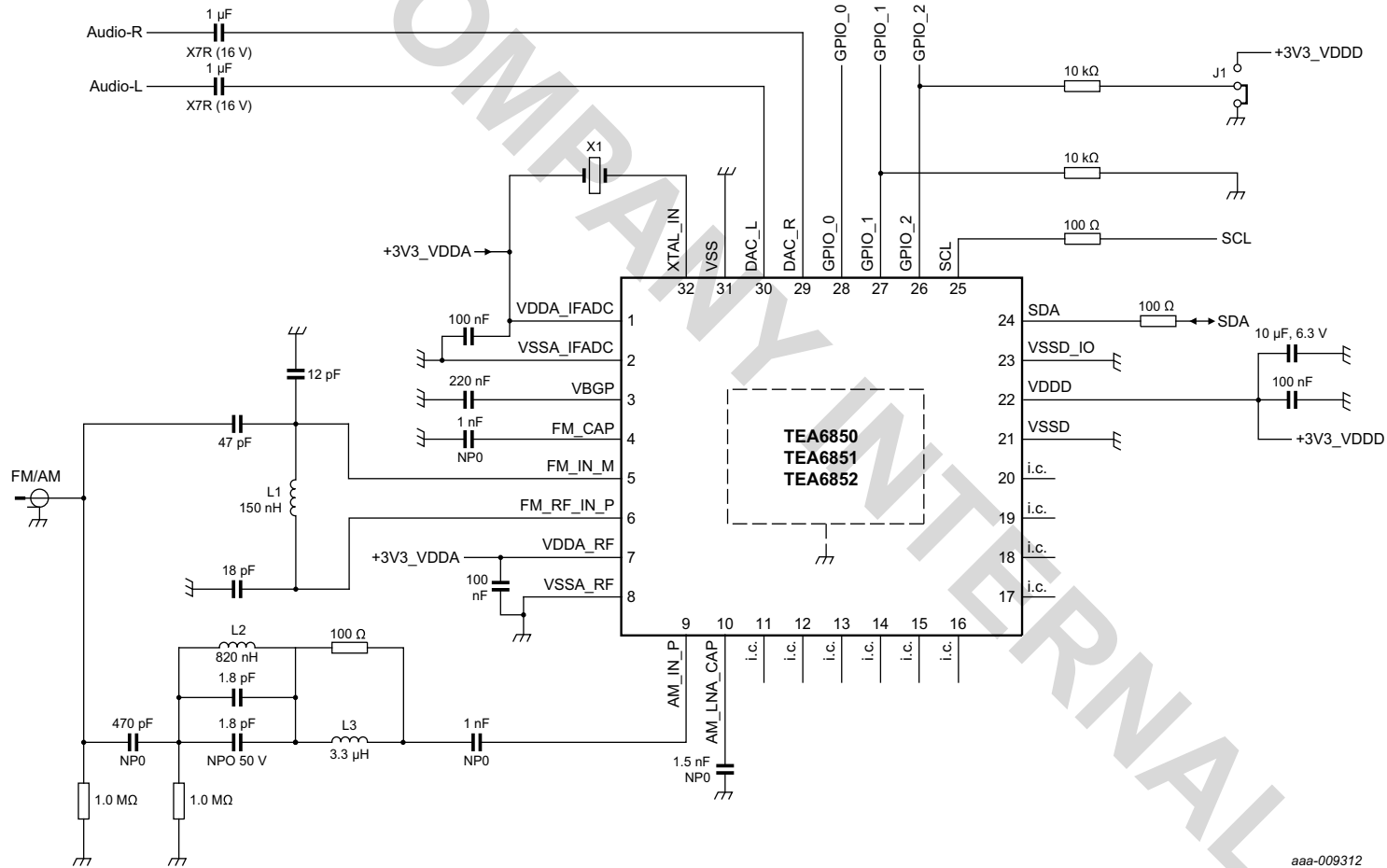


Fig 4. Schematic diagram of TEA6853



aaa-009312

Fig 5. Schematic diagram TEA6850, TEA6851 and TEA6852

## NXP Semiconductors

# TEA685X

### DSP-based radio tuner one-chip

**Table 14. List of components for Figure 4 and Figure 5**

Symbol	Type	Series	Manufacturer
L1	C2012C-R15J-RC	C2012C	Sagami
L2	C2012C-R82J	C2012C	Sagami
L3	LLM2520-3R3K	LLM2520	Toko
X1	DSX530GA (9.216 MHz)	DSX530GA	KDS
	AS04000005 (4.000 MHz)	9B (HC-49S)	TXC
	AT040000xx (4.000 MHz)	9C (HC-49S SMD)	TXC
	AV12000003 (12.000 MHz)	AV	TXC

**Table 15. DC operating points**

$V_{DDA(RF)(3V3)} = 3.3\text{ V}$ ;  $V_{DDA(IF)(3V3)} = 3.3\text{ V}$ ;  $V_{DDD(3V3)} = 3.3\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
I2S_WS <sup>[1]</sup>	17	-	0/3.3	-	-	0/3.3	-
I2S_BCK <sup>[1]</sup>	18	-	0/3.3	-	-	0/3.3	-
I2S_SD_1 <sup>[1]</sup>	19	-	1.1	-	-	1.1	-
i.c.	20	-	0	-	-	-	-
GPIO_0	28	-	0/3.3	-	-	0/3.3	-
VSSA_RF	8	external GND			external GND		
AM_LNA_CAP	10	-	0	-	0.4	0.6	0.8
AM_IN_P	9	-	0	-	-	0.63	-
VSSA_IFADC	2	external GND			external GND		
VDDA_RF	7	external 3.3			external 3.3		
FM_IN_M	5	1.15	1.27	1.45	-	1.54	-
FM_IN_P	6	1.15	1.27	1.45	-	1.54	-
FM_CAP	4	-	1.27	-	-	1.54	-
XTAL_IN	32	-	0.58	-	-	0.58	-
VDDA_IFADC	1	external 3.3			external 3.3		
DAC_R	29	-	0.9	-	-	0.9	-
DAC_L	30	-	0.9	-	-	0.9	-
VSSD	21	external GND			external GND		
SCL	25	0/external I <sup>2</sup> C-bus voltage			0/external I <sup>2</sup> C-bus voltage		
SDA	24	0/external I <sup>2</sup> C-bus voltage			0/external I <sup>2</sup> C-bus voltage		
DR_Q_DATA <sup>[1]</sup>	14	-	0/3.3	-	-	0/3.3	-
DR_BCK <sup>[1]</sup>	13	-	0/3.3	-	-	0/3.3	-
I2S_SD_0 <sup>[1]</sup>	16	-	0/3.3	-	-	0/3.3	-
DR_I_DATA <sup>[1]</sup>	15	-	0/3.3	-	-	0/3.3	-
VDDD	22	external 3.3			external 3.3		
VBGP	3	2.42	2.55	2.67	2.42	2.55	2.67
DR_BL <sup>[1]</sup>	11	-	0/3.3	-	-	0/3.3	-
VSS	31	external GND			external GND		

## NXP Semiconductors

# TEA685X

### DSP-based radio tuner one-chip

**Table 15. DC operating points ...continued**

$V_{DDA(RF)}(3V3) = 3.3\text{ V}$ ;  $V_{DDA(IF)}(3V3) = 3.3\text{ V}$ ;  $V_{DDD}(3V3) = 3.3\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
DR_WS <sup>[1]</sup>	12	-	0/3.3	-	-	0/3.3	-
VSSD_IO	23	external GND			external GND		
GPIO_2	26	-	0/3.3	-	-	0/3.3	-
GPIO_1	27	-	0/3.3	-	-	0/3.3	-

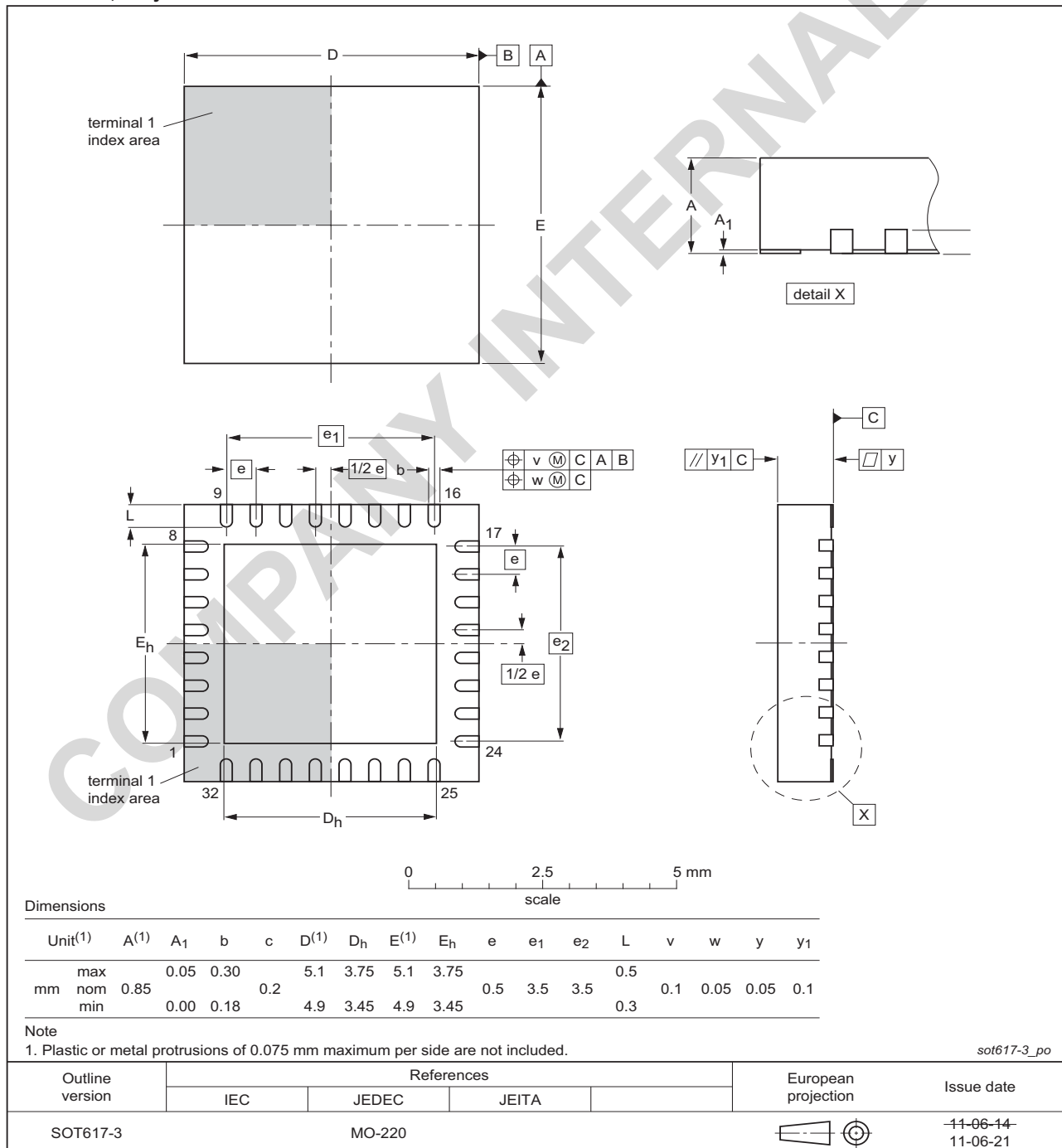
[1] This pin is internally connected for the TEA6850, TEA6851 and TEA6852. The function is only available in TEA6853.

## 16. Package outline

No tracks are permitted on the PCB top layer beneath the pin 1 marker. Refer to [Ref. 6](#) for more detailed information with respect to package and PCB layout guidelines.

**HVQFN32:** plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

**SOT617-3**



**Fig 6. Package outline SOT617-3 (HVQFN32)**

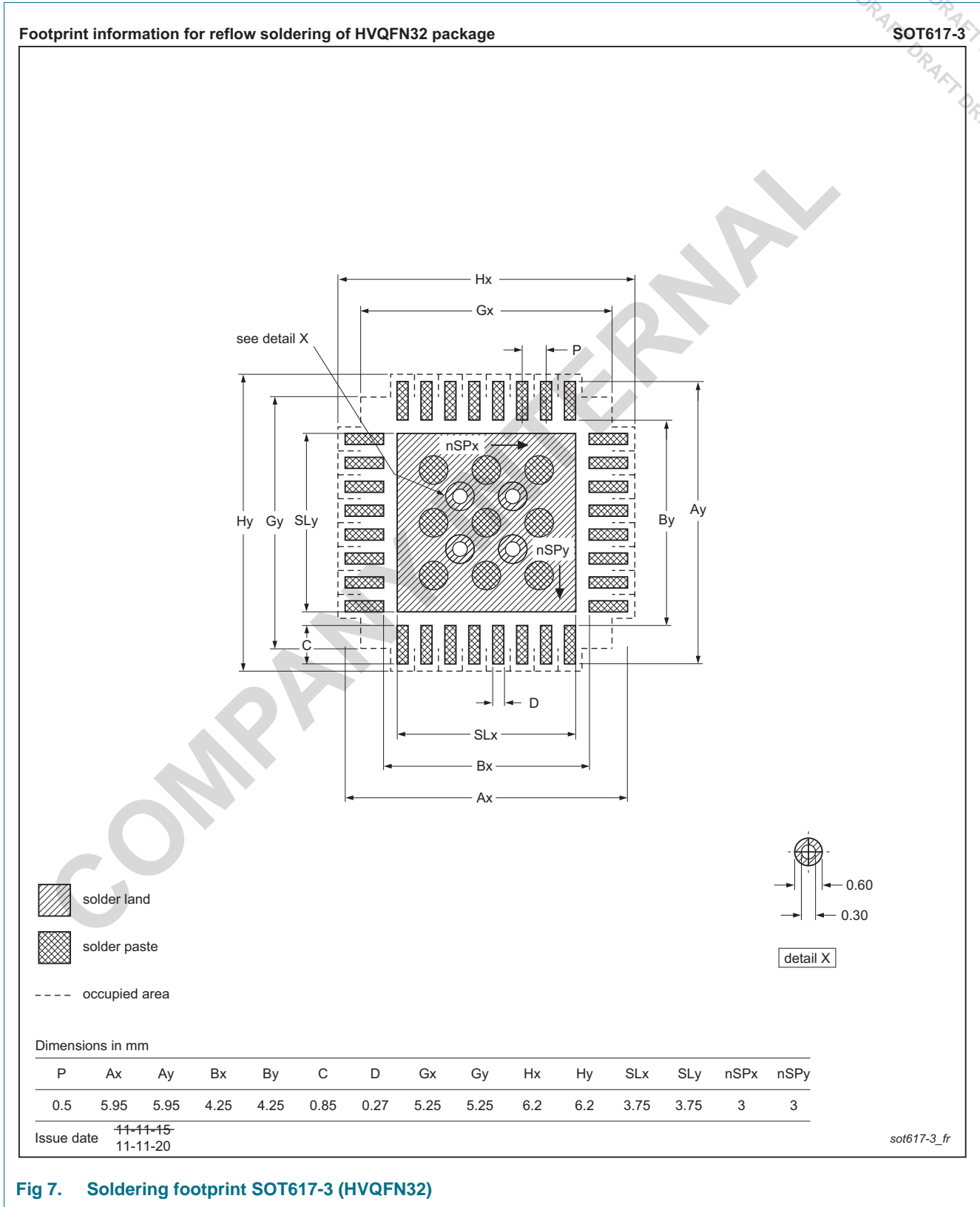


Fig 7. Soldering footprint SOT617-3 (HVQFN32)



## 17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 8](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 16](#) and [17](#)

**Table 16. SnPb eutectic process (from J-STD-020D)**

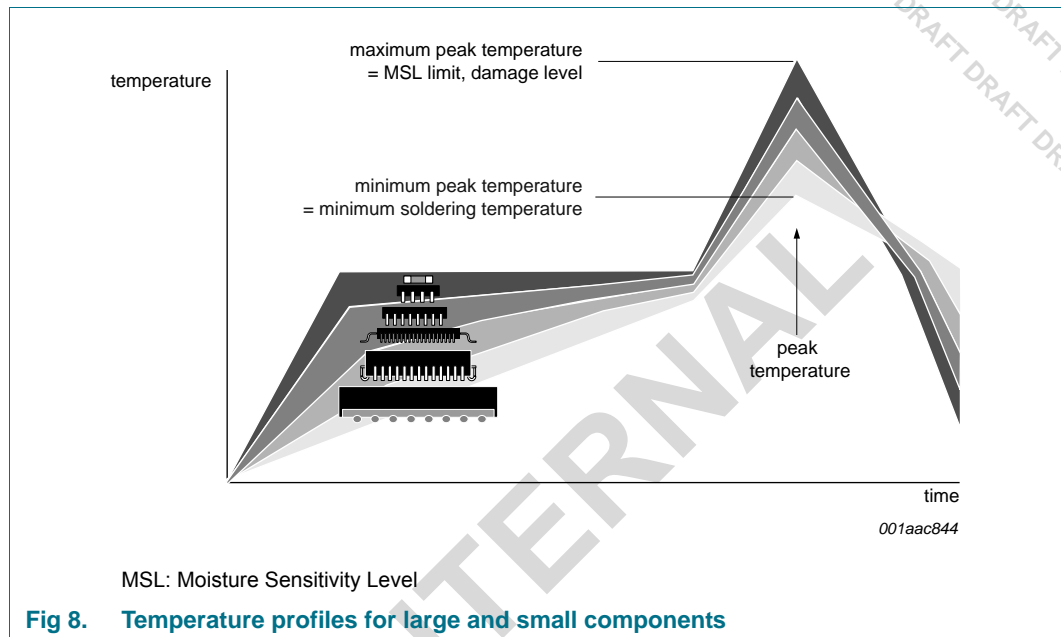
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 17. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 8](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 18. Abbreviations

**Table 18. Abbreviations**

Acronym	Description
AC	Alternating Current
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AM	Amplitude Modulation
BCK	Bit Clock
DAC	Digital-to-Analog Converter
DARC	DAta Radio Channel
DRM	Digital Radio Mondiale
DSP	Digital Signal Processor
ESD	ElectroStatic Discharge
FM	Frequency Modulation
GPIO	General Purpose Input/Output
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter IC bus
I <sup>2</sup> S	Inter IC Sound
IC	Integrated Circuit
IF	Intermediate Frequency
I/O	Input/Output
I/Q	In-phase/Quadrature phase

Table 18. Abbreviations ...continued

Acronym	Description
JEDEC	Joint Electron Device Engineering Council(s)
LNA	Low-Noise Amplifier
LO	Local Oscillator
LW	Long Wave
MPX	FM-Multiplex Signal
MW	Medium Wave
OIRT	International Radio and Television Organisation (Organisation Internationale de Radiodiffusion et de Télévision)
PACS	Precision Adjacent Channel Suppression
PCB	Printed-Circuit Board
PI	Program Identification
PLL	Phase-Locked Loop
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RMS	Root-Mean-Square
RSSI	Received Signal Strength Indicator
SNR	Signal-to-Noise Ratio
SW	Short Wave
US	United States of America
USN	UltraSonic Noise
WAM	Wideband AM
WS	Word Select

## 19. Glossary

**HD Radio™** — Technology upgrades broadcast radio from analog to digital

## 20. References

- [1] **UM10204; I<sup>2</sup>C-bus specification and user manual - v.5** — Official I<sup>2</sup>C Standard Document (available from NXP Semiconductors, International Marketing and Sales)
- [2] **IEC 60134** — Absolute Maximum Rating System
- [3] **JESD22-A114** — JEDEC Standard - Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [4] **JESD22-C101** — JEDEC Standard - Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [5] **Application note AN10365** — Surface mount reflow soldering description
- [6] **Application note <tbid>** — TEA685X Application Note
- [7] **TEA685X User Manual** — Technical information

## 21. Revision history

**Table 19. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA685X v.1	<tbid>	Preliminary data sheet	-	-

## 22. Legal information

### 22.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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# TEA685X

### DSP-based radio tuner one-chip

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## 24. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	<b>22</b>	<b>Legal information</b> . . . . .	<b>30</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>	22.1	Data sheet status . . . . .	30
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>	22.2	Definitions . . . . .	30
<b>4</b>	<b>Functionality</b> . . . . .	<b>3</b>	22.3	Disclaimers . . . . .	30
<b>5</b>	<b>Ordering information</b> . . . . .	<b>3</b>	22.4	Trademarks . . . . .	31
<b>6</b>	<b>Block diagram</b> . . . . .	<b>4</b>	<b>23</b>	<b>Contact information</b> . . . . .	<b>31</b>
<b>7</b>	<b>Pinning information</b> . . . . .	<b>5</b>	<b>24</b>	<b>Contents</b> . . . . .	<b>32</b>
7.1	Pin description . . . . .	6			
<b>8</b>	<b>Functional description</b> . . . . .	<b>7</b>			
8.1	FM front-end to IF ADC input . . . . .	7			
8.2	AM front-end to IF ADC input . . . . .	8			
8.3	Tuning system . . . . .	8			
8.4	IF ADC . . . . .	8			
8.5	Radio processing . . . . .	8			
8.5.1	AM mode features . . . . .	9			
8.5.2	FM mode features . . . . .	9			
8.5.3	RDS/RBDS . . . . .	10			
8.5.3.1	RDS demodulator . . . . .	10			
8.5.3.2	RDS decoder . . . . .	10			
8.5.4	Digital radio interface . . . . .	10			
8.6	Audio input . . . . .	10			
8.7	Audio processing . . . . .	10			
8.8	Audio output . . . . .	10			
8.9	Crystal oscillator . . . . .	11			
8.10	I <sup>2</sup> C-bus interface . . . . .	11			
<b>9</b>	<b>I<sup>2</sup>C-bus protocol</b> . . . . .	<b>11</b>			
9.1	Write mode . . . . .	11			
9.2	Read mode . . . . .	11			
<b>10</b>	<b>Overview of commands</b> . . . . .	<b>12</b>			
<b>11</b>	<b>Limiting values</b> . . . . .	<b>14</b>			
<b>12</b>	<b>Thermal characteristics</b> . . . . .	<b>14</b>			
<b>13</b>	<b>Static characteristics</b> . . . . .	<b>15</b>			
<b>14</b>	<b>Dynamic characteristics</b> . . . . .	<b>15</b>			
<b>15</b>	<b>Application information</b> . . . . .	<b>19</b>			
<b>16</b>	<b>Package outline</b> . . . . .	<b>23</b>			
<b>17</b>	<b>Soldering of SMD packages</b> . . . . .	<b>25</b>			
17.1	Introduction to soldering . . . . .	25			
17.2	Wave and reflow soldering . . . . .	25			
17.3	Wave soldering . . . . .	25			
17.4	Reflow soldering . . . . .	26			
<b>18</b>	<b>Abbreviations</b> . . . . .	<b>27</b>			
<b>19</b>	<b>Glossary</b> . . . . .	<b>28</b>			
<b>20</b>	<b>References</b> . . . . .	<b>29</b>			
<b>21</b>	<b>Revision history</b> . . . . .	<b>29</b>			

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