P-Channel Enhancement Mode Power MOSFET TDM4953

DESCRIPTION

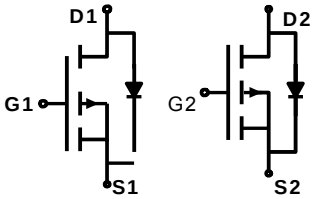
The TDM4953 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

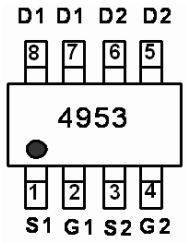
- V_{DS} = -30V,I_D = -5.1A
  $R_{DS(ON)}$ < 85mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ < 53mΩ @ V_{GS}=-10V
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package

Application

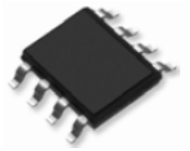
- PWM applications
- Load switch
- Power management



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TDM4953	TDM4953	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-5.1	A
Drain Current-Pulsed (Note 1)	I_{DM}	-20	A
Maximum Power Dissipation	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	℃/W

Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	μA

Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1		-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5.1A			53	mΩ
		V_{GS}=-4.5V, I_D=-4.2A			85	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-15V,I_D=-4.5A	4	7		S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz		1040		PF
Output Capacitance	C_{oss}			420		PF
Reverse Transfer Capacitance	C_{rss}			150		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V, ID=-1A, V_{GS}=-10V,R_{GEN}=6Ω		15		nS
Turn-on Rise Time	t_r			13		nS
Turn-Off Delay Time	$t_{d(off)}$			58		nS
Turn-Off Fall Time	t_f			21		nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-5.1A,V_{GS}=-10V		12		nC
Gate-Source Charge	Q_{gs}			2.2		nC
Gate-Drain Charge	Q_{gd}			3		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-1.7A			-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

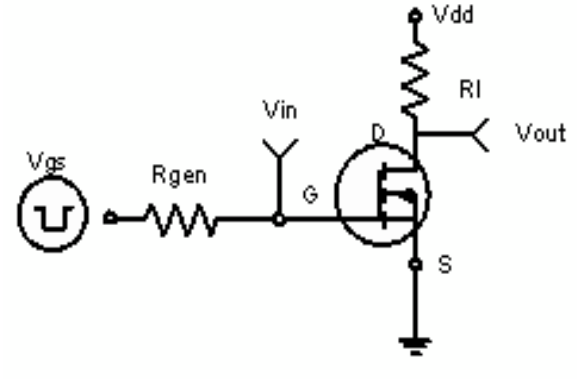


Figure 1:Switching Test Circuit

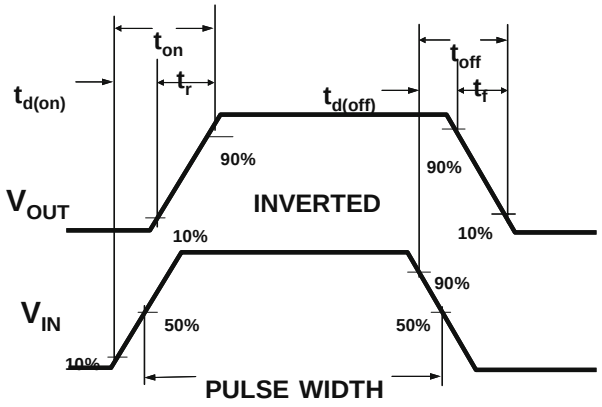


Figure 2:Switching Waveforms

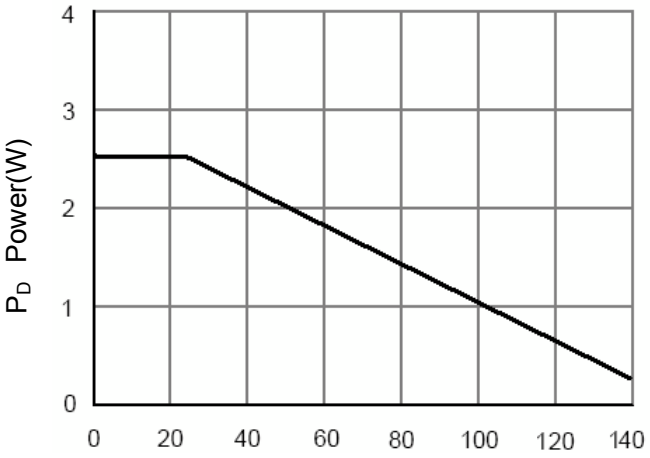


Figure 3 Power Dissipation

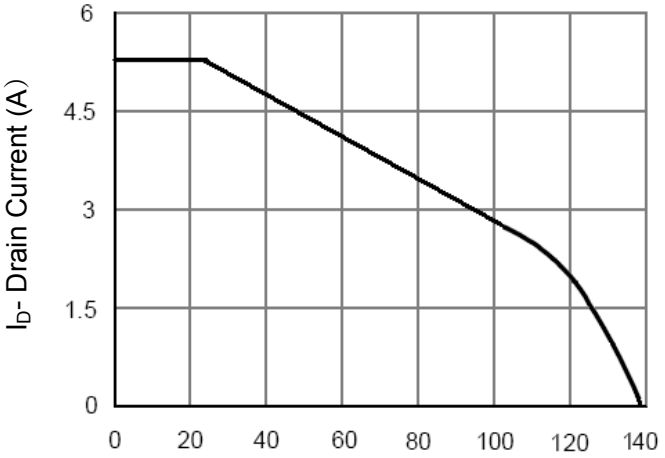


Figure 4 Drain Current

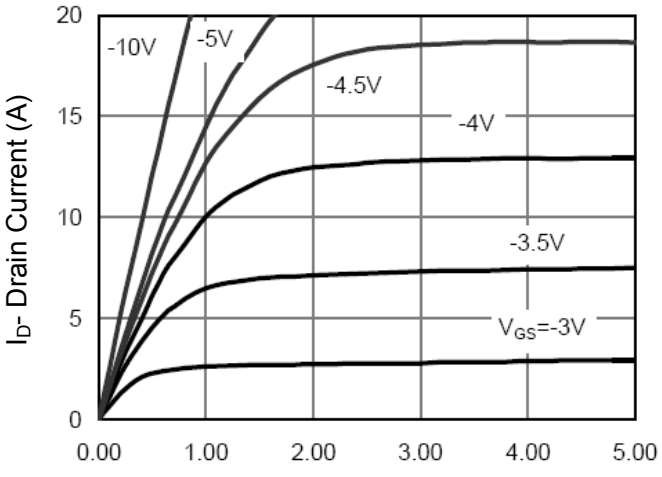


Figure 5 Output CHARACTERISTICS

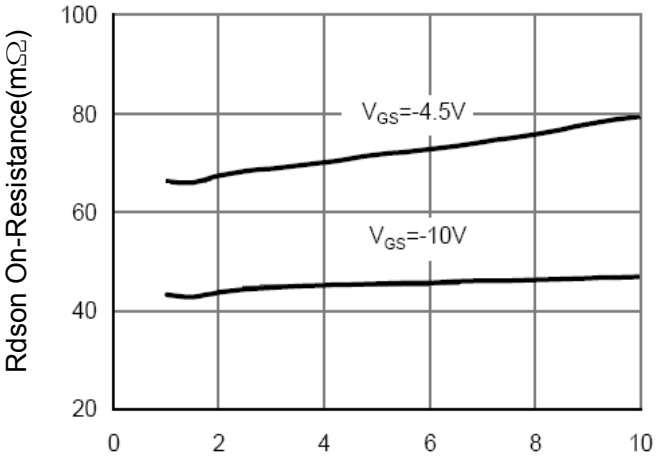


Figure 6 Drain-Source On-Resistance

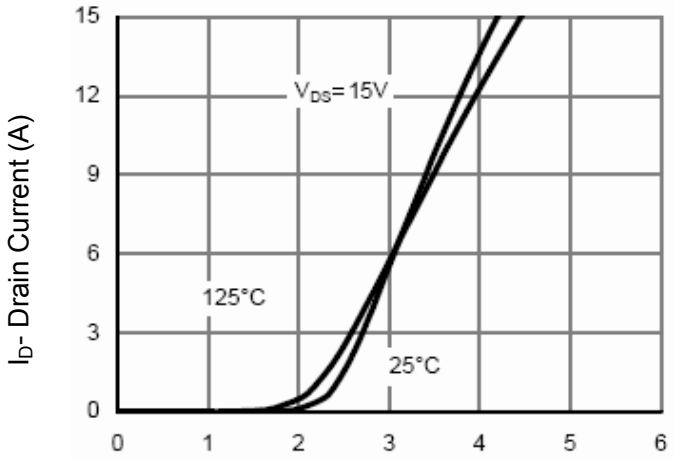


Figure 7 Transfer Characteristics

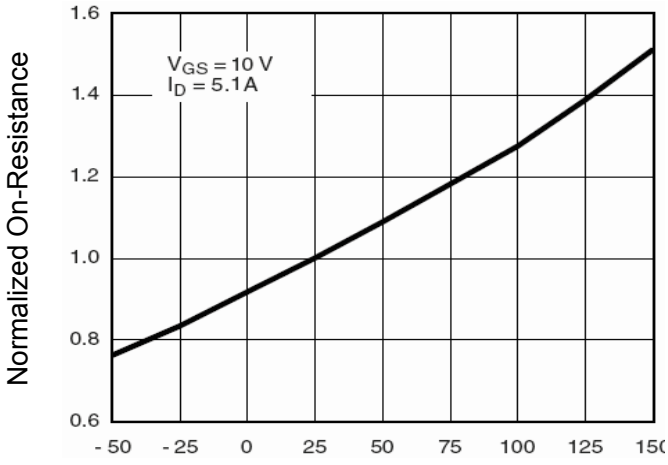


Figure 8 Drain-Source On-Resistance

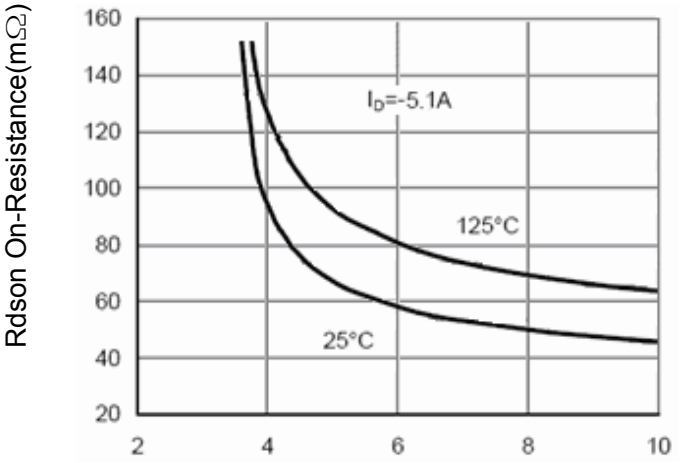


Figure 9 Rdson vs Vgs

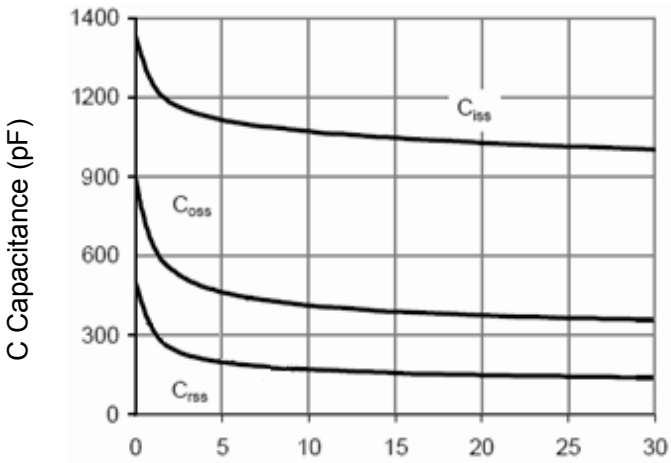


Figure 10 Capacitance vs Vds

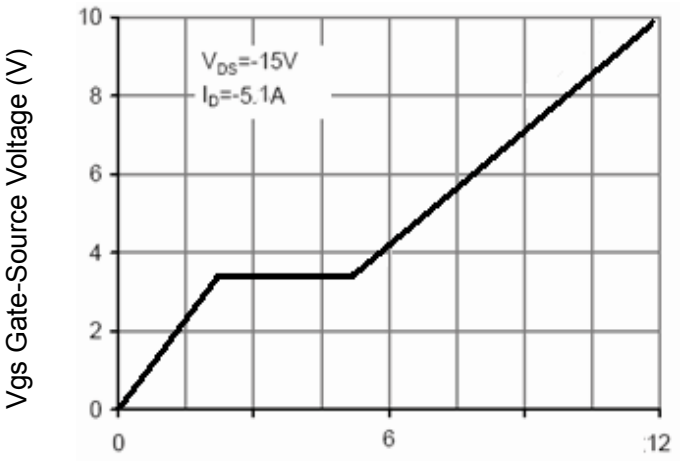


Figure 11 Gate Charge

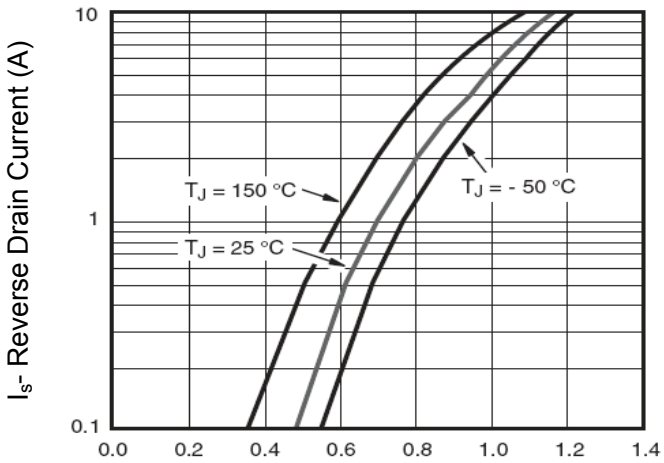


Figure 12 Source- Drain Diode Forward

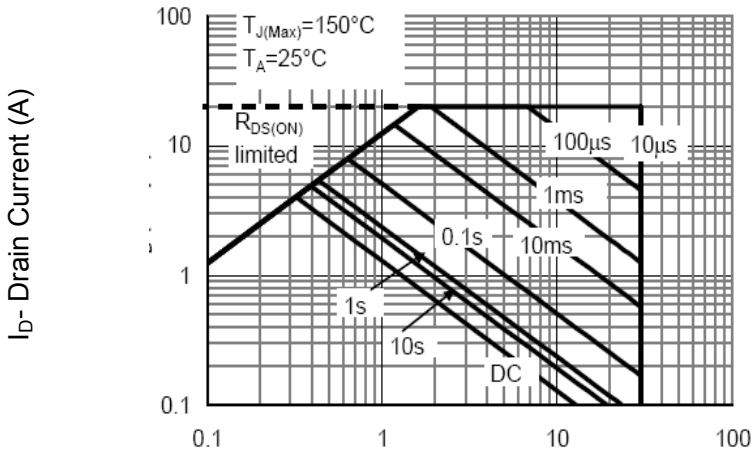


Figure 13 Safe Operation Area

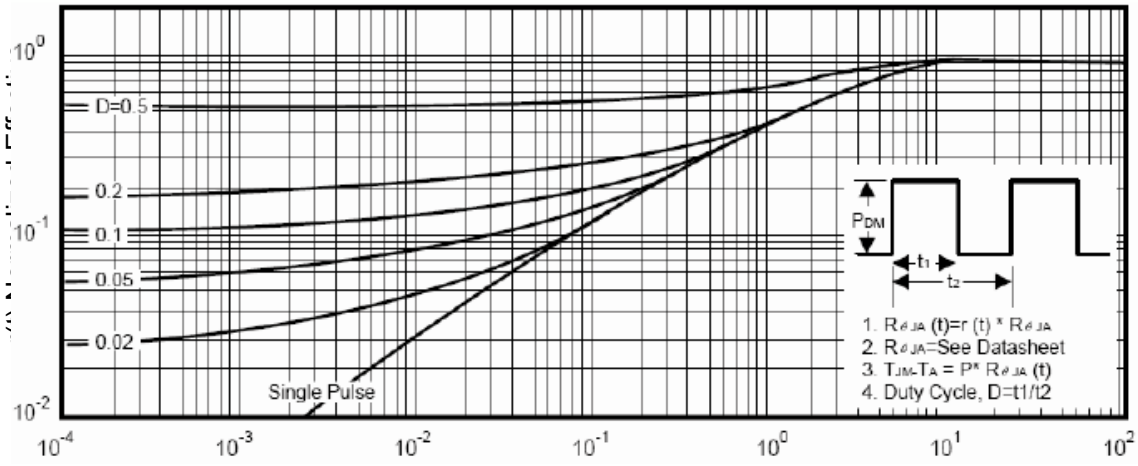


Figure 14 Normalized Maximum Transient Thermal Impedance