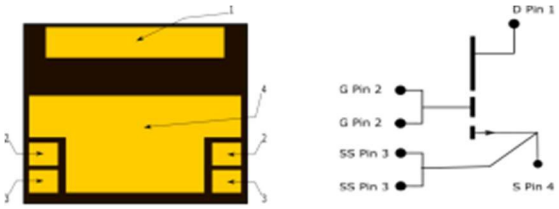
TDG650E60
Bottom- or Top-side Cooled 650 V E-mode GaN FET

Product Specification April 2020

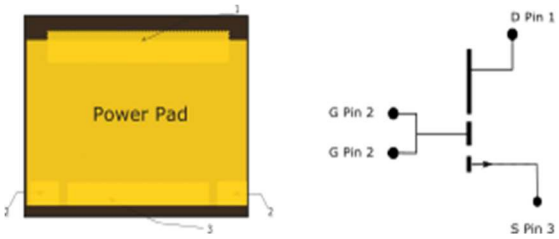
Features

- 650 V enhancement mode power switch with P-GaN gate structure
- Bottom- or Top-side cooled configuration
- RDS(on) = 25 mΩ (typ)
- IDS(max) = 60 A
- Ultra-low FOM Island Technology® die
- Ultra-low inductance GaNPX® package
- Easy gate drive requirements (0 V to 6 V) with 7V tolerance
- Transient tolerant gate drive (-20 / +10 V) 1µs
- Very high switching frequency (> 10 MHz)
- Reverse current capability
- Zero reverse recovery loss
- Small 11 x 9 mm2 PCB footprint
- Source Sense (SS) pads for optimized gate drive
- Dual gate and source sense pads for optimal board layout
- RoHS compliant
- Single diffusion lot available
- Enhanced wafer level reliability
- HiRel qualification flow
- Obsolescence support

TDG650E60B: Bottom Side cooled



TDG650E60T: Top Side cooled



Applications

- High efficiency power conversion
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half & Full Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- dc-dc Converters
- On Board Battery Chargers
- E-Switch

Description

Teledyne's TDG650E60 is an enhancement mode GaN-on-silicon power transistor based on GaN Systems Technology. The properties of GaN ensure high current, high voltage breakdown combined with very high switching frequency. GaN Systems implements patented **Island Technology®** cell layout for high-current performance and excellent thermal characteristics. GaNPX® packaging is designed for very low parasitic inductance in a smallest package. The TDG650E60 is alternatively a Bottom- or Top-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combined provide very high efficiency power switching.

Table 1 : Absolute Maximum Ratings (Tcase = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Transient Drain-to-Source Voltage[1]	V_{DS}(trans)	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Step Stress Gate-to-Source Voltage (Tj=175°C,12h) [2]	$STSV_{gs}$	8	V
Gate-to-Source Voltage - transient [1]	$V_{GS(trans)}$	-20 to +10	V
Continuous Drain Current (T_{case}=25 °C) [3]	I_{DS}	60	A
Continuous Drain Current (T_{case}=100 °C) [3]	I_{DS}	47	A
Pulse Drain Current (Pulse width 100 µs)	$I_{DS\ Pulse}$	120	A

[1] Pulse < 1 µs.
[2]Please contact Teledyne for additional Information regarding Step Stress
[3] Pulse Limited by saturation

Table 2 . Thermal Characteristics (Typical values unless otherwise noted)

Parameter for Bottom-side Cooled Package	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.27	°C /W
Thermal Resistance (junction-to-top)	$R_{\Theta JT}$	5.5	°C /W
Thermal Resistance (junction-to-ambient) [4]	$R_{\Theta JA}$	23	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C
Parameter for Top-side Cooled Package	**Symbol**	**Value**	**Units**
Thermal Resistance (junction-to-case) – top side	$R_{\Theta JC}$	0.3	°C /W
Thermal Resistance (junction-to-board)	$R_{\Theta JB}$	3.0	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

[4] Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal via under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Table 3 : Ordering Information

Ordering code	Package type	Packing method	Qty	Part Marking	Origin	ECCN
TDG650E60BEP	GaN*PX*® Bottom-side Cooled	Mini-Reel	250	TDG660BE	US	EAR99
TDG650E60BEPF	GaN*PX*® Bottom-side Cooled	Mini-Reel	250	TDG660BF	EU	EU
TDG650E60TEP	GaN*PX*® Top-side Cooled	Mini-Reel	250	T60TE	US	EAR99
TDG650E60TEPF	GaN*PX*® Top-side Cooled	Mini-Reel	250	T60TF	EU	EU

Table 4: Electrical Characteristics.

Typical values at TJ = 25 °C, VGS = 6 V. Unless otherwise noted, Min/Max values are specified over the full temperature range from TJ = -55 °C to TJ = 150 °C based on Teledyne Dynamic Burn-In[5] after 15k Cycles.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	V_{DS}	650			V	V_{GS} = 0 V, I_{DSS} = 100 µA, Tj=25C
Drain-to-Source On Resistance	$R_{DS(on)}$	11	25	60	mΩ	V_{GS} = 6 V I_{DS} = 18 A
Dynamic Drain-to-Source On Resistance Shift	$DR_{DS(on)}$		19		%	V_{GS} = 6 V I_{DS} = 18 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 14 mA
Gate-to-Source Current	I_{GS}	0.031	0.320	12	mA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3.0		V	V_{DS} = 400 V, I_{DS} = 60 A
Drain-to-Source Leakage Current	I_{DSS}	1.2	4	80	µA	V_{DS} = 650 V, V_{GS} = 0 V
Internal Gate Resistance	R_G		0.34		Ω	f = 25 MHz, open drain
Input Capacitance	C_{ISS}		518		pF	V_{DS} = 400 V, V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		126		pF	
Reverse Transfer Capacitance	C_{RSS}		5.9		pF	
Effective Output Capacitance Energy Related [6]	$C_{O(ER)}$		207		pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective Output Capacitance Time Related [7](note 5)	$C_{O(TR)}$		335		pF	
Total Gate Charge	Q_G		14.2		nC	V_{GS} = 0 to 6 V, V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		3.8		nC	

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Gate-to-Drain Charge	Q_{GD}		5.4		nC	
Output Charge	Q_{OSS}		134		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	
Turn-On Delay	tD(on)		4.6		ns	V_{DD}= 400 V V_{GS} = 0 - 6 V I_D = 16 A, $R_{G(ext)}$= 5 Ω T_J= 25 °C [8]
Rise Time	t_R		12.4		ns	
Turn-Off Delay	$t_{D(off)}$		14.9		ns	
Fall Time	t_F		22		ns	
Output Capacitance Stored Energy	E_{OSS}		17		µJ	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz
Switching Energy during turn-on	E_{on}		134		µJ	V_{DS} = 400 V, I_{DS} = 20 A V_{GS} = 0-6 V, $R_{G(on)}$ = 10 Ω $R_{G(off)}$ = 1 Ω L = 120 µH L_P = 2\ nH [9] [10]
Switching Energy during turn-off	E_{off}		17		µJ	

NOTES

[5] For more details over the dynamic Burn in please contact Teledyne

[6] $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

[7] $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

[8] See Figure 21 for timing test circuit diagram and definition waveforms

[9] L_P is the switching circuit parasitic inductance

[10] See Figure 22 for switching test circuit

Electrical Performance

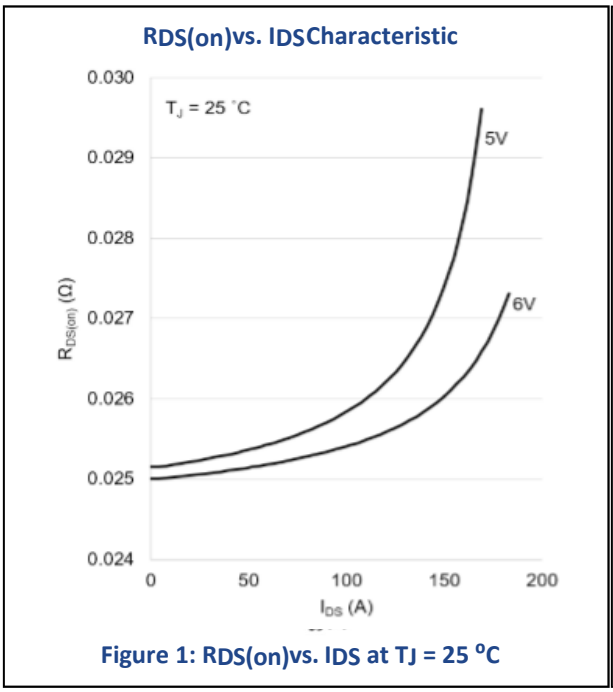


Figure 1: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

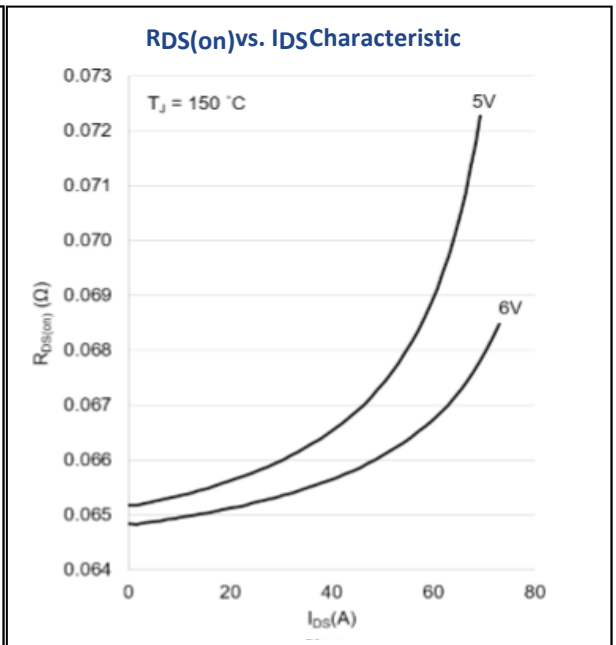


Figure 2: $R_{DS(on)}$ vs. I_{DS} at T_J = 150°C

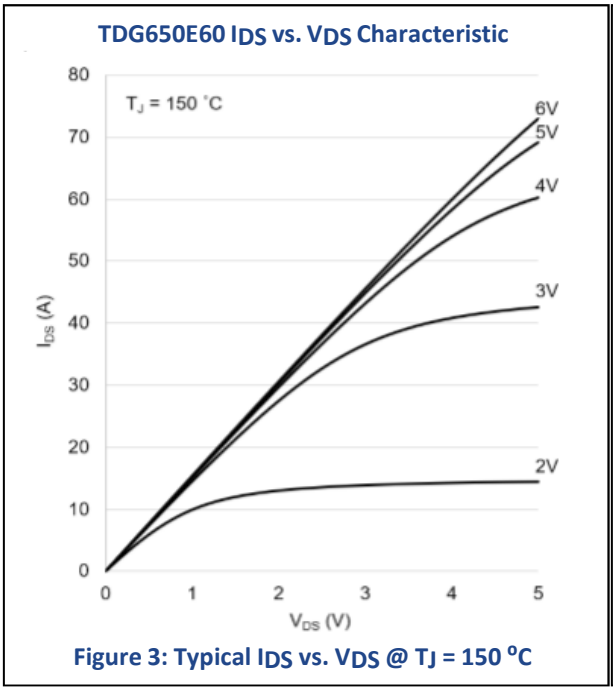


Figure 3: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

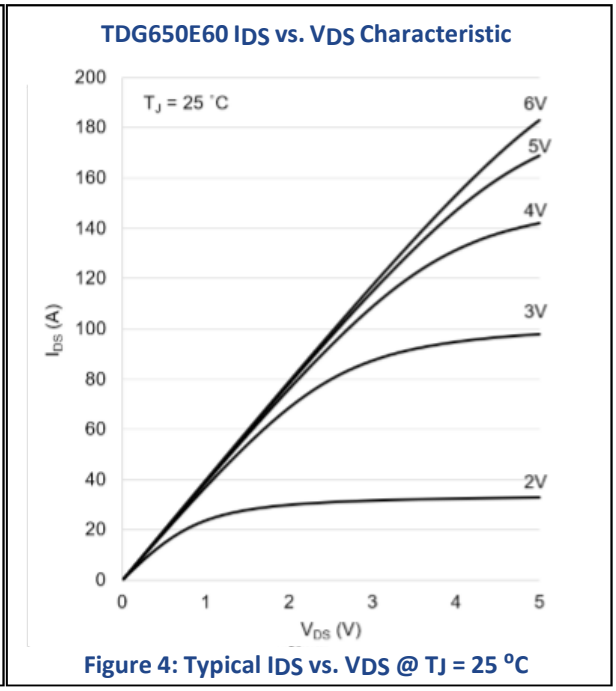


Figure 4: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

Electrical Performance

TDG650E60 I_{DS} vs. V_{DS}, T_J dependence

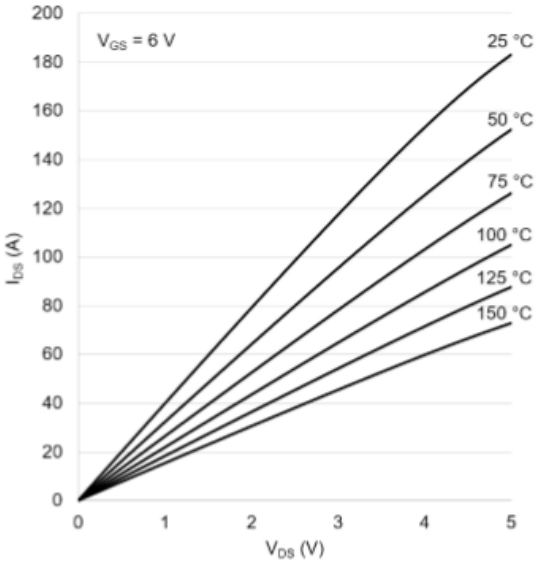


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

TDG650E60 Gate Charge, Q_G Characteristic

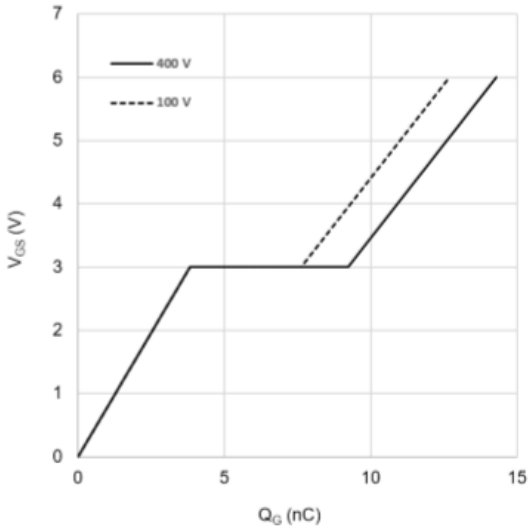


Figure 6: Typical V_{GS} vs. Q_G V_{DS} = 100, 400 V

TDG650E60 Capacitance Characteristics

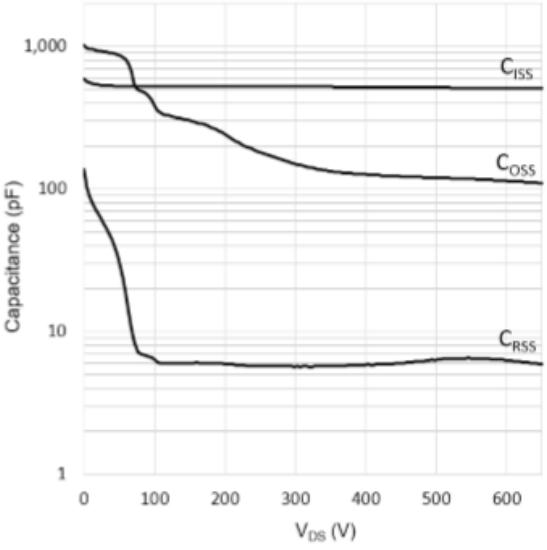


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

TDG650E60 Stored Energy Characteristic

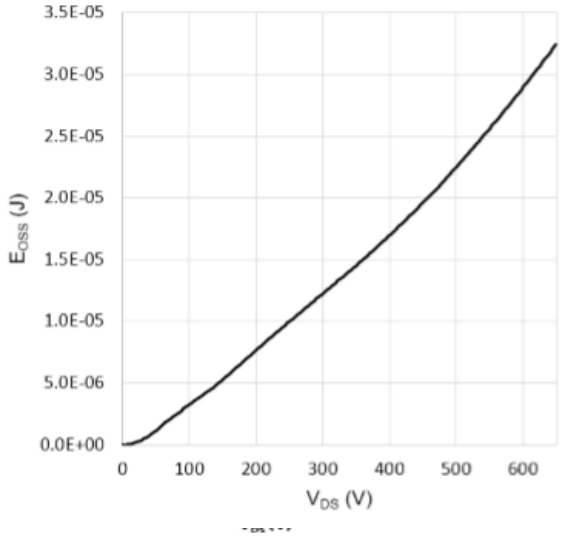


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance

TDG650E60 Reverse Conduction Characteristics

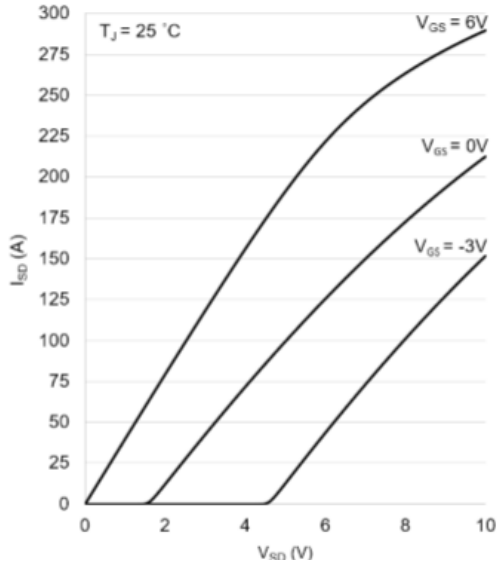


Figure 9: Typical ISD vs. VSD; TJ = 25°C

TDG650E60 Reverse Conduction Characteristics

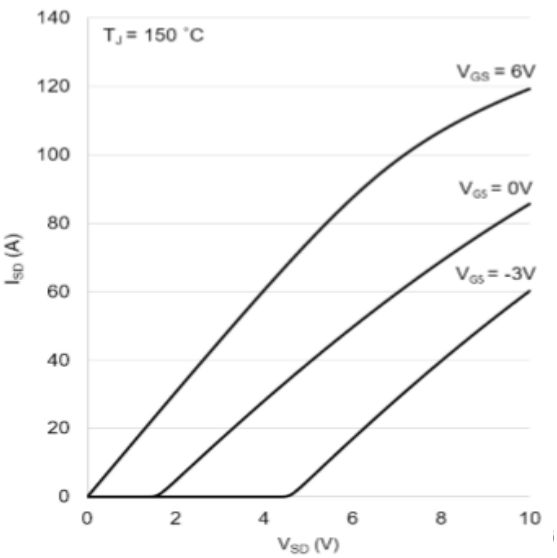


Figure 9a: Typical ISD vs. VSD; TJ = 150°C

TDG650E60 IDS vs. VGS Characteristic

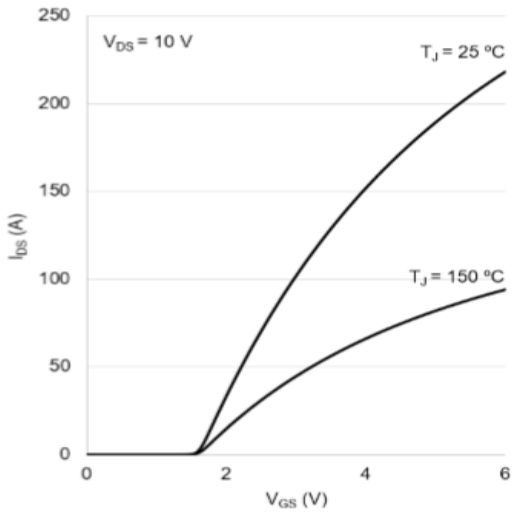


Figure 10: Typical IDS vs. VGS

RDS(on)Temperature Dependence

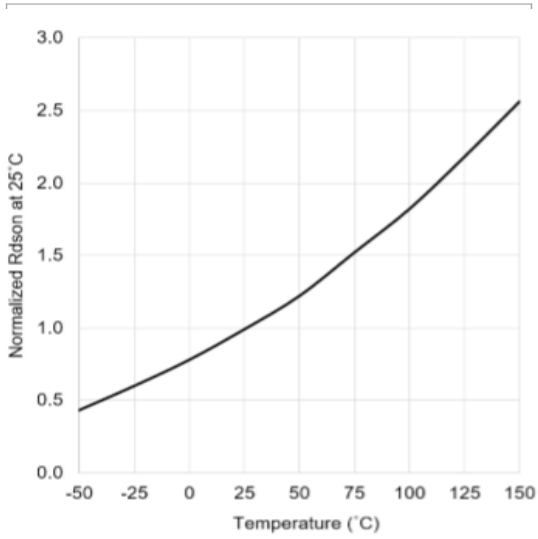


Figure 11: Normalized RDS(on as function of TJ

Electrical Performance

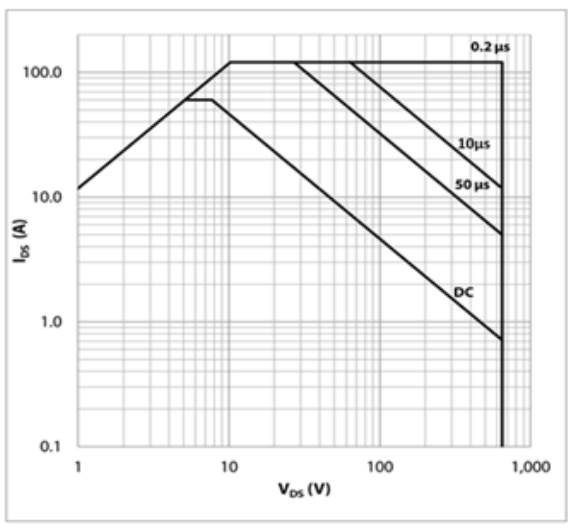


Figure 12: Safe Operating Area T_{case} = 25 ^{0}C

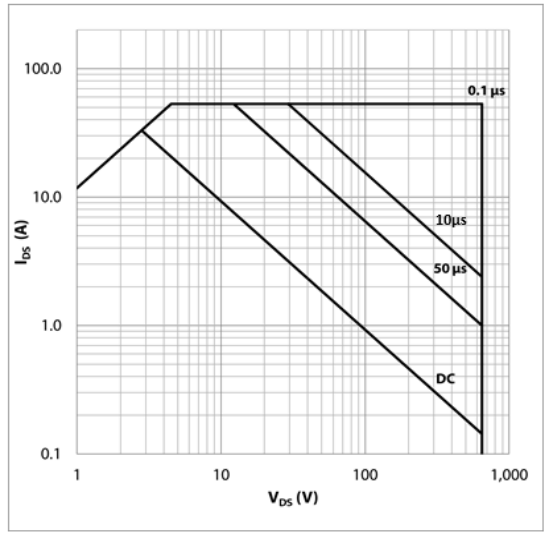


Figure 12a: Safe Operating Area T_{case} = 125 ^{0}C

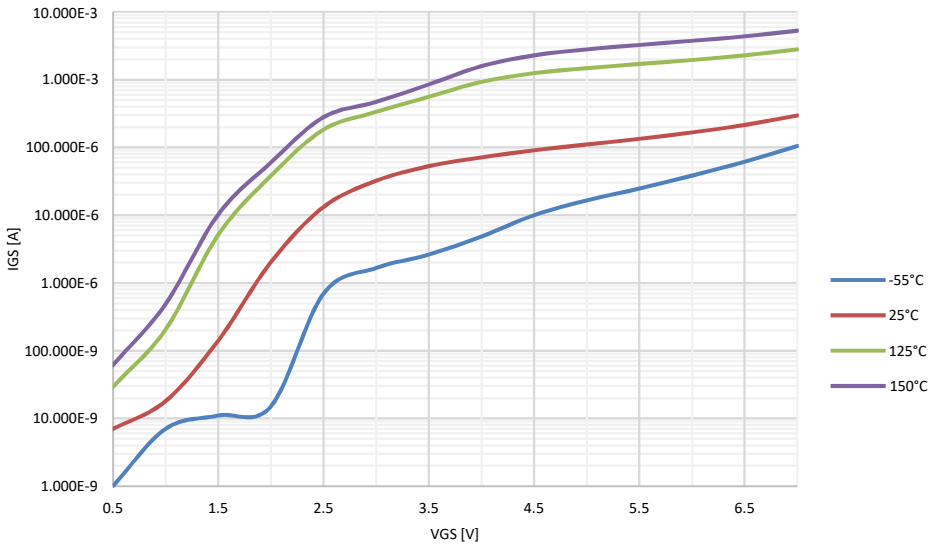


Figure 13: IGS vs VGS (log scale)- Typical values

Electrical Performance

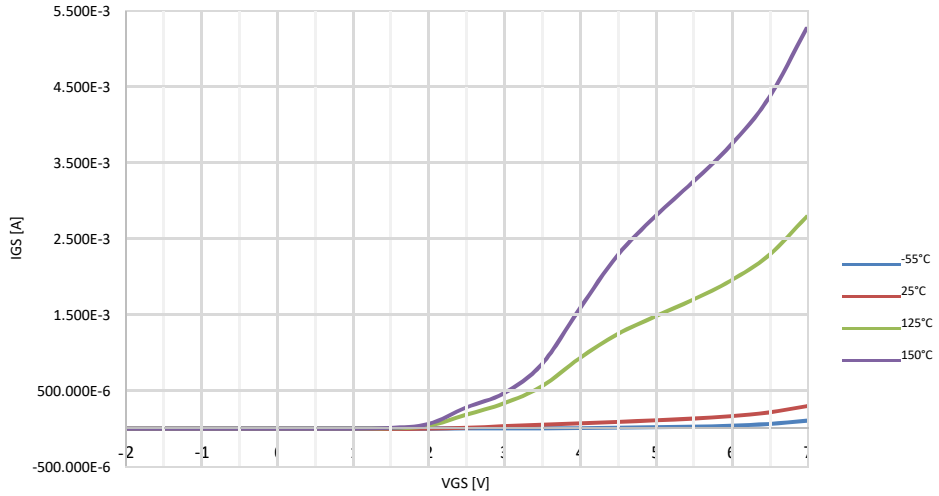


Figure 14: IGS vs VGS - Typical values

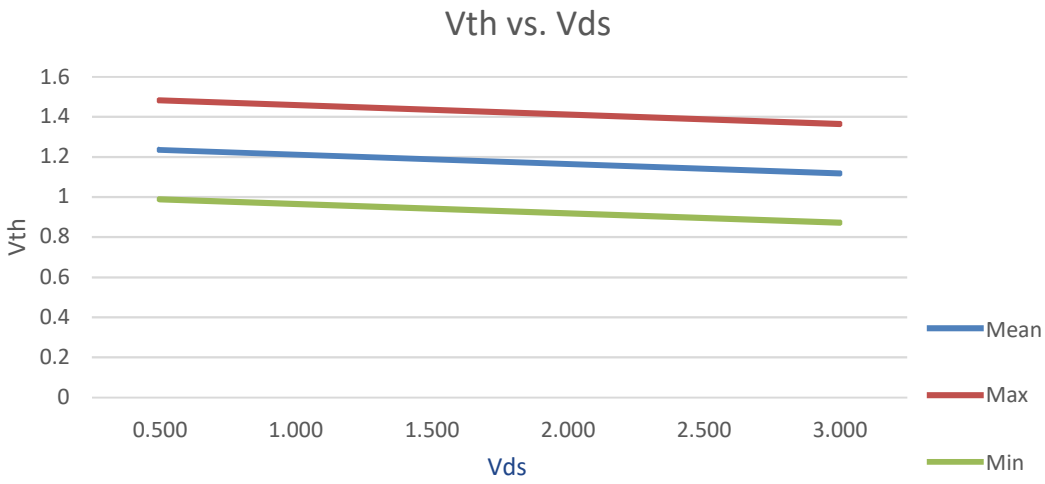


Figure 15: Vth vs. Vds at low Vds voltages

Thermal Performance Graphs

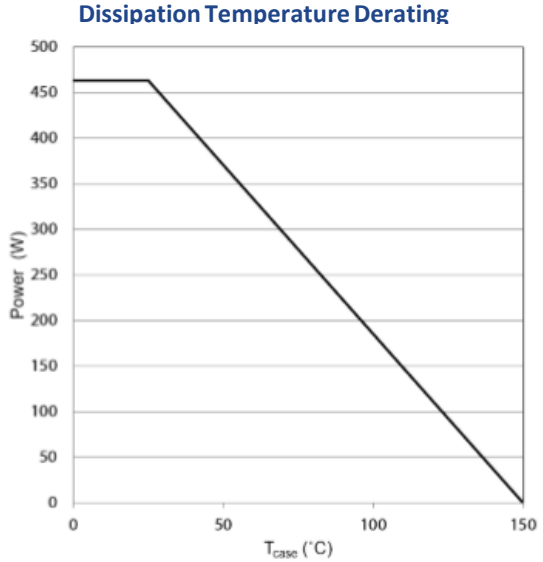


Figure 16 Derating vs. Case Temperature

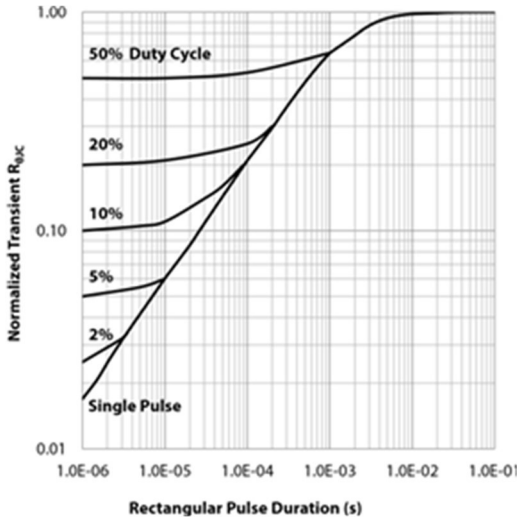


Figure 17: Transient Thermal Impedance
1.00 = Nominal DC thermal impedance

Test Circuits

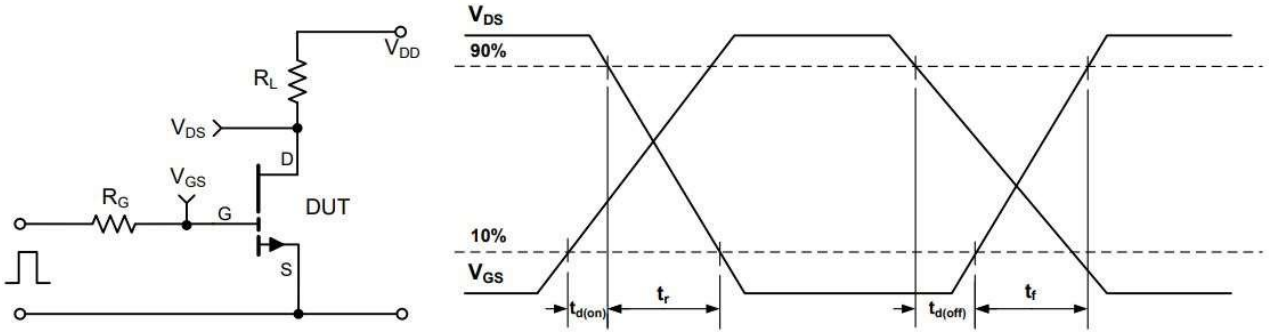


Figure 21: TDG650E60 switching time test circuit and waveforms

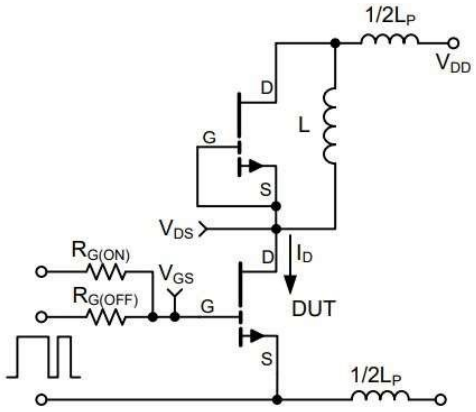


Figure 22: TDG650E60 Switching Loss Test Circuit

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. At 6 V gate drive voltage the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT does not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate; however, it increases the reverse conduction loss.

Similar to silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under- voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight enough tolerance on the gate voltage. Therefore, special care should be taken when you select and use half bridge drivers. Please see the gate driver application note, (GN001), for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.
GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance, which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very high speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate's parasitic oscillation.

Source Sensing

The TDG650E60 has two dedicated source sense pads. The GaN*PX*® packaging utilizes no wire bonds so

the source connection is very low inductance. The dedicated source sense pin will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved by connecting the gate drive signal from the driver to the gate pad on the TDG650E60 and returning from the source sense pad on the TDG650E60 to the driver ground reference.

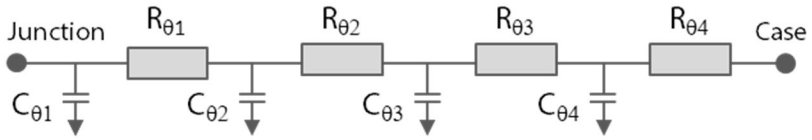
Thermal

The substrate is internally connected to the source and thermal pad on the bottom or the top side of the TDG650E60. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under the Drain pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

TDG650E60 RC thermal model:



TDG650E60B RC Breakdown of RΘJC		TDG650E60T RC Breakdown of RΘJC	
R_θ (°C/W)	C_θ (W·s/°C)	R_θ (°C/W)	C_θ (W·s/°C)
$R_{\Theta 1}$ = 0.008	$C_{\Theta 1}$ = 1.48E-04	$R_{\Theta 1}$ = 0.01	$C_{\Theta 1}$ = 1.4E-04
$R_{\Theta 2}$ = 0.124	$C_{\Theta 2}$ = 1.37E-03	$R_{\Theta 2}$ = 0.14	$C_{\Theta 2}$ = 1.23E-03
$R_{\Theta 3}$ = 0.130	$C_{\Theta 3}$ = 12.0E-03	$R_{\Theta 3}$ = 0.14	$C_{\Theta 3}$ = 10.8E-03
$R_{\Theta 4}$ = 0.008	$C_{\Theta 4}$ = 3.7E-03	$R_{\Theta 4}$ = 0.01	$C_{\Theta 4}$ = 3.7E-03

For more detail, please refer to Application Note GN007 “Modeling Thermal Behavior of GaN Systems’ GaN*PX*™ Using RC Thermal SPICE Models” available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse

recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750 V for 1 µs is acceptable.

Packaging and Soldering

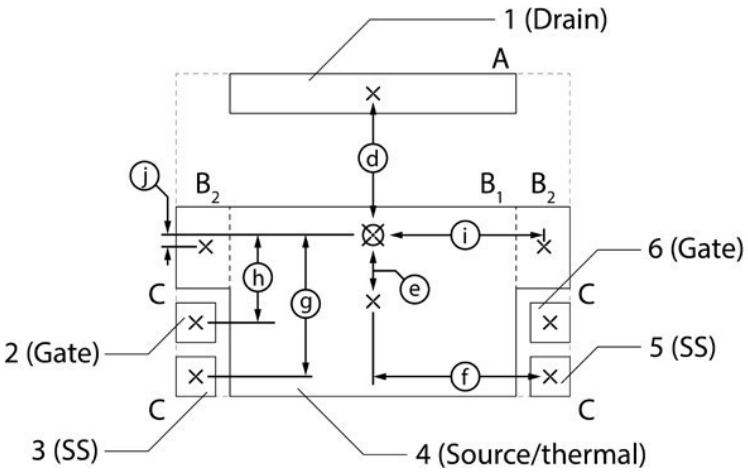
The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the TDG650E60 device to be specified to 150 °C. The device can handle at least 3 reflow cycles.
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1

(March 2008) The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °Cof peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non- Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "Non-Clean" paste residues. For more details, please refer to the soldering application note "GN011-Soldering-Recommendations- for-GaNPX®-Packaged-Devices" at www.gansystems.com

Bottom-side Cooled Recommended Minimum Footprint for Printed Circuit Board



Pad sizes

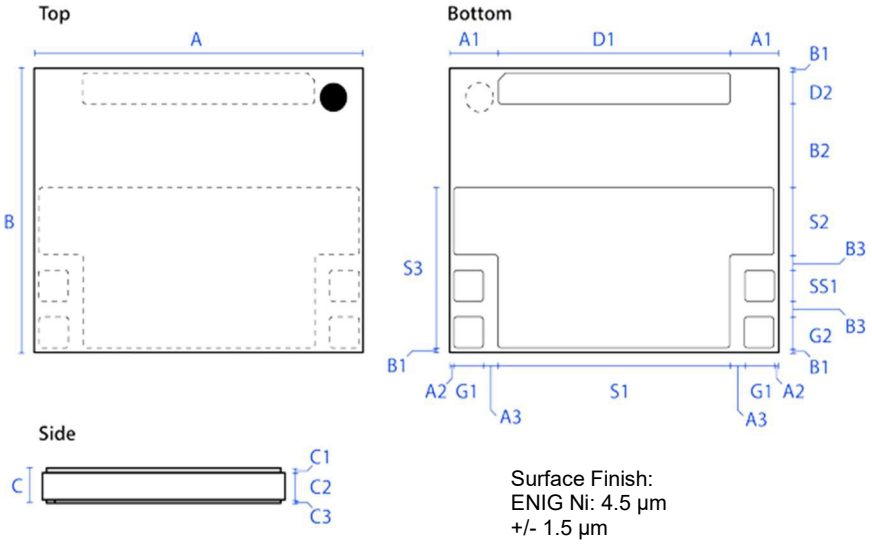
	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	7.97	1.10	0.314	0.043
B_1	7.97	5.27	0.314	0.207
B_2	1.50	2.27	0.059	0.089
C	1.10	1.10	0.043	0.043

Dimensions

	mm	Inches
d	3.94	0.155
e	1.85	0.073
f	4.94	0.194
g	3.94	0.155
h	2.44	0.096
i	4.735	0.186
j	0.35	0.014

PCB pad openings
Package outline

Bottom-side Cooled Package Dimensions

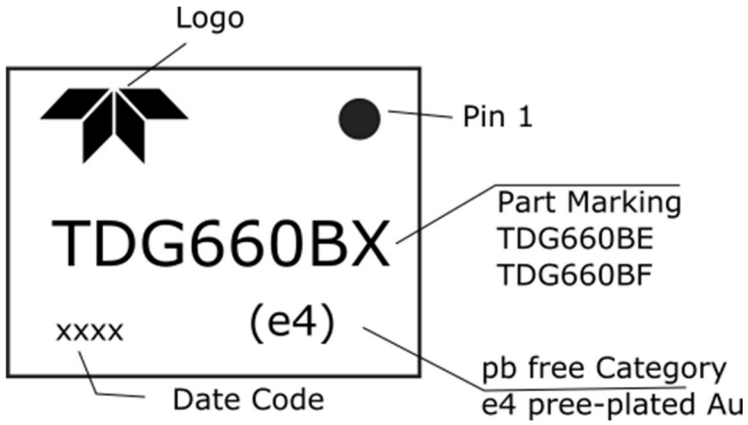


	mm	Inches	
A	11.0	0.433	± 0.10 mm (0.004")
A1	1.565	0.062	± 0.05 mm (0.002")
A2	0.065	0.003	± 0.05 mm (0.002")
A3	0.50	0.020	
B	9.00	0.354	± 0.10 mm (0.004")
B1	0.065	0.003	± 0.05 mm (0.002")
B2	2.70	0.106	
B3	0.50	0.020	
C	0.54	0.021	± 15%
C1	0.07	0.003	
C2	0.43	0.017	
C3	0.04	0.002	
D1	7.87	0.310	
D2	1.00	0.039	
G1	1.00	0.039	
G2	1.00	0.039	
S1	7.87	0.310	
S2	2.17	0.085	
S3	5.17	0.204	
SS1	1.00	0.039	

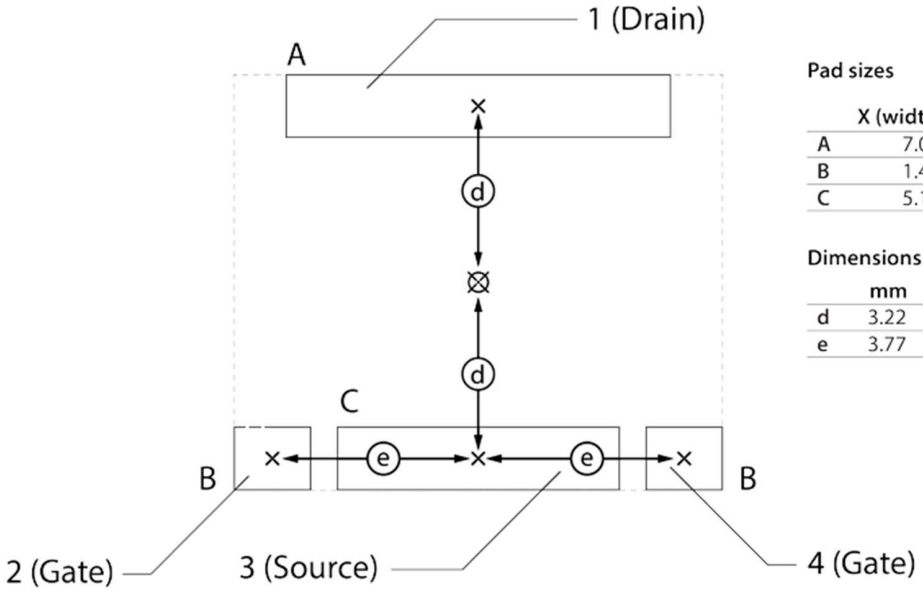
Surface Finish:
ENIG Ni: 4.5 µm
+/- 1.5 µm
Au: 0.09 µm +/- 0.03

Note: Inch measurements are approximate values

Bottom-side Cooled GaN*PX*® Part Marking



Top Side Cooled Recommended Minimum Footprint for Printed Circuit Board



Pad sizes

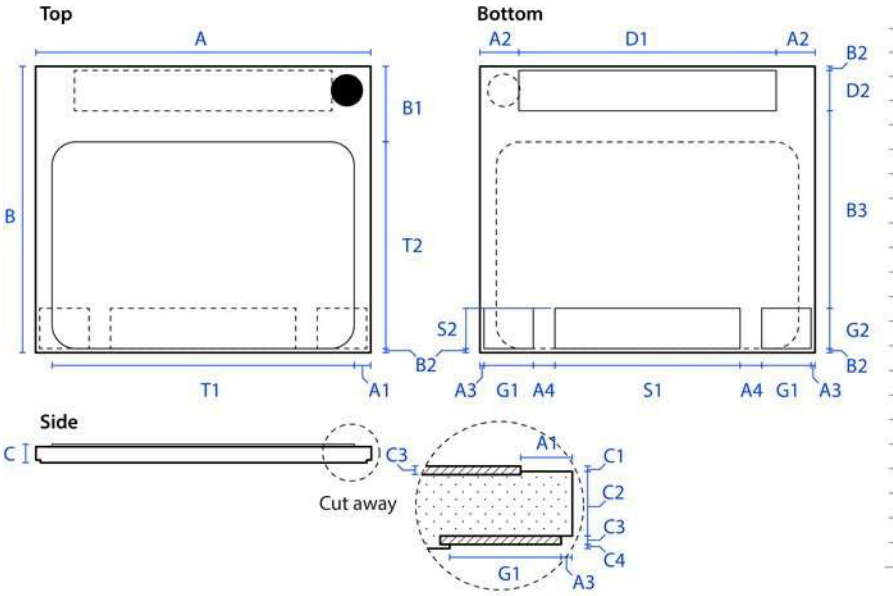
	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	7.04	1.15	0.277	0.045
B	1.40	1.15	0.055	0.045
C	5.17	1.15	0.204	0.045

Dimensions

	mm	Inches
d	3.22	0.127
e	3.77	0.148

PCB pad openings
Package outline

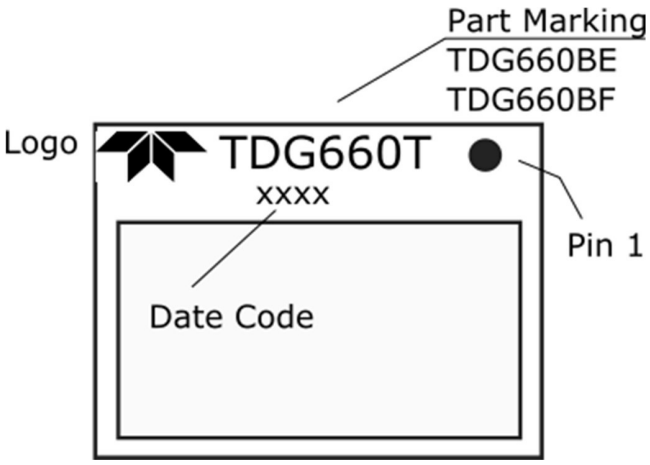
Top-side Cooled Package Dimensions



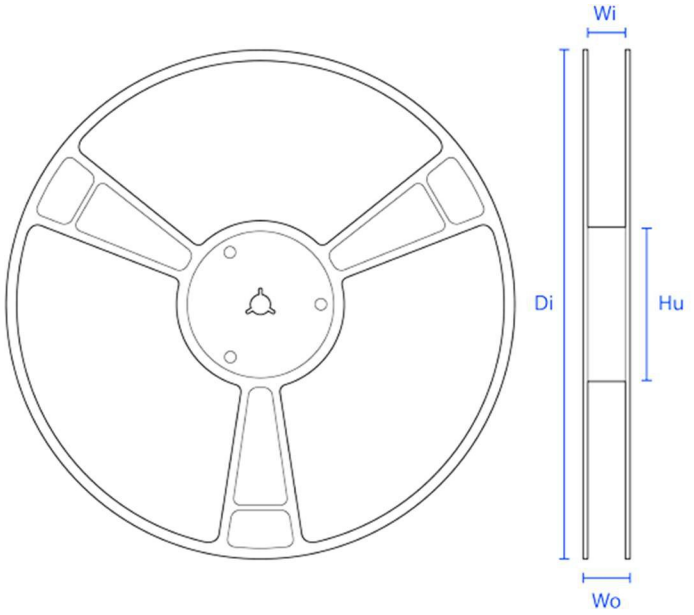
	mm	Inches	
A	9.00	0.354	± 0.10 mm (0.004″)
A1	0.365	0.014	± 0.05 mm (0.002″)
A2	1.03	0.041	± 0.05 mm (0.002″)
A3	0.075	0.003	± 0.05 mm (0.002″)
A4	0.59	0.023	
B	7.64	0.301	± 0.10 mm (0.004″)
B1	1.925	0.076	± 0.05 mm (0.002″)
B2	0.075	0.003	± 0.05 mm (0.002″)
B3	5.39	0.212	
C	0.54	0.0213	± 0.05 mm (0.002″)
C1	0.04	0.0016	
C2	0.40	0.0157	
C3	0.07	0.0028	
C4	0.03	0.0012	
D1	6.94	0.273	
D2	1.05	0.041	
G1	1.30	0.051	
G2	1.05	0.041	
S1	5.07	0.200	
S2	1.05	0.041	
T1	8.27	0.326	
T2	5.64	0.222	

Note: Inch measurements are approximate values

Top Side Cooled GaN*PX*® Part Marking

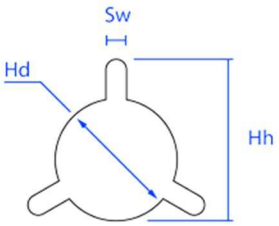


TDG650E60 GaN*PX*® Tape and Reel Information

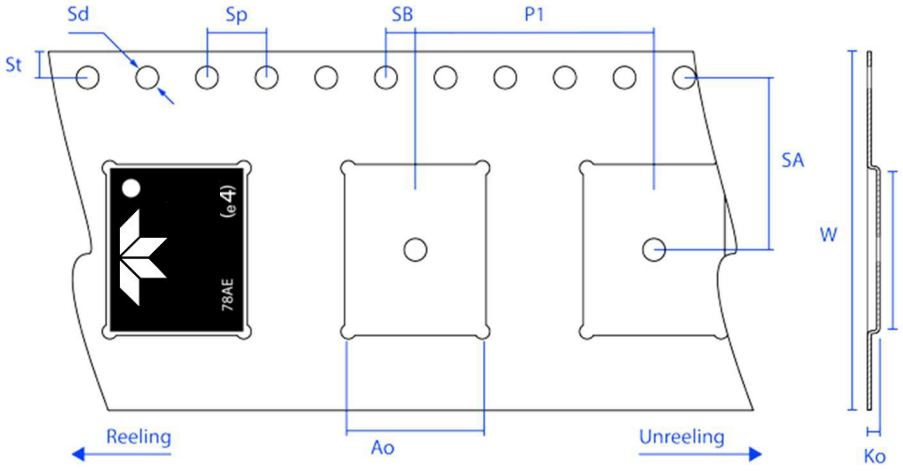


Dimensions (mm)

	13" reel (330 mm)		7" mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	178.0	+ 1.0 / - 0.0
Wo	30.4	MAX	27.7	+/-1.0
Wi	24.4	+ 2.0 / - 0.0	25.0	+ 1.0 / - 0.0
Hu	100.0	+/- 1.5	60.0	+ 1.0 / - 0.0
Hh	17.2	+/- 0.2	17.0	+/- 0.5
Sw	2.2	+/- 0.2	2.0	+/- 0.5
Hd	13.0	+ 0.5 / - 0.2	13.0	+/- 0.2



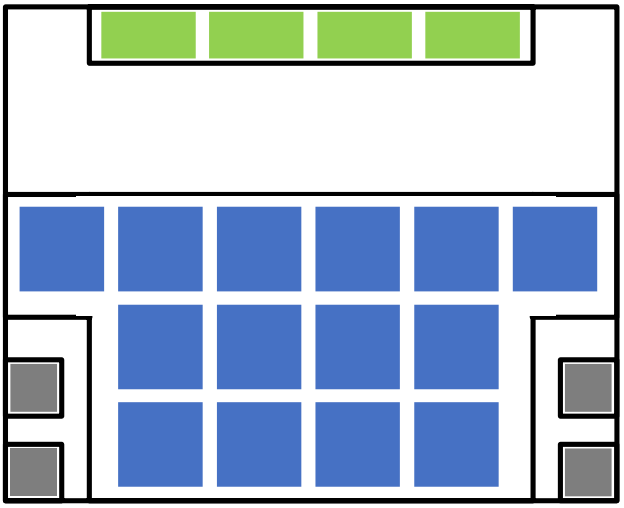
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	16.00	+/- 0.1
W	24.00	+ 0.3 / - 0.1
Ko	1.14	+/- 0.1
Ao	9.48	+/- 0.1
Bo	11.43	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	11.50	+/- 0.1
SB	2.00	+/- 0.1

Recommended Solder Stencil for Bottom-side Cooled PCB Footprint

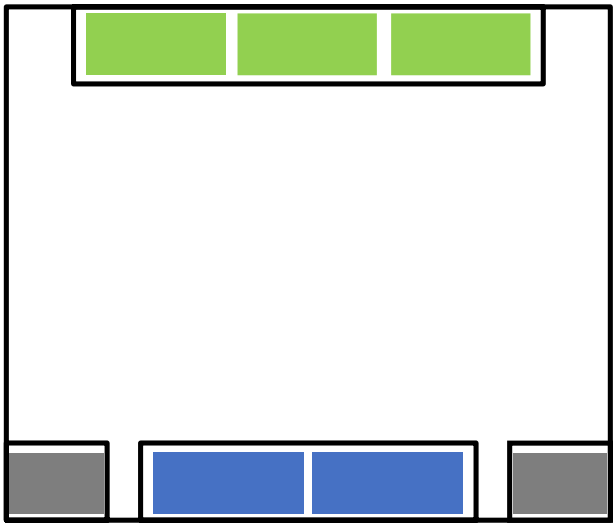


Dimension of stencil aperture

0.97 x 0.97 mm
1.7 x .81 mm
1.49 x 1.49 mm

- Thickness of stencil: 100 µm
- Solder paste coverage: 70%

Recommended Solder Stencil for Top-side Cooled PCB Footprint



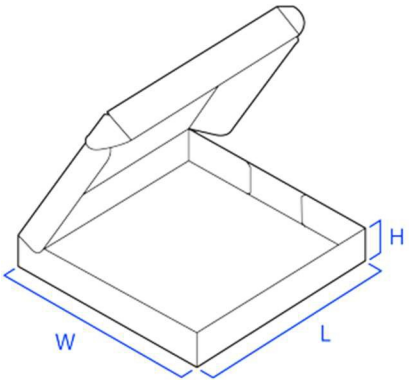
Dimension of stencil aperture

1.3 x 0.9 mm
2.32 x 0.9 mm
2.1 x 0.9 mm

- Thickness of stencil: 100 µm
- Solder paste coverage: 70%

The TDG650E60T offers top-side thermal transfer through a heat-sink attached directly to the device. The top-side cooling interface offers advantages such as keeping the thermal transfer path outside the PCB, but care must be taken with the mechanical interface between the heat sink and package to prevent damage to the device. For more details, please refer to the thermal design guide application note " GN002_Thermal-Design-Guide-for-Top-Side-Cooled-GaNpx-T-Devices" at www.gansystems.com

Tape and Reel Box Dimensions



Outside dimensions (mm)		
	7″ mini-reel	13″ tape-reel
W	197	342
L	204	355
H	32	53

Document Revision History:

Document No.	Description	Date
TDG650E60 Rev 180725d_1	Initial Release	12/17/2019
TDG650E60 04_2020 Rev1	• Updated Absolute Maximum Ratings table • Updated Electrical Characteristics table • Updated Electrical Performance Graphs • Added Recommended Solder Stencil	4/8/2020

Document Categories

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

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