TDC1049

High-Speed A/D Converter

9-Bit, 30 Msps

Features

- 30 Msps conversion rate, 15 MHz analog bandwidth
- 9-Bit resolution and linearity
- Sample-and-hold circuit not required
- Differential phase 0.5 degrees
- Differential gain 1.0%
- Overflow flag
- Single -5.2V power supply
- Differential ECL outputs
- Available in a 64-pin DIP, 68-contact LCC and 68-pin ceramic pin grid array

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Applications

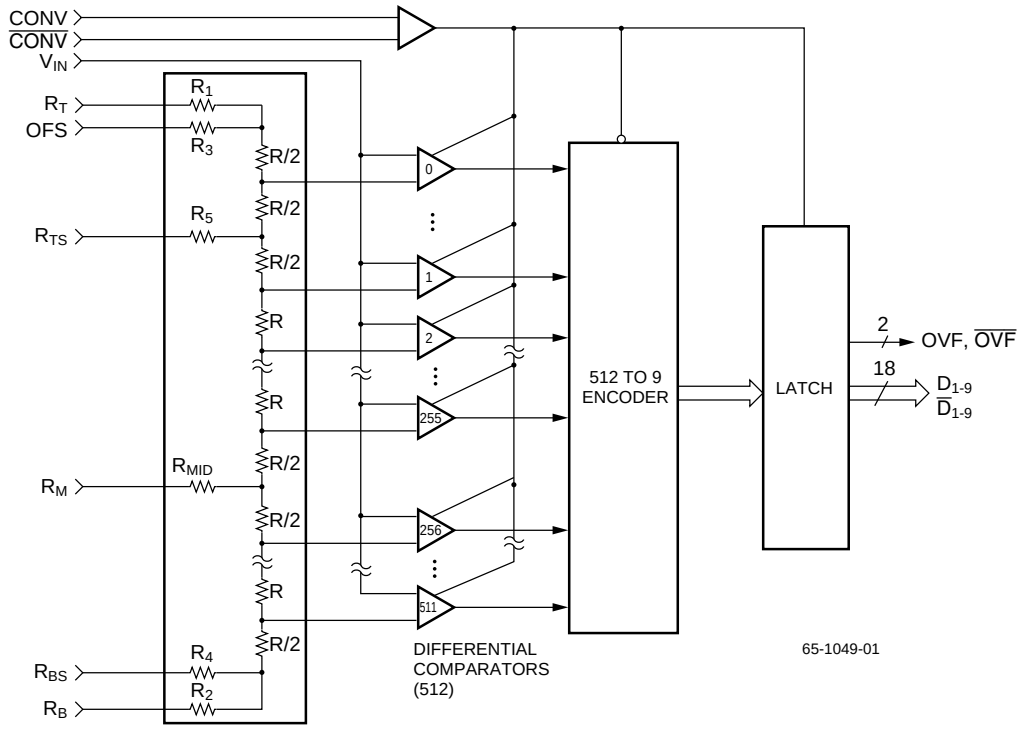
- Video data conversion
- Radar data conversion
- High-speed data acquisition

Description

The TDC1049 is a flash (full-parallel) analog-to-digital converter capable of converting analog signals with full-power frequency components up to 15 MHz into 9-bit words at rates up to 30 Msps (Megasamples Per Second). A sample-and-hold circuit is not required. All digital inputs and outputs are differential ECL.

The TDC1049 consists of 512 latching comparators, encoding logic and an output register. A differential convert signal controls the conversion operation. The outputs can be connected to give either true or inverted binary or offset two's complement fommats.

Block Diagram



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Functional Description

General Information

The TDC1049 has three functional sections: a comparator array, encoding logic and output register. The comparator array compares the input signal with 512 reference voltages to produce an N-of-512 code or “thermometer” code. The comparators referenced to voltages less than the input signal will be on and those referenced to voltages greater than the input signal will be off. The encoding logic converts the N-of-512 code into 9-bit binary data. The output register holds the output between updates.

Power

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For optimum performance, separate analog and digital power, V_{EEA} and V_{EED} should be supplied to the TDC1049. Separate analog and digital power supplies or a common supply with separate analog and digital paths and high-frequency decoupling can be used. The return path for the current drawn from V_{EEA} and V_{EED} is A_{GND} and D_{GND}, respectively. The returns A_{GND} and D_{GND} should also be kept separate and connected together at the power supply terminals. It is recommended that provisions be made on the printed circuit board for shorting jumpers between analog and digital ground as close to the A/D converter as possible. The installation of the jumpers depends upon the printed circuit board layout and overall system performance once the system is in operation. The voltage difference between V_{EEA} and V_{EED} must be less than +0.1V. The same voltage difference limit applies to the difference between A_{GND} and D_{GND}. All power and ground inputs to the converter must be connected.

Reference

The TDC1049 converts analog signals in the range $V_{RB} < V_{IN} < V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B) at the bottom of the reference resistor chain, and V_{RT} (the voltage applied to R_T) at the top of the reference resistor chain, should both be between +0.1V and -2.1V. Within that range, V_{RT} must be more positive than V_{RB}. The linearity specification is based upon a 2.0V difference between V_{RT} and V_{RB}. The nominal voltages are V_{RT} = 0.0V and V_{RB} = -20V. To avoid damage to the converter, the voltage across V_{RT} and V_{RB} must not exceed 2.2V. A decoupling capacitor is recommended between R_B and A_{GND}. Noise introduced at this point, as well as the other reference inputs (R_T, R_{TS}, R_M, R_{BS}, OFS), may result in encoding errors.

A midpoint tap, R_M, allows the converter to be adjusted for optimum integral linearity. It can also be used to achieve a nonlinear transfer function, but adjustment of R_M is not required to meet 9-bit linearity. If this node is driven by external circuitry, it should be driven from a low-impedance source; if not used, it must be left open.

Parasitic resistances, R1 and R2, introduce offset errors at the top and bottom of the reference resistor chain. Sense points, R_{TS}, R_{BS} and OFS, may be used to reduce the effect of these offset errors. Overflow Sense (OFS) may be used to reduce the effect of the offset at the overflow (most positive) comparator whenever the Overflow (OVF, $\overline{OVF}$) flags are used. Sense points are not required for 9-bit linearity and, if not used, they must be left open.

Convert

The TDC1049 requires a differential ECL clock (CONV and $\overline{CONV}$) signal. The conversion occurs (the comparators are latched) within t_{STO} (Sampling Time Offset) of the rising edge of CONV. The 512 to 9 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output register on the next rising edge of CONV. Data for sample N is available at the output t_D (Output Delay Time) after the rising edge of sample N+1.

Analog Input

The TDC1049 uses latching comparators which are connected to the analog inputs V_{IN}. For optimal performance, the source impedance of the driver amplifier should be less than 25Ω. The input signal will not damage the TDC1049 if it remains within the range of V_{EEA} to +0.5V. If the input signal is between the V_{RT} and V_{RB}, the output will be a binary number between 0 and 511 inclusive. All five analog inputs must be connected.

Outputs

The outputs of the TDC1049 are differential ECL. The recommended pull-down resistance is 500Ω to -2V, or a 220/330Ω termination between D_{GND} and V_{EED}. The OVF signal indicates that the analog input has exceeded the threshold of the most positive comparator. Data is held valid at the output register for at least t_{HO} (Output Hold Time) after the rising edge of CONV. New data becomes valid t_D after the rising edge of CONV.

No Connects

There are several pins labeled NC (No Connect). These pins are not connected internally and may be either left open or connected to analog ground to aid heat transfer from the package and to reduce electrical noise.

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Pin Assignments

64 Lead Sidebrazed Ceramic DIP

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	D_8	17	V_{EEA}	33	D_2	49	V_{IN}
2	D_7	18	NC	34	$\overline{D_1}$ (MSB)	50	V_{IN}
3	$\overline{D_7}$	19	V_{EEA}	35	D_1 (MSB)	51	A_{GND}
4	D_6	20	NC	36	$\overline{OVF}$	52	A_{GND}
5	$\overline{D_6}$	21	NC	37	OVF	53	V_{IN}
6	D_5	22	V_{EED}	38	D_{GND}	54	NC
7	$\overline{D_5}$	23	NC	39	D_{GND}	55	R_T
8	A_{GND}	24	NC	40	R_{BS}	56	OFS
9	NC	25	A_{GND}	41	R_B	57	R_{TS}
10	NC	26	NC	42	NC	58	D_{GND}
11	V_{EED}	27	NC	43	V_{IN}	59	$\overline{CONV}$
12	NC	28	$\overline{D_4}$	44	NC	60	CONV
13	NC	29	D_4	45	A_{GND}	61	D_{GND}
14	V_{EEA}	30	$\overline{D_3}$	46	A_{GND}	62	$\overline{D_9}$ (LSB)
15	NC	31	D_3	47	V_{IN}	63	D_9 (LSB)
16	NC	32	$\overline{D_2}$	48	R_M	64	$\overline{D_8}$

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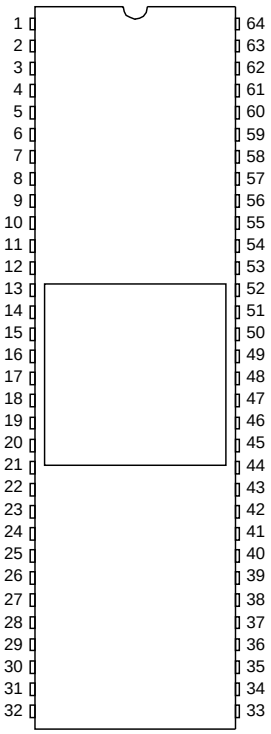

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64 Lead Bottombraze Ceramic DIP

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$\overline{D_8}$	17	R_M	33	$\overline{D_2}$	49	NC
2	D_9 (LSB)	18	V_{IN}	34	D_3	50	NC
3	$\overline{D_9}$ (LSB)	19	A_{GND}	35	$\overline{D_3}$	51	V_{EEA}
4	D_{GND}	20	A_{GND}	36	D_4	52	NC
5	CONV	21	NC	37	$\overline{D_4}$	53	NC
6	$\overline{CONV}$	22	V_{IN}	38	NC	54	V_{EED}
7	D_{GND}	23	NC	39	NC	55	NC
8	R_{TS}	24	R_B	40	A_{GND}	56	NC
9	OFS	25	R_{BS}	41	NC	57	A_{GND}
10	R_T	26	D_{GND}	42	NC	58	D_5
11	NC	27	D_{GND}	43	V_{EED}	59	$\overline{D_5}$
12	V_{IN}	28	OVF	44	NC	60	D_6
13	A_{GND}	29	$\overline{OVF}$	45	NC	61	$\overline{D_6}$
14	A_{GND}	30	D_1 (MSB)	46	V_{EEA}	62	D_7
15	V_{IN}	31	$\overline{D_1}$ (MSB)	47	NC	63	$\overline{D_7}$
16	V_{IN}	32	D_2	48	V_{EEA}	64	D_8

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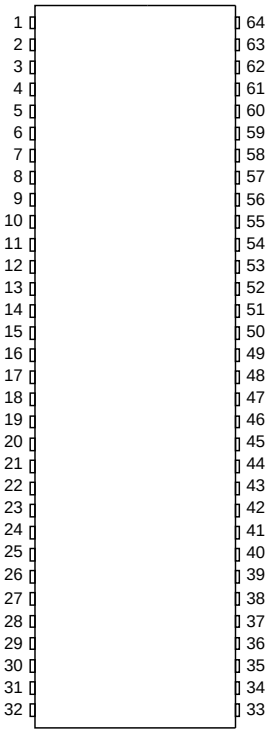

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Pin Assignments (continued)

68 Lead LCC

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	D_8	18	V_{EEA}	35	$\overline{D}_2$	52	R_M
2	$\overline{D}_7$	19	NC	36	D_2	53	V_{IN}
3	D_7	20	V_{EEA}	37	$\overline{D}_1$ (MSB)	54	V_{IN}
4	$\overline{D}_6$	21	V_{EEA}	38	D_1 (MSB)	55	A_{GND}
5	D_6	22	V_{EED}	39	$\overline{OVF}$	56	NC
6	$\overline{D}_5$	23	NC	40	OVF	57	A_{GND}
7	D_5	24	NC	41	D_{GND}	58	V_{IN}
8	NC	25	NC	42	NC	59	R_T
9	A_{GND}	26	NC	43	R_{BS}	60	NC
10	NC	27	A_{GND}	44	R_B	61	OFS
11	NC	28	NC	45	NC	62	R_{TS}
12	NC	29	NC	46	V_{IN}	63	$\overline{CONV}$
13	V_{EED}	30	NC	47	NC	64	CONV
14	V_{EEA}	31	$\overline{D}_4$	48	A_{GND}	65	D_{GND}
15	NC	32	D_4	49	A_{GND}	66	$\overline{D}_9$ (LSB)
16	V_{EEA}	33	$\overline{D}_3$	50	V_{IN}	67	D_9 (LSB)
17	NC	34	D_3	51	NC	68	$\overline{D}_8$

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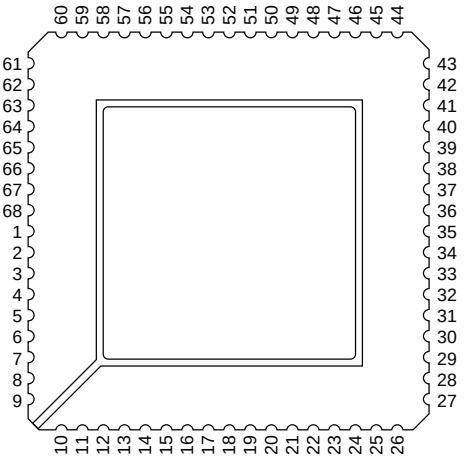

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68 Lead Ceramic Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	V_{EEA}	F10	D_8	K4	A_{GND}
A3	V_{EED}	B10	NC	F11	$\overline{D}_7$	K5	V_{IN}
A4	NC	B11	A_{GND}	G1	$\overline{D}_1$ (MSB)	K6	V_{IN}
A5	NC	C1	NC	G2	D_1 (MSB)	K7	NC
A6	NC	C2	NC	G10	D_9 (LSB)	K8	A_{GND}
A7	NC	C10	D_5	G11	$\overline{D}_8$	K9	V_{IN}
A8	NC	C11	NC	H1	$\overline{OVF}$	K10	R_{TS}
A9	NC	D1	D_4	H2	OVF	K11	$\overline{CONV}$
A10	V_{EED}	D2	$\overline{D}_4$	H10	D_{GND}	L2	NC
B1	NC	D10	D_6	H11	$\overline{D}_9$ (LSB)	L3	NC
B2	A_{GND}	D11	$\overline{D}_5$	J1	NC	L4	A_{GND}
B3	V_{EEA}	E1	D_3	J2	D_{GND}	L5	R_M
B4	NC	E2	$\overline{D}_3$	J10	CONV	L6	NC
B5	V_{EEA}	E10	D_7	J11	D_{GND}	L7	V_{IN}
B6	V_{EEA}	E11	$\overline{D}_6$	K1	R_{BS}	L8	A_{GND}
B7	V_{EEA}	F1	D_2	K2	R_B	L9	R_T
B8	NC	F2	$\overline{D}_2$	K3	V_{IN}	L10	OFS

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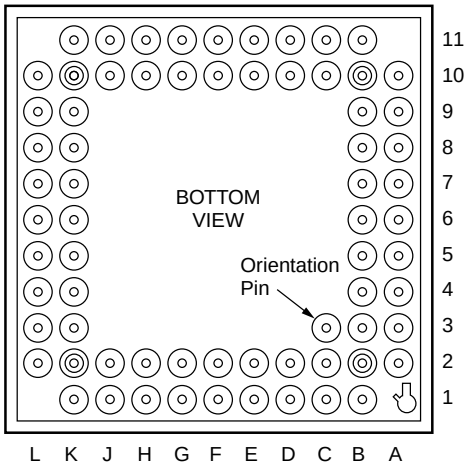

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Pin Definitions

Pin Name	Pin Number				Value	Pin Function Description
	Bottom-brazed DIP	Sidebrazed DIP	LCC	PGA		
V_{EEA}	46, 48, 51	14,17,19	14, 16, 18, 20, 21	B9, B7, B6, B5	-5.2V	Analog Supply Voltage
V_{EED}	43, 54	11, 22	13, 22	A3, A10	-5.2V	Digital Supply Voltage
D_{GND}	4, 7, 26, 27	38, 39, 58, 61	41, 65	J2, J11, H10	0.0V	Digital Ground
A_{GND}	13, 14, 19, 20, 40, 57	8, 25, 45, 46, 51, 52	9, 27, 48, 49, 55, 57	B2, K4, L4, K8, L8,	0.0V	Analog Ground
R_T	10	55	59	L9	0.0V	Reterence Resistor, Top
R_{TS}	8	57	62	K10	0.0V	Reference Resistor, Top Sense
R_B	24	41	44	K2	-2.0V	Reference Resistor, Bottom
R_{BS}	25	40	43	K1	-2 0V	Reference Resistor, Bottom Sense
R_M	17	48	52	L5	-1.0V	Reference Resistor, Midpoint
OFS	9	56	61	L10	0.0V	Overflow Sense
CONV	5	60	64	J10	ECL	Convert
$\overline{CONV}$	6	59	63	K11	ECL	Convert, Complement
V_{IN}	12, 15, 16, 18, 22	43, 47, 49, 50, 53	46, 50, 53, 54, 58	K3, K5, K6, L7, K9	0V to -2V	Analog Signal Input
D_1 MSB	30	35	38	G1	ECL	Most Significant Bit
D_2–D_8	32, 34, 36, 58, 60, 62, 64	33, 31, 29, 7, 5, 3, 1	36, 34, 7, 5, 3, 1	F1, E1, D1, C10, D10, E10, F10	ECL	
D_9 LSB	2	63	67	G10	ECL	Least Significant Bit
$\overline{D}_1$ MSB	31	34	37	G2	ECL	Most Significant Bit Complement
$\overline{D}_2$–$\overline{D}_8$	33, 35, 37, 59, 61, 63, 1	32, 30, 28, 6, 4, 2, 64	35, 33, 31, 6, 4, 2, 68	F2, E2, D2, D11, E11, F11, G11	ECL	
$\overline{D}_9$ LSB	3	62	66	H11	ECL	Least Significant Bit Complement
OVF	28	37	40	H2	ECL	Ovedlow Output
$\overline{OVF}$	29	36	39	H1	ECL	Overflow Output Complement
NC	11, 21, 23, 38, 39, 41, 42, 44, 45, 47, 49, 50, 52, 53, 55, 56	9, 10, 12, 13, 15,16, 18, 20, 21, 23, 24, 26, 27, 42, 44, 54	8, 10, 11, 12, 15, 17, 19, 23, 24, 25, 26, 28, 29, 30, 42, 45, 47, 51, 56, 60	B1, C2, C1, J1, L2, L3, L6, K7, C11, B10, A9, B8, A8, A7, A6, A5, B4, A4, A2	Open	No Connect

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Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min.	Max.	Unit
Supply Voltages			
V_{EED} (measured to D_{GND})	-7.0	+0.5	V
V_{EEA} (measured to A_{GND})	7.0	+0.5	V
A_{GND} (measured to D_{GND})	-1.0	+1.0	V
V_{EEA} (measured to V_{EED})	-0.5	+0.5	V
Input Voltages[2]			
CONV, $\overline{CONV}$ (measured to D_{GND})	+0.5	V_{EE}	V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5	V_{EE}	V
V_{RT} (measured to V_{RB})	-2.5	+2.5	V
Output			
Short-circuit duration (single output in HIGH state to ground)	Infinite		
Temperature			
Operating, case	-60	+140	°C
junction		+175	°C
Lead, soldering (10 seconds)		300	°C
Storage	- 65	+150	°C

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Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
V_{EED}	Digital Supply Voltage (measured to D_{GND})	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
V_{EEA}-V_{EED}	Supply Voltage Differential	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LDW	12			12			ns
t_{PWH}	CONV Pulse Width, HIGH	15			15			ns
V_{ICM}	Input Voltage, Common Mode	-0.5		-2.5	-0.5		-2.5	V
V_{IDF}	Input Voltage, Differential	0.3		1.2	0.3		1.2	V
V_{IN}	Input Voltage Range	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
V_{RT}	Most Positive Reference Inputs[1]	-0.1	0.0	0.1	-0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input[1]	-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

Note:

1. V_{RT} must be more postive than V_{RB}, and the voltage reference differential must be within the specified range.

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DC Electrical Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min.	Max.	Min.	Max.	
I_{EE}	Supply Current	V_{EED}, V_{EEA} = Max					
		T_A = 0°C to 70°C		-950			mA
		T_A = 70°C		-750			mA
		I_C = - 55°C to 125° C				-1090	mA
		T_C = 125°C				-750	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom	10	36	10	36	mA
R_{REF}	Total Reference Resistance		56	200	56	200	Ω
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	16		16		KΩ
C_{IN}	Analog Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		160		160	pF
I_{CB}	Inpul Constant Bias Current	V_{EEA} = Max, V_{IN} = 0V		500		750	µA
I_I	Input Current, CONV, $\overline{CONV}$	V_{EED} = Max, V_I = -0.7V		150		180	µA
V_{OL}	Output Voltage, Logic LOW[1]	V_{EED} = Nom		-1.6		-1.5	V
V_{OH}	Output Voltage, Logic HIGH[1]	V_{EED} = Nom	-0.95		-1.1		V
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		20		20	pF

Note:
1. Test Load = 500Ω to -2v on each output.

AC Electrical Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min.	Max.	Min.	Max.	
F_S	Maximum Conversion Rate	V_{EED}, V_{EEA} = Min	30		30		Msps
t_{STO}	Sampling Time Offset	V_{EED}, V_{EEA} = Min	-2	6	-2	6	ns
t_D	Output Delay[1]	V_{EED}, V_{EEA} = Min		27		27	ns
t_{HO}	Output Hold Time[1]	V_{EED}, V_{EEA} = Min	3		3		ns

Note:
1. Test Load = 500Ω to -2V on each output, C_{LOAD} = 20pF.

Timing Diagrams

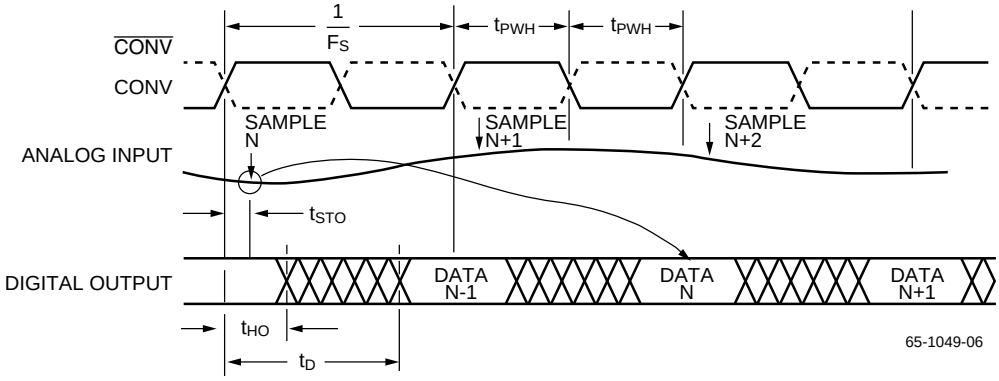

Figure 1. Timing Diagram

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Timing Diagrams (continued)

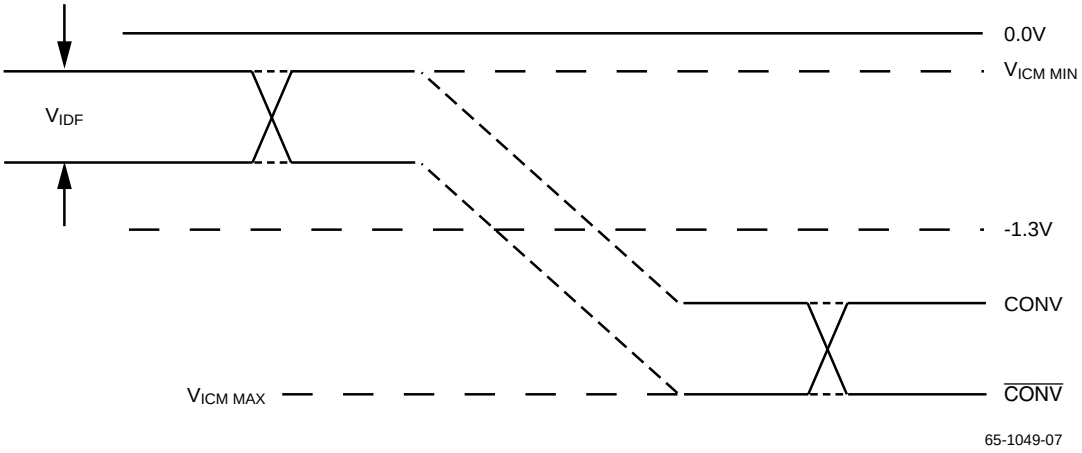

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Figure 2. CONVert, $\overline{\text{CONV}}$vert Switching Levels

System Performance Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min.	Max.	Min.	Max.	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.15		0.20	%
		V_{RT}, V_{RB} = Nom, V_{RM} Adjusted		0.10		0.10	%
E_{LD}	Linearity Error Differential	V_{RT}, V_{RB} = Nom		0.1		0.1	%
Q	Code Size	V_{RT}, V_{RB} = Nom	15	185	15	185	% Nominal
E_{OTS}	Offset Error, Top	V_{IN} = V_{RT}, R_{TS} Connected		±4		±4	mV
E_{OT}	Offset Error, Top	V_{IN} = V_{RT}		30		30	mV
E_{OBS}	Offset Error, Bottom	V_{IN} = V_{RB}, R_{BS} Connected		±4		±4	mV
E_{OB}	Offset Error, Bottom	V_{IN} = V_{RB}		-30		-30	mV
T_{CO}	Offset Error, Temperature Coefficient			20		20	µV/°C
t_{TR}	Transient Response, Full-Scale			20		20	ns
BW	Bandwidth, Full Power Input	±0.9dB Frequency Response	15		15		MHz
SNR	Signal-to-Noise Ratio	30Msps Conversion Rate, 10MHz Bandwidth					
	Peak Signal/RMS Noise	1.25MHz Input	57		57		dB
		5.0MHz Input	53		53		dB
	RMS Signal/RMS Noise	1.25MHz Input	48		48		dB
		5.0MHz Input	44		44		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error	F_S = 4 x NTSC		0.5		0.5	Degree
DG	Differential Gain Error	F_S = 4 x NTSC		1.5		1.5	%

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Typical Performance Curves

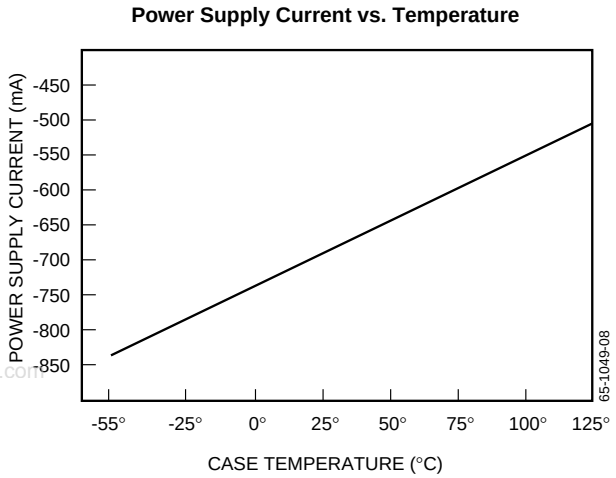

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Figure 3. Power Supply Current vs. Temperature

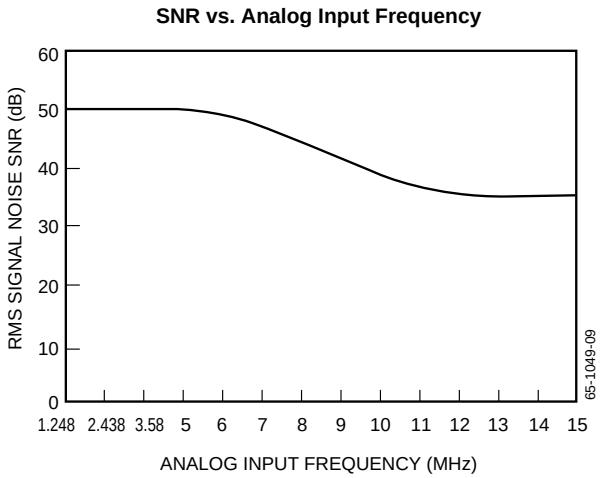

Figure 4. SNR vs. Analog Input Frequency

Equivalent Circuits

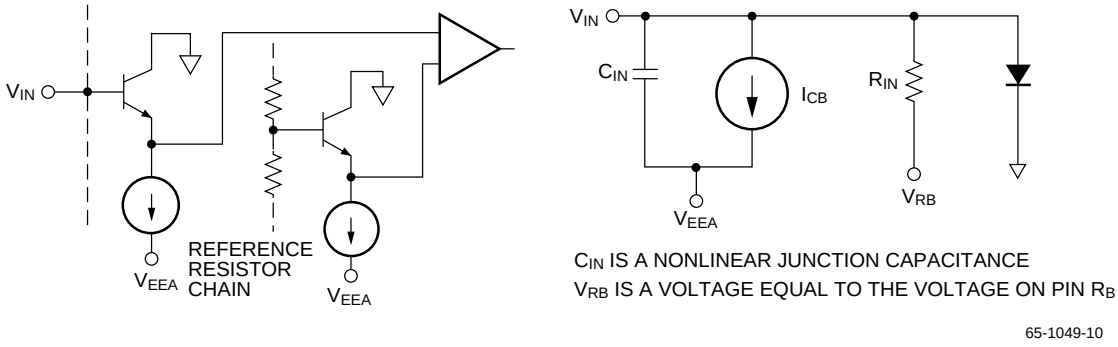

Figure 5. Simplified Analog Input Equivalent Circuits

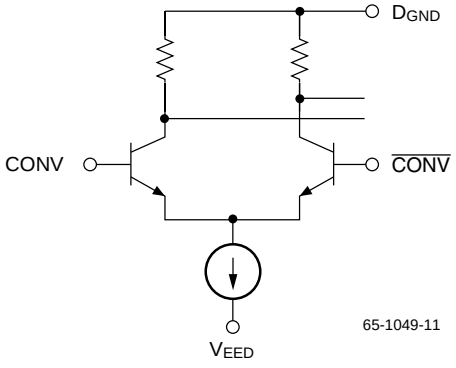

Figure 6. Digital Input Equivalent Circuit

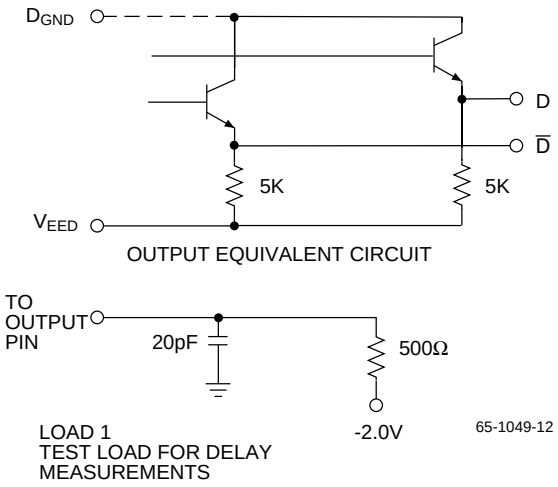

Figure 7. Output Circuits

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Output Coding Table[1]

V_{IN}	OVF	D_1 MSB	D_9 LSB
+0.0039V	1	000000000	
0.0000V	0	000000000	
-0.0039V	0	000000001	
•	•	•	
•	•	•	
•			
-0.9980V	0	011111111	
-1.0020V	0	100000000	
-1.0059V	0	100000001	
•	•	•	
•	•	•	
•			
-1.9961V	0	111111110	
-2.0000V	0	111111111	

Note:
1. Voltages are code midpoints.

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Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown on the back page of this document; however, the applicable SMD is the sole controlling document defining the SMD product.

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Notes:

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Mechanical Dimensions

64 Lead Sidebrazed Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.120	.175	3.05	4.44	
B1	.015	.023	.38	.58	7
B2	.040	.065	1.02	1.65	2
C1	.008	.015	.20	.38	7
D	3.170	3.240	80.52	82.30	
E	.880	.910	14.60	15.48	
e	.100 BSC		2.54 BSC		4, 8
eA	.900 BSC		22.86 BSC		6
L	.125	.175	3.18	4.45	
Q	.025	.065	.63	1.65	3
S1	.005	—	.13	—	5
S2	.005	—	.13	—	

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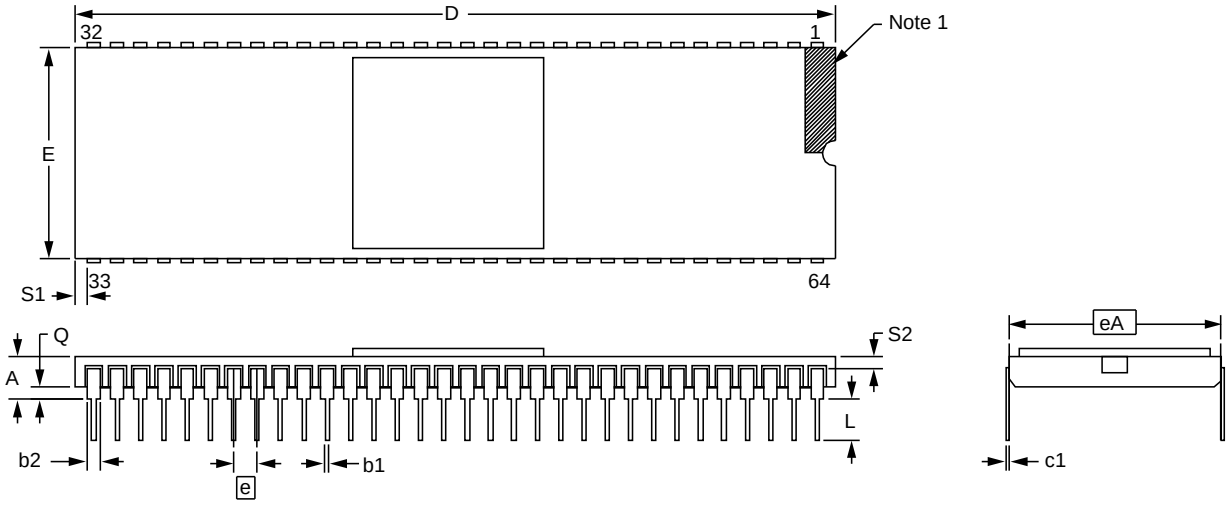
Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 32, 33, and 64 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 64.
5. Applies to all four corners (leads number 1, 32, 33, and 64).
6. "eA" shall be measured at the centerline of the leads.
7. All leads – Increase maximum limit by .003(.08mm) measured at the center of the flat when lead finish is applied.
8. Sixty-two spaces.



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Mechanical Dimensions (continued)

64 Lead Bottombrazed Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.125	.200	3.18	5.08	
B1	.015	.023	.38	.58	7
B2	.040	.065	1.02	1.65	2
C1	.008	.015	.20	.38	7
D	3.110	3.240	80.00	82.30	
E	.790	.810	20.07	20.57	
e	.100 BSC		2.54 BSC		4, 8
eA	.900 BSC		22.86 BSC		6
L	.125	.175	3.18	4.45	
Q	.050	.100	1.27	2.54	3
S1	.005	—	.13	—	5
S2	.005	—	.13	—	

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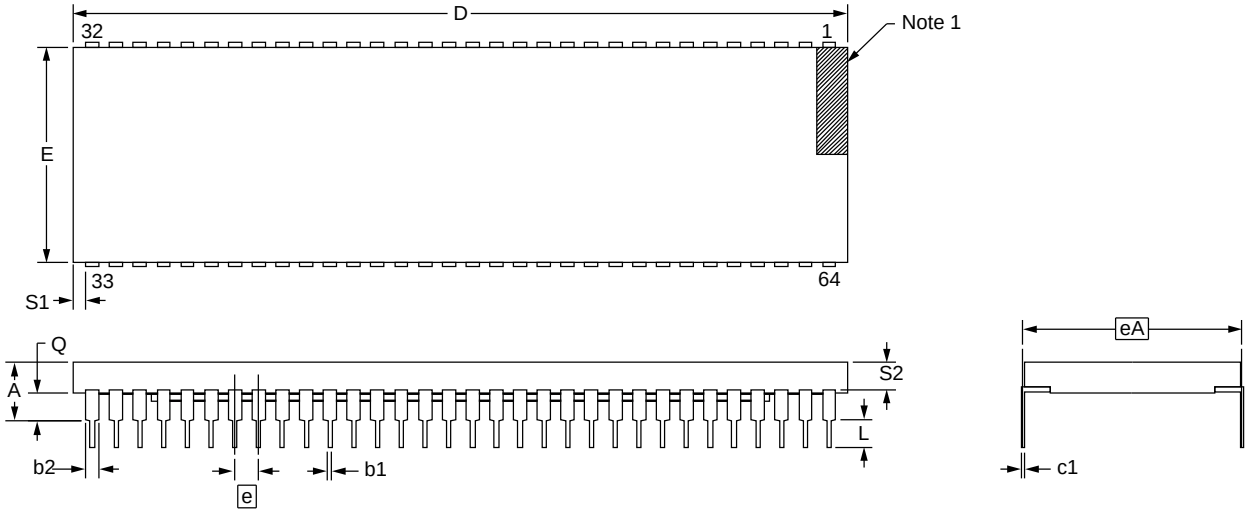
Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 32, 33, and 64 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 64.
5. Applies to all four corners (leads number 1, 32, 33, and 64).
6. "eA" shall be measured at the centerline of the leads.
7. All leads – Increase maximum limit by .003(.08mm) measured at the center of the flat when lead finish is applied.
8. Sixty-two spaces.



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Mechanical Dimensions (continued)

68 Lead LCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.082	.110	2.08	2.79	3, 6
A1	.071	.093	1.83	2.39	3, 6
B1	.022	.028	.560	.710	2
B3	.006	.022	.150	.560	2,5
D/E	.938	.962	23.82	24.43	
D1/E1	.800 BSC		20.32 BSC		
D2/E2	.400 BSC		10.16 BSC		
e	.050 BSC		1.27 BSC		
h	.040 BSC		1.02 BSC		4
j	.020 BSC		.510 BSC		4
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.91	2.41	
L3	.003	.015	.080	.380	5
ND/NE	17		17		
N	68		68		

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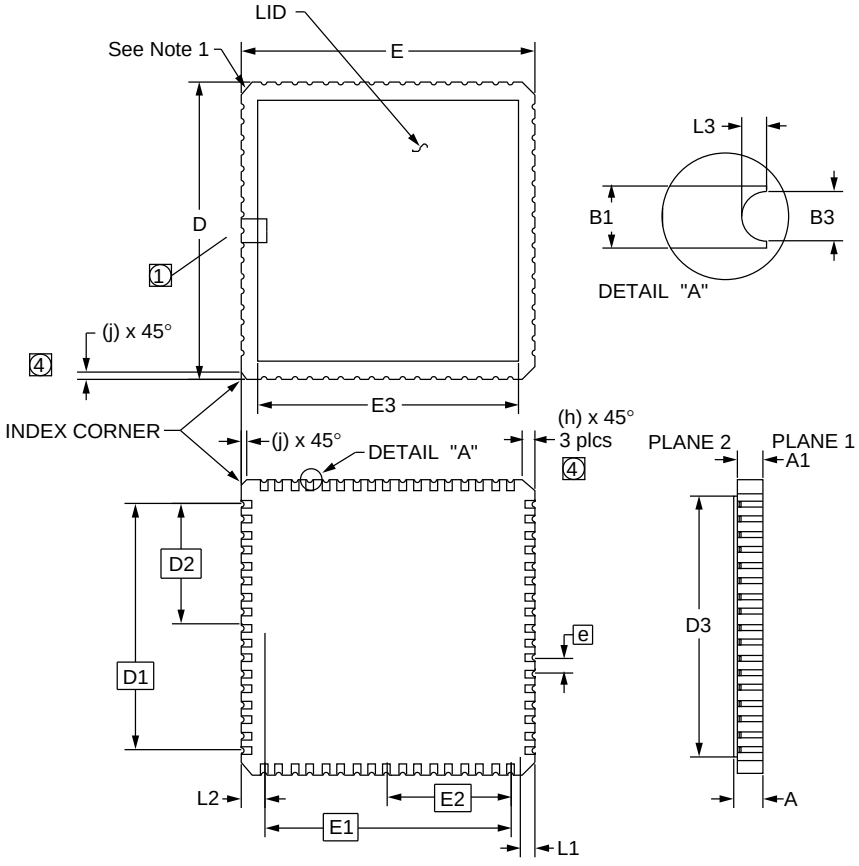
Notes:

1. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2. Plane 1 terminal 1 identification may be an extension of the length of the metallized terminal which shall not be wider than the B1 dimension.
2. Unless otherwise specified, a minimum clearance of .015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
3. Dimension "A" controls the overall package thickness. The maximum "A" dimension is the package height before being solder dipped.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing. The index corner shall be clearly unique.
5. Dimension "B3" minimum and "L3" minimum and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. Dimension "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dripping.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.



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Mechanical Dimensions (continued)

68 Lead Plastic Grid Array

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.025	.060	0.64	1.52	
A2	.105	.180	2.67	4.57	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

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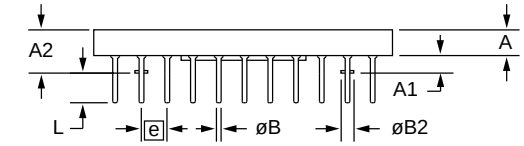
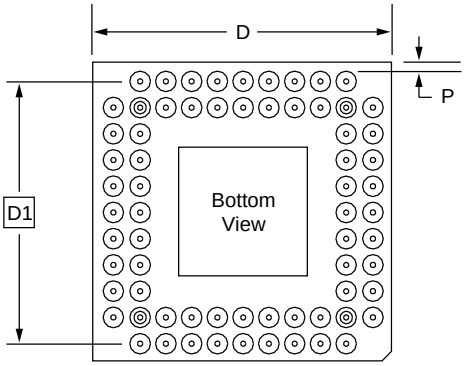
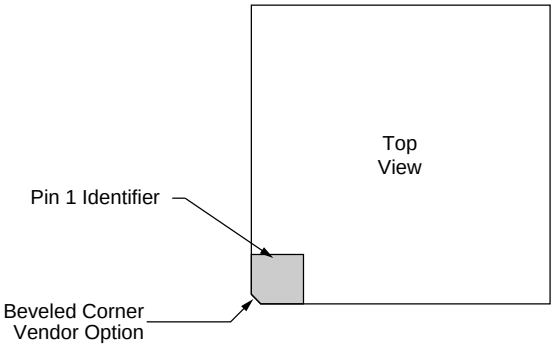
Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.







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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1049J0C	STD - T_A = 0°C to 70°C	Commercial	64 Lead Sidebrazed Ceramic DIP	1049J0C
TDC1049J0V	EXT - T_C = -55°C to 125°C	MIL-STD-883	64 Lead Sidebrazed Ceramic DIP	1049J0V
5962-8853201XA	EXT - T_C = -55°C to 125°C	Per Standard Mil Drawing	64 Lead Sidebrazed Ceramic DIP	5962-8853201XA
TDC1049C1C	STD - T_A = 0°C to 70°C	Commercial	68-Lead LCC	1049C1C
TDC1049C1V	EXT - T_C = -55°C to 125°C	MIL-STD-883	68-Lead LCC	1049C1V
5962-8853201ZA	EXT - T_C = -55°C to 125°C	Per Standard Mil Drawing	68-Lead LCC	5962-8853201ZA
TDC1049G8C	STD - T_A = 0°C to 70°C	Commercial	68 Lead Ceramic PGA	1049G8C
TDC1049G8V	EXT - T_C = -55°C to 125°C	MIL-STD-B83	68 Lead Ceramic PGA	1049G8V

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Standard Military Drawing	Nearest Equivalent Fairchild Product No.	Package
5962-8853201XA	TDC1049J0V	64 Lead Sidebrazed Ceramic DIP
5962-8853201YA	TDC1049J3V	64 Lead Bottombrazed Ceramic DIP
5962-8853201ZA	TDC1049C1V	68-Lead LCC
5962-8853201UA	TDC1049L1V	68-Lead LCC

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