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TDC1016

Video Speed D/A Converter

10-Bit, 20 Msps

Features

- 20 Msps conversion rate
- 8, 9, or 10-bit linearity
- Voltage output, no amplifier required
- Single supply operation (-5.2V, ECL compatible)
- Dual supply operation (±5.0V, TTL compatible)
- Internal 10-bit latched data register
- Low glitch energy
- Disabling controls, forcing full-scale, zero, and inverting input data
- Binary or two's complement input data formats
- Differential gain = 1.5%, differential phase = 1.0°

Applications

- Construction of video signals from digital data 3x or 4x NTSC or PAL color subcarrier frequency
- CRT graphics displays, RGB, Raster, Vector
- Waveform synthesis

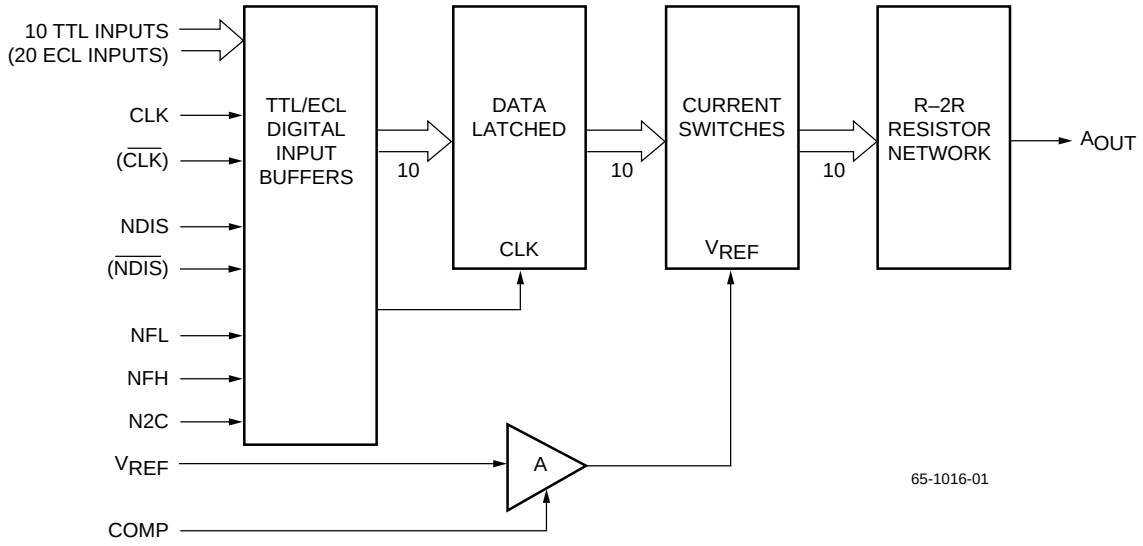
Description

The TDC1016 is a bipolar monolithic digital-to-analog converter which can convert digital data into an analog voltage at rates up to 20 Msps (Megasamples Per Second). The device includes an input data register and operates without an external deglitcher or amplifier.

Operating the TDC1016 from a single -5.2V power supply will bias the digital inputs for ECL levels, while operating from a dual ±5V power supply will bias the digital inputs for TTL levels.

All versions of the TDC1016 are 10-bit digital-to-analog converters, but are available with linearity specifications of either 8, 9, or 10 bits. The TDC1016 is patented under U.S. patent number 3283120 with other patents pending.

Block Diagram



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Functional Description

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General Information

TTL/ECL buffers are used for all digital inputs to the TDC1016. Logic family compatibility depends upon the connection of power supplies. When single power supply (-5.2V) operation is employed, all data, clock, and disable inputs are compatible with differential ECL logic levels. All digital inputs become compatible with TTL levels when dual power supply (±5.0V) operation is used.

The internal 10-bit register latches data on the rising edge of the clock (CLK) pulse. Currents from the current sources are switched accordingly and combined in the resistor network to give an analog output voltage. The magnitude of the output voltage is directly proportional to the magnitude of the digital input word.

The NFL and NFH inputs can be used to simplify system calibration by forcing the analog output voltage to either its zero-scale or full-scale value. The TDC1016 can be operated in binary, inverse binary, two's complement or inverse two's complement input data formats.

Power

The TDC1016 can be operated from a single -5.2V power supply or from a dual ±5.0V power supply. For single power supply operation, V_{CC} is connected to D_{GND} and all inputs to the device become ECL compatible. When V_{CC} is tied to +5.0V, the inputs are TTL compatible.

The return path for the output from the 10 current sources is A_{GND}. The current return path for the digital section is D_{GND}. D_{GND} and A_{GND} should be returned to system power supply ground by way of separate conductive paths to prevent digital ground noise from disturbing the analog circuitry of the TDC1016. All A_{GND} pins must be connected to system analog ground.

Reference

The reference input is normally set to -1.0V with respect to A_{GND}. Adjusting this voltage is equivalent to adjusting system gain The temperature stability of the TDC1016 analog output (A_{OUT}) depends primarily upon the temperature stability of the applied reference voltage

The internal operational amplifier of the TDC1016 is frequency stabilized by an external 1 μF tantalum capacitor connected between the COMP pin and V_{EE}. A minimum of 1 μF is adequate for most applications, but 10 microfarads or more is recommended for optimum performance. The negative side of this capacitor should be connected to V_{EE}.

Controls

The NDIS inputs are used to disable the TDC1016 by forcing its output to the zero-scale value (current sources off). The NDIS inputs are asynchronous, active without regard to the CLK inputs. The other digital control inputs are synchronous, latched on the rising edge of the CLK pulse.

The rising edge of the CLK pulse transfers data from the input lines to the internal 10-bit register. In TTL mode, the inverted inputs for CLK, DATA, and NDIS are inactive and should be left open.

The Input Coding Table illustrates the function of the digital control inputs. A two's complement mode is created by activating N2C with a Logic 0 When NFH and NFL are both activated with a Logic 0 the input data to the 10-bit register is inverted.

Data Inputs

Data inputs are ECL compatible when single power supply operation is employed. The J5 and C2 packages allow for differential ECL inputs while the J7 and B7 packages have only single-ended inputs. When differential ECL data is used, any data input can be inverted simply by reversing the connections to the true and inverted data input pins. All inverted input pins should be left open if single-ended ECL or TTL modes are used. All data inputs have an internal 40 KΩ pullup resistor to V_{CC}.

Analog Output

The analog output voltage is negative with respect to A_{GND} and varies proportionally with the magnitude of the input data word. The output resistance at this point is 80Ω, nominally.

No Connects

There are several pins labeled no connect (NC) on the TDC1016 J5 and C2 packages, which have no connections to the chip. These pins should be left open.

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Pin Assignments

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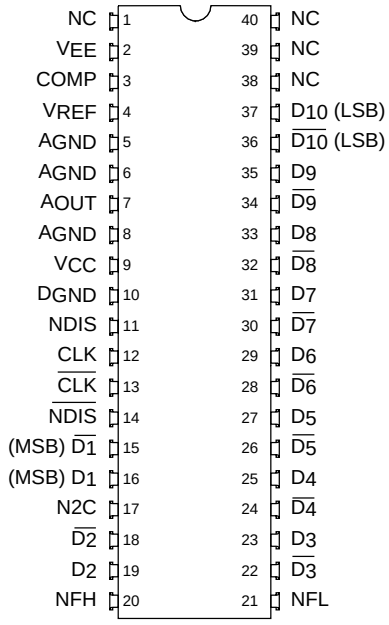
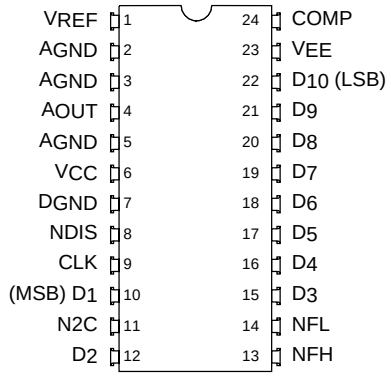
40 Lead Ceramic DIP



24 Lead Ceramic DIP



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Pin Descriptions

Pin Name	Pin Number 40-Lead	Pin Number 24-Lead	Value	Pin Function Description
Power				
V_{CC}	9	6	+5.0V	Positive Supply Voltage.
V_{EE}	2	23	-5.0V	Negative Supply Voltage.
A_{GND}	5, 6, 8	2, 3, 5	0.0V	Analog Ground.
D_{GND}	10	7	0.0V	Digital Ground.
Reference				
V_{REF}	4	1	-1.0V	Reference Voltage In.
COMP	3	24	1μF	Compensation.
Controls				
NDIS	11	8	TTL/ECL	Not Disable.
$\overline{NDIS}$	14	—	ECL	Not Disable (Inv).
CLK	12	9	TTL/ECL	Clock.
$\overline{CLK}$	13	—	ECL	Clock (Inv).
N2C	17	11	TTL/ECL	Not Two's Complement.
NFH	20	13	TTL/ECL	Not Force HIGH.
NFL	21	14	TTL/ECL	Not Force LOW.
Data Inputs				
D_1–D_{10}	16, 19, 23, 25, 27, 29, 31, 33, 35, 37	10, 12, 15–20, 27, 22	TTL/ECL	Data Bits 1–10. D_1 is the MSB, D_{10} is the LSB.

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Pin Descriptions (continued)

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Pin Name	Pin Number		Value	Pin Function Description
	40-Lead	24-Lead		
$\overline{D}_1$–$\overline{D}_{10}$	15, 18, 22, 24, 26, 28, 30, 32, 34, 36	—	ECL	Data Bits 1–10 (Inv). $\overline{D}_1$ is the MSB, $\overline{D}_{10}$ is the LSB.
Analog Output				
A_{OUT}	7	4	0V–1V	Analog Output Voltage
No Connection				
NC	1, 38–40	—	Open	No Connection

Absolute Maximum Ratings (beyond which the device wille be damaged)[1]

Parameter	Min.	Max.	Unit
Supply Voltages			
V_{CC} (measured to D_{GND})	-0.5	+7.0	V
V_{EE} (measured to A_{GND})	-7.0	+0.5	V
AG_{ND} (measured to D_{GND})	-0.5	+0.5	V
Input Voltages			
Digital (measured to D_{GND})	-7.0	+7.0	V
Reference (measured to A_{GND})	-1.5	+0.5	V
Output			
Applied Voltage (measured to A_{GND})[2]	-2.0	+2.0	V
Short-Circuit Duration	Indefinite		
Temperature			
Operating, Ambient		+125	°C
Operating, Junction		+175	°C
Lead, Soldering (10 seconds)		+300	°C
Storage	-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

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Operating Conditions

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Symbol	Parameter		Temperature Range						Unit
			Standard			Extended			
			Min.	Nom.	Max.	Min.	Nom.	Max.	
V_{CC}	Positive Supply Voltage	TTL Mode	4.75	5.0	5.25	4.50	5.0	5.50	V
		ECL Mode	-0.25	0.0	0.25	-0.25	0.0	0.25	V
V_{EE}	Negative Supply Voltage		-4.5	-5.0	-5.5	-4.5	-5.0	-5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})		-0.1	0.0	0.1	-0.1	0.0	0.1	V
t_{PWL}	CLK Pulse Width, LOW		15			20			ns
t_{PWH}	CLK Pulse Width, HIGH		15			20			ns
t_S	Input Register Set-up Time	TTL Mode	20			22			ns
		ECL Mode	25			27			ns
t_H	Input Register Hold Time		2			2			ns
V_{IL}	Logic 0	TTL Mode	D_{GND}		0.8	D_{GND}		0.8	V
		ECL Mode			-1.67			-1.67	V
V_{IH}	Logic 1	TTL Mode	2.0		V_{CC}	2.0[1]		V_{CC}	V
		ECL Mode	-1.0			-1.0			V
V_{REF}	Reference Voltage		-0.8	-1.0	-1.2	-0.8	-1.0	1.2	V
C_{COMP}	Compensation Capacitor		1.0			1.0			μF
T_A	Ambient Temperature		0		70				°C
T_C	Case Temperature					-55		125	°C

Note:

1. V_{IH}/NDIS = 2.2 Min.

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Temperature Range				Unit
			Standard		Extended		
			Min.	Max.	Min.	Max.	
I_{CC}	Power Supply Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		20		20	mA
I_{EE}	Power Supply Current	TTL Mode, V_{CC} = Max, V_{EE} = Max[1]		-130		-150	mA
I_{REF}	Reference Input Current	VEE = Max, VREF = -10V		10		10	μA
I_{IL}	Logic 0 Input Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		-1.0		-1.0	mA
		ECL Mode, V_{CC} = 0.0, V_{EE} = Max		-300		-300	μA
I_{IH}	Logic 1 Input Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		75		75	μA
		ECL Mode, V_{CC} = 0.0, V_{EE} = Max		350		350	μA
C_{OUT}	Output Capacitance	A_{OUT} to A_{GND} (Figure 2)		10		10	pF
C_{IN}	Digital Input Capacitance	Any Digital Input to D_{GND}		35		35	pF
R_{OUT}	Output Resistance	A_{OUT} to A_{GND} (Figure 2)	70	95	70	95	Ω

Note:

1. Return current from V_{EE} flows through AGND.

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AC Electrical Characteristics

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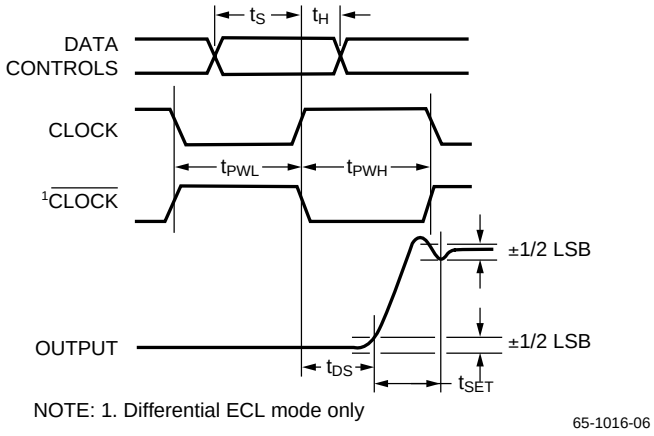
Symbol	Parameter	Test Conditions	Temperature Range				Unit
			Standard		Extended		
			Min.	Max.	Min.	Max.	
F_C	Maximum Data Rate	TTL Mode Full-Scale Output Step	20		20		MSPS
		ECL Mode Full-Scale Output Step	17.8		17.8		MSPS
t_{DS}	Data Turn on Delay	RL = 75 Ohms		30		30	ns
t_{SET}	Settling Time	TDC1016-8 to 0.2%		30		30	ns
		TDC1016-9 to 0.1%		35		35	ns
		TDC1016-10 to .05%		40		40	ns
t_{RV}	Output 10% to 90% Risetime	V_{EE} = Nom., RL = 75Ω, Full-Scale Step		5.5		5.5	ns

Timing Diagram



NOTE: 1. Differential ECL mode only

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Figure 1. Timing Diagram

System Performance Characteristics

Parameter		Test Conditions	Temperature Range				Unit
			Standard		Extended		
			Min.	Max.	Min.	Max.	
RES	Resolution	All TDC1016 Devices		10		10	Bits
ELI, ELD	Linearity Error Integral and Differential, Independent Based	TDC1016-8		0.2		0.2	% FS
		TDC1016-9		0.1		0.1	% FS
		TDC1016-10		0.075			% FS
V_{OFS}	Full-Scale Output Voltage	V_{EE} = Nom, RL ≥ 10kΩ, V_{REF} = -1.000V	-0.95	-1.05	-0.95	-1.05	V
V_{OZS}	Zero-Scale Output Voltage	V_{EE} = Nom, RL ≥ 10 kΩ, V_{REF} = -1.000V		±15		±15	mV
DP	Differential Phase	NTSC 4x Subcarrier[1]		1.0		1.0	Degrees
DG	Differential Gain	NTSC 4x subcarrier[1]		1.5		1.5	%
GE	Glitch Energy (Area)	RL = 50Ω, Midscale		125		125	pV-sec
GV	Glitch Voltage	RL = 50Ω, Midscale		35		35	mV

Note:

1. In excess of theoretical DP and DG due to quantizing error.

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Equivalent Circuits

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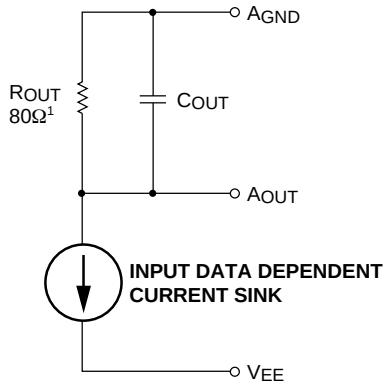

NOTE: 1. 75Ω requires outside trim

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Figure 2. Analog Output Equivalent Circuit, TTL and ECL Mode

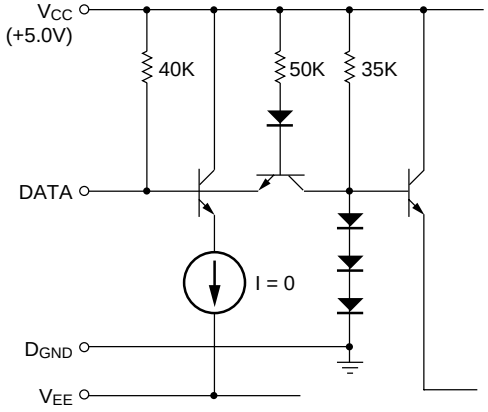

Figure 3. Digital Input Equivalent Circuit, TTL Mode

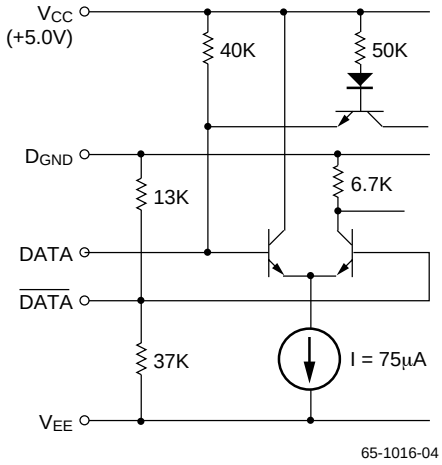

Figure 4. Digital Input Equivalent Circuit, ECL Mode

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Input Coding Table

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NDIS	N2C	NFH	NFL	Data	Output	Description
0	x	x	x	xxxxxxxxxx	0.0	Output Disabled
1 1	1 1	1 1	1 1	1111111111 0000000000	0.0 -1.0	Binary (Default State for TTL Mode Control) Inputs Open
1 1	1 1	0 0	0 0	1111111111 0000000000	-1.0 0.0	Inverse Binary
1 1	0 0	1 1	1 1	0111111111 1000000000	0.0 -1.0	Two's Complement
1 1	0 0	0 0	0 0	0111111111 1000000000	-1.0 0.0	Inverse Two's Complement
1 1	x x	0 1	1 0	xxxxxxxxxx xxxxxxxxxx	0.0 -1.0	Force HIGH Force LOW

Notes:

1. For TTL, 0.0 < V_{IL} < +0.8V is Logic 0.
2. For TTL, +2.0 < V_{IH} < +5.0V is Logic 1.
3. For ECL, -1.85 < V_{IL} < -1.67V is Logic 0.
4. For ECL, -1.0 < V_{IH} < -0.8V is Logic 1.
5. x = don't care.

Applications Discussion

Calibration

The TDC1016 is calibrated by adjusting the voltage reference to give the desired full-scale output voltage. The current switches can be turned on either by loading the data register with full-scale data or by bringing the NFH input to a logic zero. Note that all 10 current switches are activated by the NFH input and the resulting full-scale output voltage will be greater than if the system used only eight or nine bits for full-scale data.

Typical Application

The Typical Interface Circuit (Figure 5) shows the TDC1016 in a typical application, reconstructing video signals from digital data. Television timing signals, SYNC and BLANKING, are added by injecting current from the Wilson current source into a resistor divider circuit at the output of the TDC1016.

The TDC1016 output and currents from the SYNC and BLANKING inputs are summed and amplified by the HA2539 wide-band operational amplifier. Note the careful power supply decoupling at the power input pins of the amplifier. The output of the circuit is a composite video signal with SYNC and BLANKING levels coming from external sources. This technique allows the TDC1016 to use its entire dynamic range for the video information while pulses are added by other means.

The reference for the TDC1016 is generated by dividing the output voltage from a two-terminal band-gap voltage reference. System gain is calibrated by adjusting variable resistor R1. Analog and digital grounds should be routed back to system power supply ground by separate paths.

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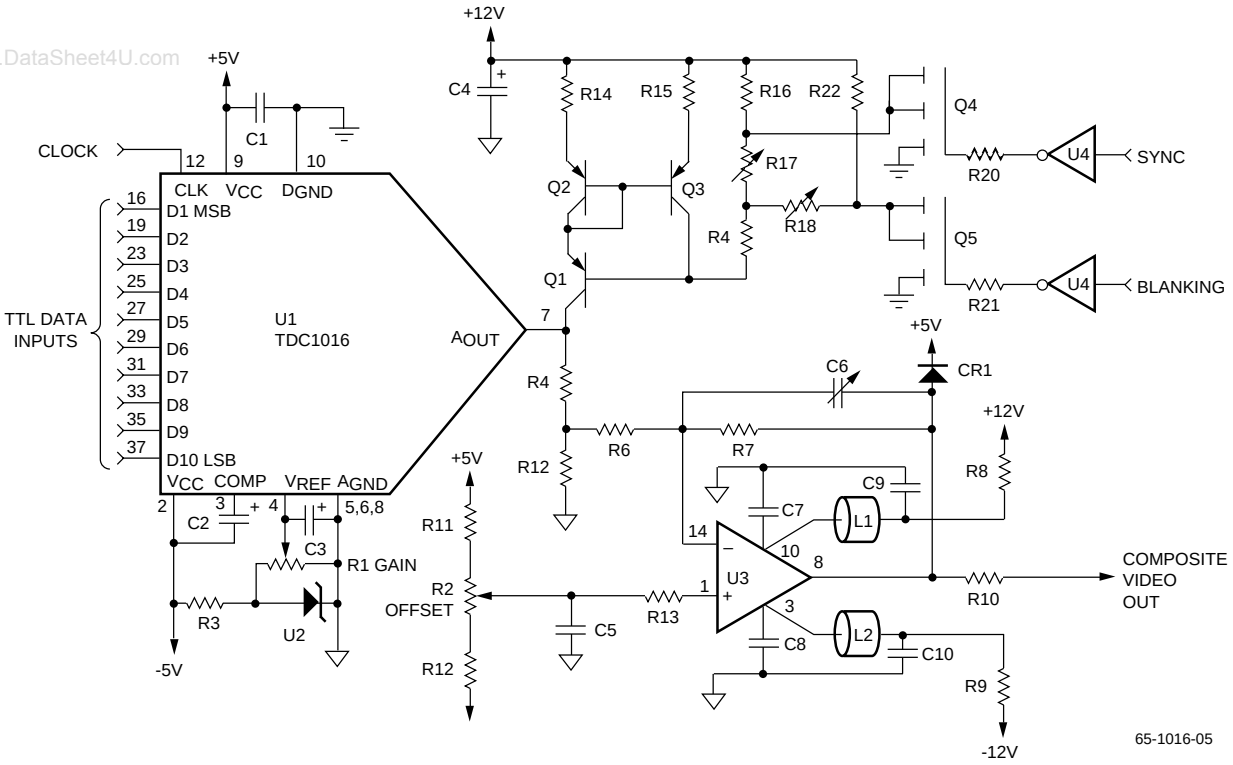

Figure 5. Typical Interface Circuit

Table 1. Bill of Materials

Resistors			
R1	5K	1/4W	10-turn
R2	1K	1/4W	10-tum
R3	1K	1/4W	5%
R4	43	1/4W	5%
R5	33	1/4W	5%
R6	330	1/4W	5%
R7	750	1/4W	5%
R8, R9	10	1/4W	5%
R10	75	1/4W	2%
R11, R12	10K	1/4W	5%
R13	220	1/4W	5%
R14, R15	100	1/4W	5%
R16, R22	390	1/4W	5%
R17, R18	2K	1/4W	10-turn
R19	1K	1/4W	5%
R20, R21	1K	1/4W	5%

Capacitors		
C1	0.01μF	50V
C2	1.0μF	10V
C3	1.0μF	10V
C4	2.2μF	25V
C5	0.1μF	50V
C6	2–5pF	50V
C7	0.1μF	50V
C8	0.1μF	50V
C9	0.1μF	50V
C10	0.1μF	50V

RF Chokes	
L1, L2	Ferrite Beads

Diodes	
CR1	1N4001

Transistors	
Q1	2N2907
Q2	2N2907
Q3	2N2907
Q4	2N6660
Q5	2N6660

Integrated Circuits	
U1	TDC1016
U2	LM113
U3	HA2539
U4	SN7404

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Mechanical Dimensions

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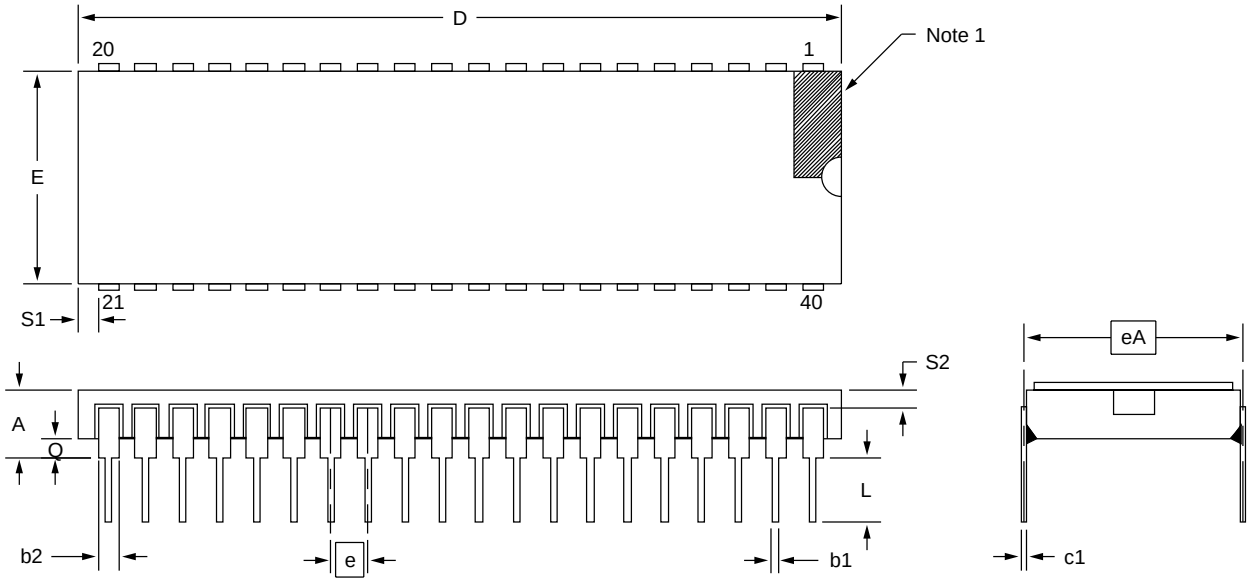
40 Lead Sidebrazed Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.120	.175	3.05	4.44	
b1	.014	.023	.360	.580	7
b2	.040	.065	1.02	1.65	2
c1	.008	.015	.200	.380	7
D	1.970	2.030	50.04	51.56	
E	.575	.610	14.60	15.49	
e	.100 BSC		2.54 BSC		4, 8
eA	.600 BSC		15.24 BSC		6
L	.125	.200	3.18	5.08	
Q	.025	.060	.63	1.52	3
S1	.005	—	.13	—	5
S2	.005	—	.13	—	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 20, 21, and 40 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 40.
5. Applies to all four corners (leads number 1, 20, 21, and 40).
6. "eA" shall be measured at the centerline of the leads.
7. All leads – Increase maximum limit by .003(.08mm) measured at the center of the flat when lead finish is applied.
8. Thirty-eight spaces.



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Mechanical Dimensions (continued)

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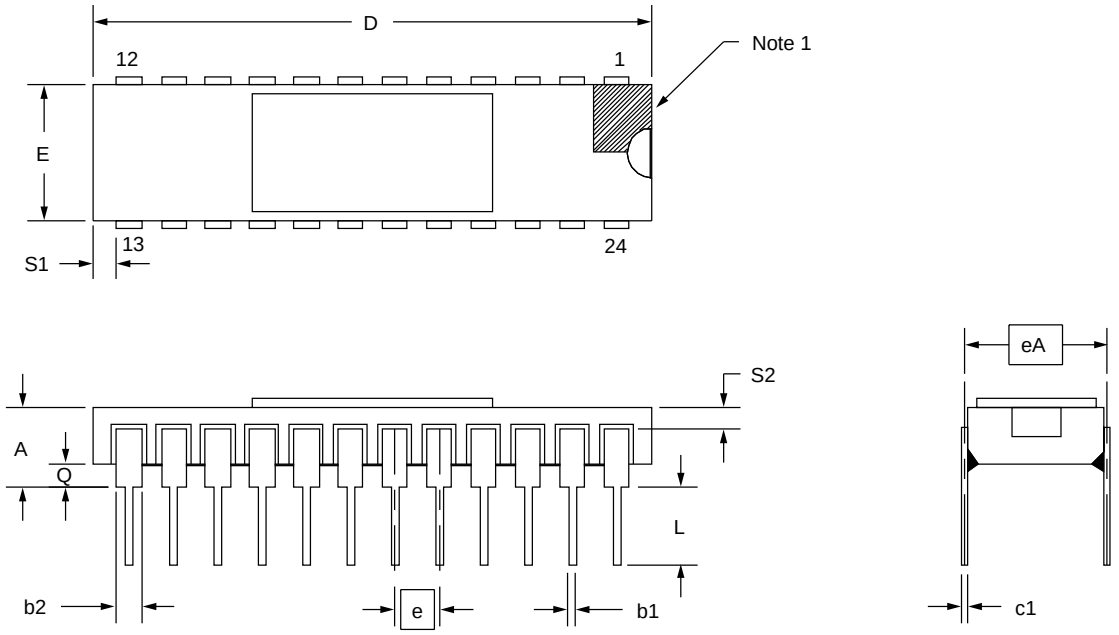
24 Lead Sidebrazed Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.120	.175	3.05	4.44	
b1	.014	.023	.360	.580	7
b2	.040	.065	1.02	1.65	2
c1	.008	.015	.200	.380	7
D	1.180	1.220	29.97	30.99	
E	.575	.610	14.60	15.49	
e	.100 BSC		2.54 BSC		4, 8
eA	.600 BSC		15.24 BSC		7
L	.125	.200	3.18	5.08	
Q	.025	.060	.630	1.52	3
S1	.005	—	.13	—	5
S2	.005	—	.13	—	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 12, 13, and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
5. Applies to all four corners (leads number 1, 12, 13, and 24).
6. "eA" shall be measured at the centerline of the leads.
7. All leads – Increase maximum limit by .003(.08mm) measured at the center of the flat when lead finish is applied.
8. Twenty-two spaces.



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Ordering Information

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Product Number	Temperature Range	Screening	Package	Package Marking
TDC1016J5CX	STD – T_A = 0°C to 70°C	Commercial	40 Pin Ceramic	1016J5CX
TDC1016J5AX	EXT – T_C = -55°C to 125°C	High Reliability	40 Pin Ceramic	1016J5AX
TDC1016J7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin Ceramic	1016J7CX
TDC1016J7AX	EXT – T_C = -55°C to 125°C	High Reliability	24 Pin Ceramic	1016J7AX

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