TDC1008

Use TMC2208 for New Designs

VLSI Multiplier–Accumulator

8 X 8 Bit, 100ns

The TDC1008 is a high-speed 8 x 8 bit parallel multiplier-accumulator which operates at a 100 nanosecond cycle time (10MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 16-bit product. Products may be accumulated to a 19-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), an 8-bit Most Significant Product (MSP), and an 8-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, LSP and MSP. The output register can be preloaded directly via the output ports.

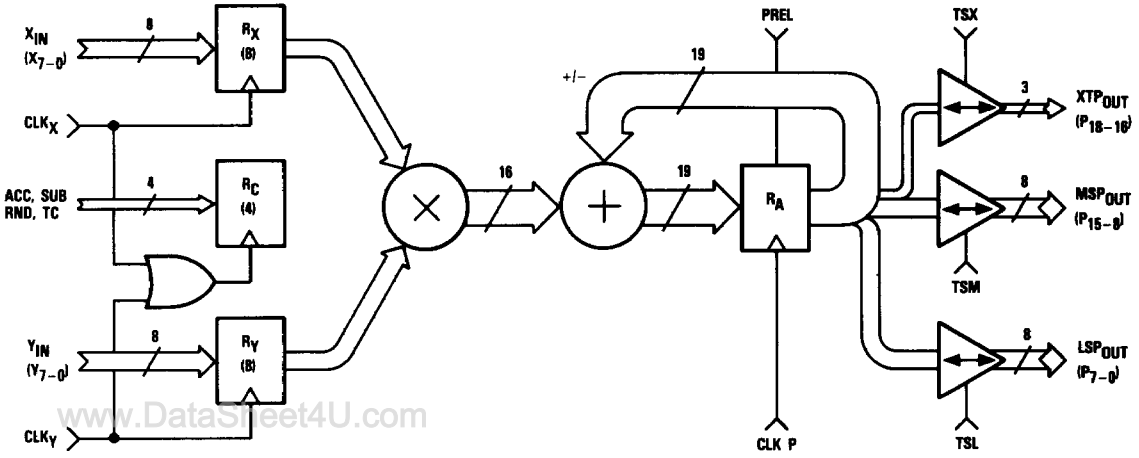
Features

- 100ns Multiply-Accumulate Time (Worst Case)
- 8 x 8 Bit Parallel Multiplication With Accumulation To 19-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Outputs
- Two's Complement Or Unsigned Magnitude Operation
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 48 Lead Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram

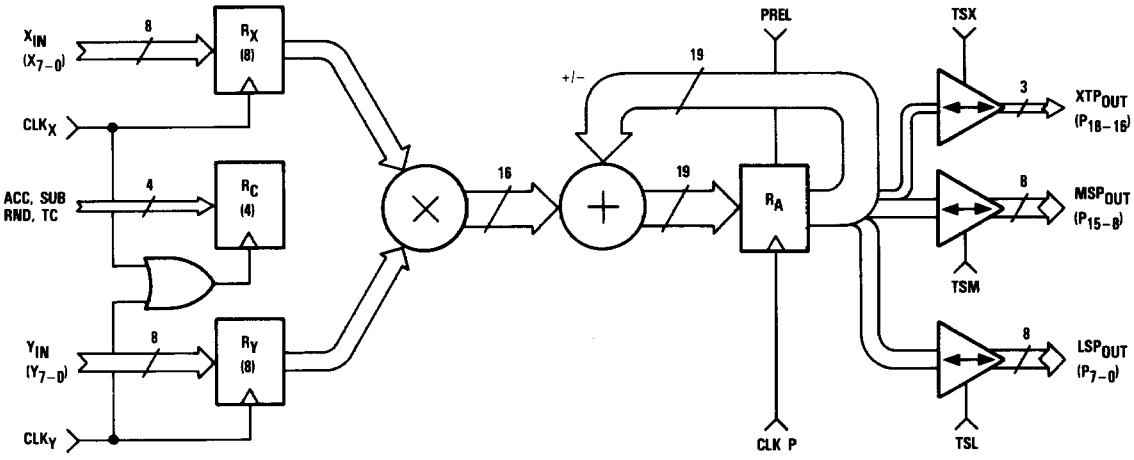


TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

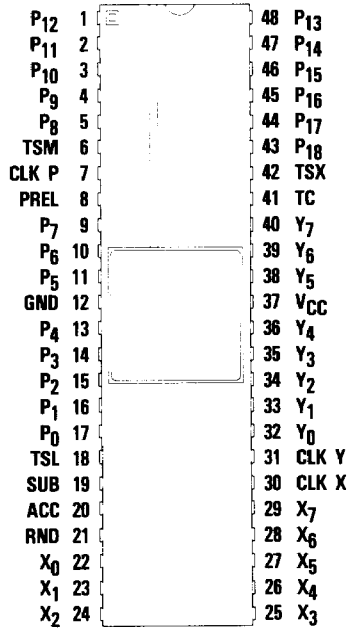
Phone: (619) 457-1000
Telex: 697-957
TWX: 910-335-1571

40G01343 Rev. C-4/88
Printed in the U.S.A.

Functional Block Diagram



Pin Assignments



48 Lead DIP – J4 Package

Functional Description

General Information

The TDC1008 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 8-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each input is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 8-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TDC1008 to be used on a bus, or allow the outputs to be multiplexed over the same 8-bit output lines.

Power

The TDC1008 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J4 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 37
GND	Ground	0.0V	Pin 12

Data Inputs

The TDC1008 has two 8-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_7 and Y_7, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_6 and Y_0 through Y_6 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J4 Package
X_7	X Data MSB	TTL	Pin 29
X_6		TTL	Pin 28
X_5		TTL	Pin 27
X_4		TTL	Pin 26
X_3		TTL	Pin 25
X_2		TTL	Pin 24
X_1		TTL	Pin 23
X_0	X Data LSB	TTL	Pin 22
Y_7	Y Data MSB	TTL	Pin 40
Y_6		TTL	Pin 39
Y_5		TTL	Pin 38
Y_4		TTL	Pin 36
Y_3		TTL	Pin 35
Y_2		TTL	Pin 34
Y_1		TTL	Pin 33
Y_0	Y Data LSB	TTL	Pin 32

Data Outputs

The TDC1008 has a 19-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 8-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J4 Package
P_{18}	Product MSB	TTL	Pin 43
P_{17}		TTL	Pin 44
P_{16}		TTL	Pin 45
P_{15}		TTL	Pin 46
P_{14}		TTL	Pin 47
P_{13}		TTL	Pin 48
P_{12}		TTL	Pin 1
P_{11}		TTL	Pin 2
P_{10}		TTL	Pin 3
P_9		TTL	Pin 4
P_8		TTL	Pin 5
P_7		TTL	Pin 9
P_6		TTL	Pin 10
P_5		TTL	Pin 11
P_4		TTL	Pin 13
P_3		TTL	Pin 14
P_2		TTL	Pin 15
P_1		TTL	Pin 16
P_0	Product LSB	TTL	Pin 17

Clocks

The TDC1008 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers is loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J4 Package
CLK X	Clock Input Data X	TTL	Pin 30
CLK Y	Clock Input Data Y	TTL	Pin 31
CLK P	Clock Product Register	TTL	Pin 7

Controls

The TDC1008 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW, and PRELoad is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs unsigned magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and their sum is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J4 Package
TSX	XTP Three-State Control	TTL	Pin 42
TSM	MSP Three-State Control	TTL	Pin 6
TSL	LSP Three-State Control	TTL	Pin 18
PREL	Preload Control	TTL	Pin 8
RND	Round Control Bit	TTL	Pin 21
TC	Two's Complement Control	TTL	Pin 41
ACC	Accumulate Control	TTL	Pin 20
SUB	Subtract Control	TTL	Pin 19

Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register→ Output pin	Register→ Output pin	Register→ Output pin
L	L	L	H	Register→ Output pin	Register→ Output pin	Hi-Z
L	L	H	L	Register→ Output pin	Hi-Z	Register→ Output pin
L	L	H	H	Register→ Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register→ Output pin	Register→ Output pin
L	H	L	H	Hi-Z	Register→ Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register→ Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Figure 1. Fractional Two's Complement Notation

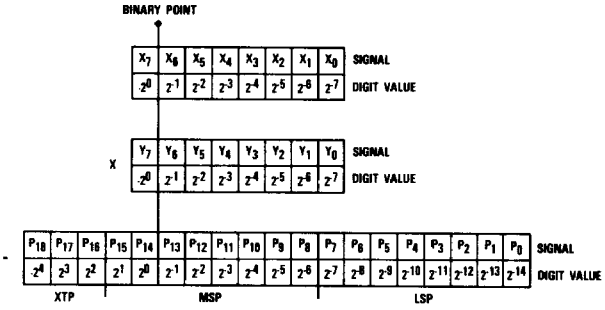


Figure 2. Fractional Unsigned Magnitude Notation

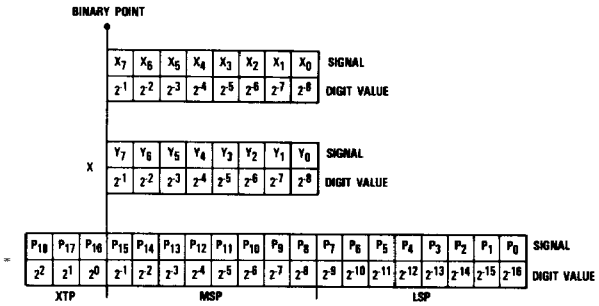


Figure 3. Integer Two's Complement Notation

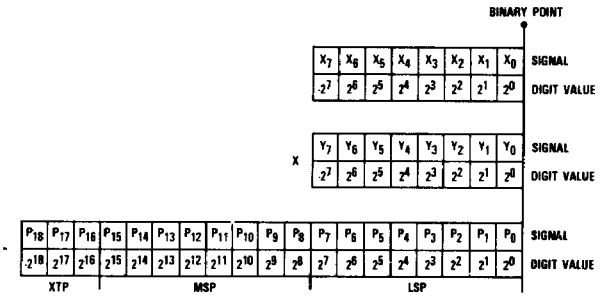
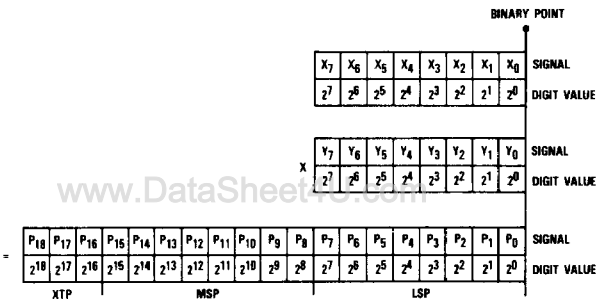


Figure 4. Integer Unsigned Magnitude Notation



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to + 6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Setup Time (Except PREL)	25			30			ns
t_S	Input Setup Time (PREL)	40			45			ns
t_H	Input Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static		450		525	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		Data, Registered Controls		−0.4		−0.4	mA
		Clocks, Unregistered Controls		−1.0		−1.0	mA
		CLK P		−2.0		−2.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		Data, Registered Controls		75		100	μA
		Clocks, Unregistered Controls		75		100	μA
		CLK P		150		200	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		−400		−400	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		75		100	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{CC} = MIN		100		125	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1}[2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Figure 5. Timing Diagram

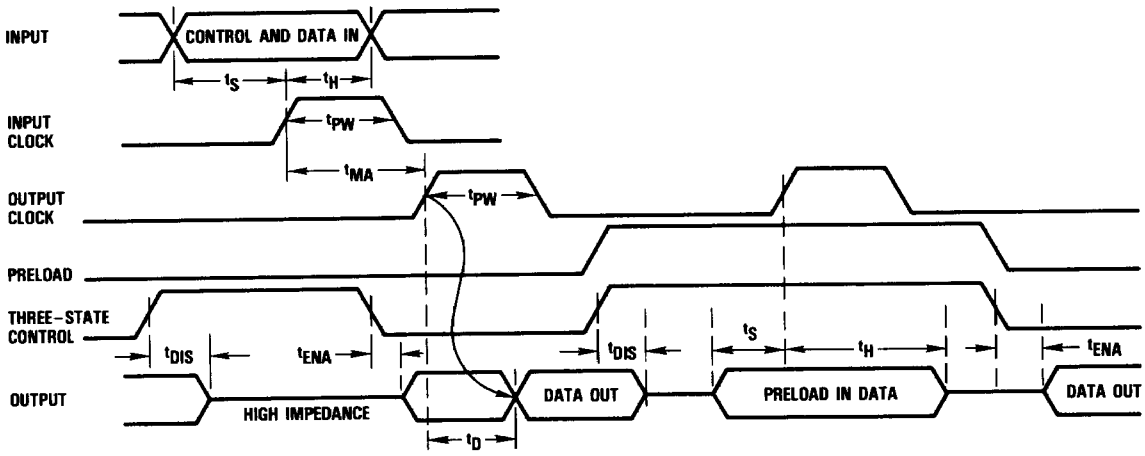
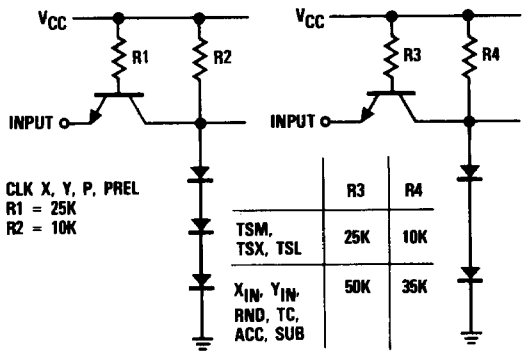


Figure 6. Equivalent Input Circuit



	R3	R4
TSM, TSX, TSL	25K	10K
X_{IN}, Y_{IN}, RND, TC, ACC, SUB	50K	35K

Figure 7. Equivalent Output Circuit

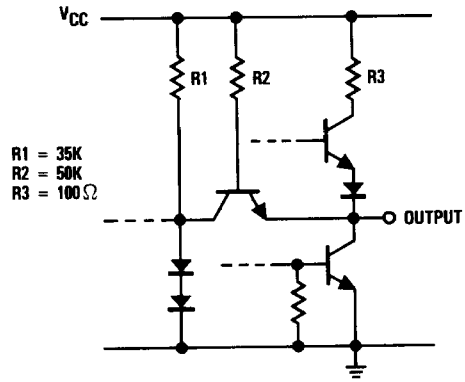


Figure 8. Test Load

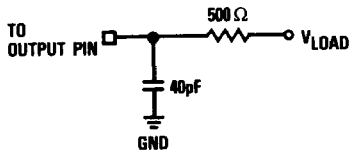
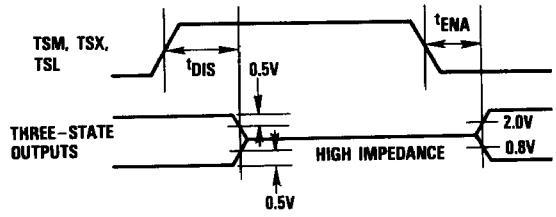


Figure 9. Transition Levels For Three-State Measurements



Application Notes

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and the desired register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TDC1008 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1008J4C	STD-T_A = 0°C to 70°C	Commercial	48 Lead DIP	1008J4C
TDC1008J4G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	48 Lead DIP	1008J4G
TDC1008J4A	EXT-T_C = -55°C to 125°C	High Reliability[1]	48 Lead DIP	1008J4A

Note:

1. Per TRW document 70Z1757.