TDA8921TH class-D audio amplifier 2 x 50W single chip

1. General description

The TDA8921 is an high efficiency class-D audio power amplifier system. Typical output power is 2 x 50 W and it operates with high efficiency and very low dissipation. The devices comes in a HSOP24 power package with a small internal heatsink. No external heatsink is required, or depending on supply voltage and load a very small one. The system operates over a wide supply voltage range from ±15 up to =±30 V and consumes a very low quiescent current.

2. Features

- High efficiency (>90%)
- Operating voltage from ±15 V to ± 30V
- Very low quiescent current
- Low distortion
- Fixed gain of 30 dB in Single Ended and 36 dB in BTL
- High output power
- Good ripple rejection
- Internal switching frequency can be overruled by an external clock
- No switch-on or switch-off plop noise
- Short-circuit proof across the load
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Electrostatic discharge protection (pin to pin)
- Thermally protected

3. Applications

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters)

4. Quick reference data

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General, V_p = ± 25V						
V_p	operating supply voltage		±15	±25	±30	V
$I_{q(tot)}$	total quiescent current		-	55	75	mA
η	efficiency	P_o = 30 W	-	90	-	%
Stereo single-ended configuration						
P_o	output power, R_{LOAD} = 8 ohm	THD = 10%, Vp= ± 25 V	30	37	-	W
P_o	output power, R_{LOAD} = 4 ohm	THD = 10%, Vp= ± 21 V	40	50	-	W
G_v	closed loop voltage gain		29	30	31	dB
$\lvert Z_i \rvert$	input impedance		45	68	-	kΩ
$V_{n(o)}$	noise output voltage		-	200	400	µV
SVRR	supply voltage ripple rejection		40	50	-	dB
α_{cs}	channel separation		-	65	-	dB
|Vo|	DC output offset voltage			0	150	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mono Bridge-Tied load configuration						
P_o	output power, R_{LOAD} = 8 ohm	THD = 10%, Vp= ± 21 V	80	100	-	W
G_v	closed loop voltage gain		35	36	37	dB
$\|Z_i\|$	input impedance		23	34	-	kΩ
$V_{n(o)}$	noise output voltage		-	280	-	μV
SVRR	supply voltage ripple rejection		-	44		dB
|Vo|	DC output offset voltage			0	200	mV

5. Ordering information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8921TH	HSOP24	heatsink small outline package; 24 leads	SOT566BB1C

6. Block diagram digital power stage

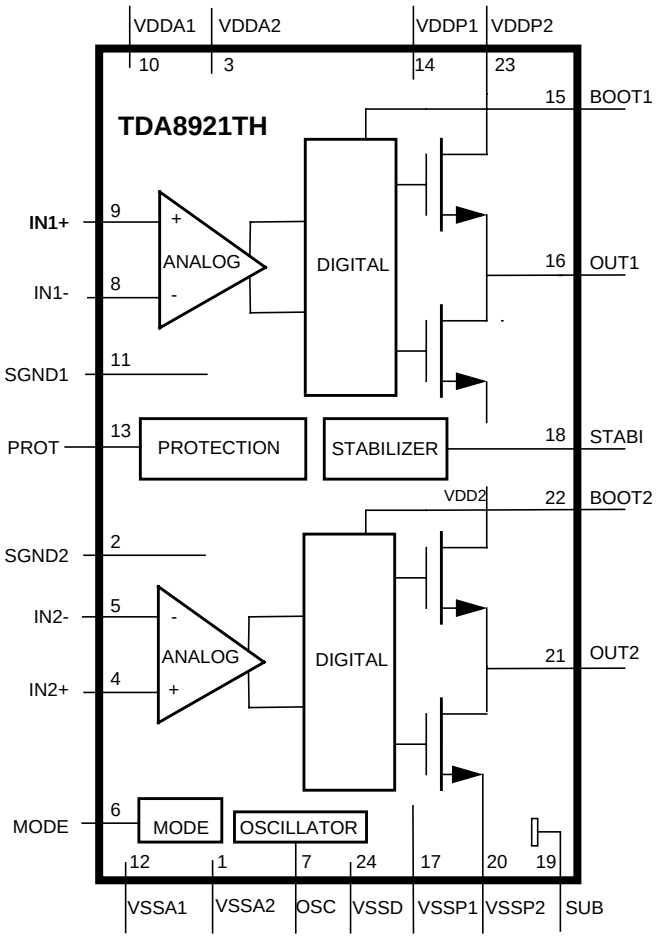


Figure 1 Block diagram

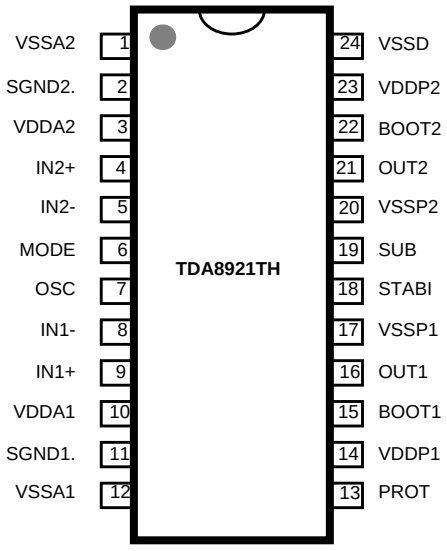


Figure 2 Pin configuration

7. Pinning

SYMBOL	PIN	DESCRIPTION
VSSA2	1	Negative analog supply channel 2
SGND2	2	Signal ground channel 2
VDDA2	3	Positive analog supply channel 2
IN2+	4	Positive audio input channel 2
IN2-	5	Negative audio input channel 2
MODE	6	Mode select input (standby/mute/operating)
OSC	7	Oscillator frequency adjustment, or tracking input
IN1-	8	Negative audio input channel 1
IN1+	9	Positive audio input channel 1
VDDA1	10	Positive analog supply channel 1
SGND1	11	Signal ground channel 1
VSSA1	12	Negative analog supply channel 1
PROT	13	Time constant capacitor for protection delay
VDDP1	14	Positive power supply channel 1
BOOT1	15	Bootstrap capacitor channel 1
OUT1	16	PWM output channel 1
VSSP1	17	Negative power supply channel 1
STABI	18	Decoupling internal stabilizer for logic supply
SUB	19	Substrate, must be connected to negative supply
VSSP2	20	Negative power supply channel 2
OUT2	21	PWM output channel 2
BOOT2	22	Bootstrap capacitor channel 2
VDDP2	23	Positive power supply channel 2
VSSD	24	Negative digital supply

8. Functional description

The TDA8921TH is a two channel audio power amplifier system using the class-D technology. In the analog controller part the analog audio input signal is converted into a digital PWM signal. For driving the low pass filter and the loud-speaker load a digital power stage is used. It performs a level shift from the low power digital PWM signal at logic levels to a high power PWM signal switching between the main supply lines. A second order low pass filter converts the PWM signal to an analog audio signal across the loudspeaker.

Digital power stage

It contains the high power D-MOS switches, the drivers, timing and handshaking between the power switches and some control logic. For protection a temperature sensor and a maximum current detector is on the chip.

Analog low power controller

For the two audio channels it contains two pulse width modulators (PWM), two analog feedback loops and two differential input stages. Furthermore it contains circuits common to both channels like the oscillator, all reference sources, the mode functionality and a digital timing manager.

Using this chip an audio system with two independent amplifier channels with high output power, high efficiency (90%), low distortion and a low quiescent current is obtained. The amplifiers channels can be connected in the following configurations:

- Mono bridge-tied load (BTL) amplifier
- Stereo single-ended (SE) amplifiers.

The amplifier system can be switched in three operating modes with the MODE select pin:

- Standby mode, with a very low supply current.
- Mute mode, the amplifiers are operational, but the audio signal at the output is suppressed.
- Operating mode (amplifier fully operational) with output signal.

For suppressing pop noise the amplifier will remain automatically for approx. 220ms in the mute mode before switching to operating. In this time the coupling capacitors at the input are fully charged. See fig. 5 for an example of a switching circuit for driving the mode pin.

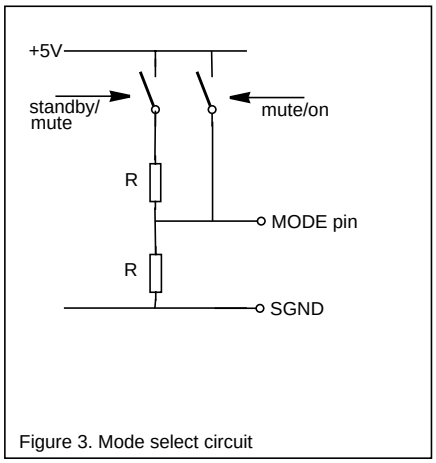


Figure 3. Mode select circuit

Pulse Width Modulation (PWM) frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approx. 350 kHz. Using a second order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. This switching frequency is fixed by an external resistor R_{OSC} connected between pin OSC and VSS. With the resistor value given in the schematic of the reference design, the carrier frequency is typical 350 kHz. The carrier frequency can be calculated using:

$$f_{osc} = 9 \times 10^9 / R_{osc} \text{ [Hz]}$$

If two or more class-D systems are used in the same audio application, it is advised to have all devices working at the same switching frequency. This can be realized by connecting all OSC pins together and feed them from a external central oscillator. Using an external oscillator it is necessary to force the OSC pin to a DC-level above SGND for switching form internal to external oscillator. In this case the internal oscillator is disabled and the PWM will be switching on the external frequency.The frequency range of the external oscillator must be in the range as specified in the switching characteristics.

Application in a practical circuit:

Internal oscillator: R_{osc} connected from OSC pin to V_{SS}

external oscillator: connect oscillator signal between OSC pin and SGND pin; delete R_{osc}

Protections

Temperature-, supply voltage- and short circuit protections sensors are included on the chip. In case of exceeding the maximum current or maximum temperature the system shuts down. The protection is activated in case of:

1. Over-temperature

If the junction temperature (Tj) exceeds 150°C, then the power stage shuts down immediately. The power stage starts switching again if the temperature is dropped to approx. 130°C, so there is a hysteresis of approx. 20°C.

2. Short-circuit across the loudspeaker terminals:

When the loudspeaker terminals are short-circuited it will be detected by the current protection. If the output current exceeds the maximum output current of 5 Amp, then the power stage shuts down within less than1µs and the high current is switched off. In this state the dissipation is very low. Every 220ms the system tries to restart again. If there is still a short across the loudspeaker load, the system is switched off again as soon as the maximum current is exceeded.The average dissipation will be low because of this low duty cycle.

3. Start-up safety test
During the start-up sequence, when the mode pin is switched from standby to mute, the condition at the output terminals of the power stage are checked. In case of a short of one of the output terminals to V_{DD} or V_{SS} the start-up procedure is interrupted and the systems waits for un-shorted outputs. Because the test is done before enabling the power stages, no large currents can be flowing in case of a short circuit. This system protects for shorts at both sides of the output filter to both supply lines. When there is a short from the power PWM output of the power stage to one of the supply lines - so before the demodulation filter - it will also be detected by the 'start-up safety test. Practical use from this test feature can be found in detection of shorts on the pcb.
Remark: this test is only operational prior or during the start-up sequence, so not during normal operation.

4. Supply voltage alarm
If the supply voltage goes below the value of ± 12.5V the under voltage protection is activated and system shuts down correctly and silently without plopnoises. When the supply voltage comes above the threshold the system is restarted again after 220ms. If the supply voltage exceeds ± 32V the overvoltage protection is activated and the power stages shuts down. They are enabled again as soon as the supply voltage drops down the threshold.
Additional there is balance protection which compares the positive (Vdd) and the negative (Vss) supply voltages and triggers if the voltage difference between them exceeds a certain level. This level is dependent on the sum of both supply voltages. Example: the protection is triggered if Vdd = +25V and Vss = -30V.

Differential audio inputs

For a high common mode rejection and a maximum of flexibility of application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the channels is inverted, so that a load can be connected between the two output filters. In this case the system operates as a mono BTL amplifier and with the same loudspeaker impedance a four times higher output power can be obtained. For more information see the application information.
Also in the stereo single ended configuration it is recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies.

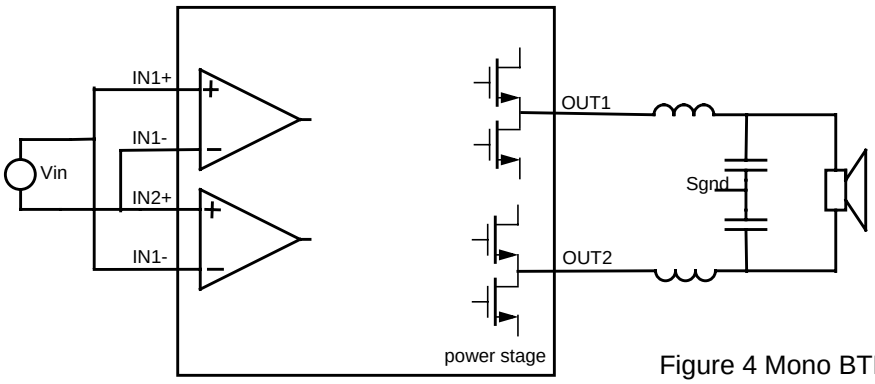


Figure 4 Mono BTL application

9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_p	supply voltage		–	±30	V
V_{ms}	mode select switch voltage	with respect to SGND	–	5.5	V
V_{sc}	short circuit voltage of output pins		–	±30	V
I_{ORM}	repetitive peak current in output pin		–	5	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C

10. Thermal characteristics

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c}$	thermal resistance from junction to case		2 *)	K/W

*) Under investigation

11. Static characteristics

V_p = ±25 V; T_{amb} = 25 °C; measured in Fig. 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_p	supply voltage range	(1)	±15	±25	±30	V
I_q	quiescent current	no load connected	-	55	75	mA
I_{stb}	standby current		-	200	500	µA
Mode select pin; see Fig. 5						
V_{ms}	input voltage range	(2)	0	-	5.5	V
I_{ms}	input current	V_{ms} = 5.5 V	-	-	1000	µA
V_{th1+}	threshold voltage	standby → mute; (2)	-	1.6	2.0	V
V_{th1-}	threshold voltage	mute → standby; (2)	0.8	1.0	-	V
$V_{ms}H1$	hysteresis $\lvert(V_{th1+}) - (V_{th1-})\rvert$		-	600	-	mV
V_{th2+}	threshold voltage	mute → on; (2)	-	3.8	4.0	V
V_{th2-}	threshold voltage	on → mute; (2)	3.0	3.2	-	V
$V_{ms}H2$	hysteresis $\lvert(V_{th2+}) - (V_{th2-})\rvert$		-	600	-	mV
Audio input pins						
$V_{in}DC$	DC input level	(2)		0		V
Amplifier outputs						
$\lvert V_{OO}\rvert$	output offset voltage	on and mute (2)	-	-	150	mV
$\lvert \Delta V_{OO}\rvert$	delta output offset voltage	on ↔ mute (2)	-	-	80	mV
Stabilizer 12V						
V_{stabi}	Stabilizer output voltage	mute and operating (3)	11	13	15	V
$I_{stabi\ max}$	Stabilizer max. output current	mute and operating	10			mA

Notes

1. The circuit is DC adjusted at V_p = ±15 to ±30 V.
2. With respect to SGND (0 V).
3. With respect to V_{SS}

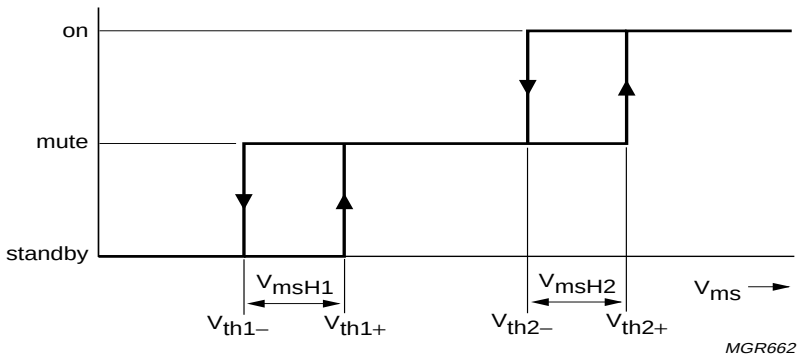


Fig. 5 Mode select pin

12. Switching characteristics

V_p = ±25 V; T_{amb} = 25 °C; measured in Fig. 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching frequency						
f_{oscTYP}	typical oscillator frequency	R_{OSC} = 30.0 kohm	309	317	329	kHz
f_{oscTYP}	typical oscillator frequency	R_{OSC} = 27 kohm, see reference design		360		kHz
f_{osc}	oscillator frequency range	Note 1	210		600	kHz
V_{OSC}	maximum voltage at OSC pin	frequency tracking			SGND+ 12	V
V_{OSC_trip}	Triplevel at OSC pin for tracking	frequency tracking	-	SGND+ 2.5	-	V
f_{track}	frequency range for tracking	frequency tracking	210		600	kHz
V_{OSC}^{EXT}	Amplitude at OSC pin for tracking	Note 2	tbf	-	tbf	V
PWM output						
t_r	rise time output voltage		-	30	-	ns
t_f	fall time output voltage		-	30	-	ns
t_{blank}	blanking time		-	40	-	ns
t_{min}	minimal pulse width	note 3	-	190	240	ns
R_{ds_on}	R_{DS_ON} output transistors		-	0.2	0.3	ohm

Note 1: frequency set with Rosc, according to formula in functional description

Note 2: for tracking the external oscillator has to switch around (SGND+2.5V) with a minimum amplitude of V_{OSC}^{EXT}

Note 3: The effective minimal pulse width during clipping is $t_{min}/2$

For the practical useable minimal and maximal duty cycle which determines the maximum output power:

$$(t_{min} \cdot f_{osc} / 2) \cdot 100\% \ < \ \text{duty cycle} \ < \ (1 - (t_{min} \cdot f_{osc}) / 2) \cdot 100\%$$

Using the typical values:

$$3.5\% \ < \ \text{duty cycle} \ < \ 96.5\%$$

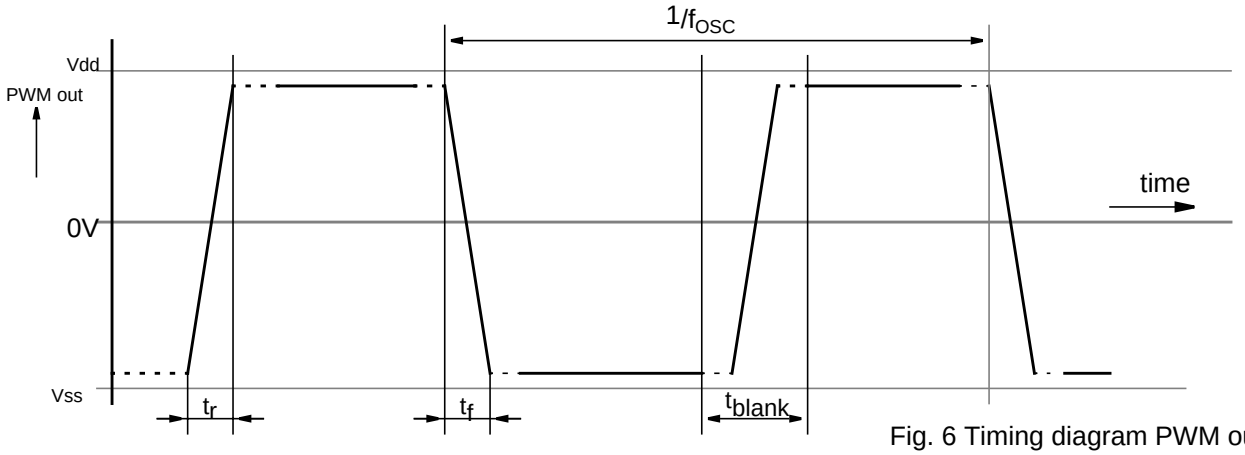


Fig. 6 Timing diagram PWM output

13. Dynamic AC characteristics

Single ended application

V_p = ±25 V; R_L = 8 Ω; f_i = 1 kHz; T_{amb} = 25 °C; measured in Fig. 9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power, R_{LOAD} = 8 ohm	V_p = ±25 V; THD = 0.5%	25 *)	30	-	W
		V_p = ±25 V; THD = 10%	30 *)	37	-	W
	output power, R_{LOAD} = 4 ohm	V_p = ±21 V; THD = 0.5%	30 *)	40	-	W
		V_p = ±21 V; THD = 10%;	40 *)	50	-	W
	output power, R_{LOAD} = 8 ohm	V_p = ±30 V; THD = 0.5%;	-	40	-	W
		V_p = ±30 V; THD = 10%;	-	52	-	W
THD	total harmonic distortion	P_o = 1 W; note 1				
		f_i = 1 kHz	-	0.01	0.05	%
		f_i = 10 kHz	-	0.1	-	%
G_v	closed loop voltage gain		29	30	31	dB
η	efficiency	P_o = 30 W; f_i = 1 kHz; note 2	85	90	-	%
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 3	-	55	-	dB
		on; f_i = 1 kHz; note 4	40	50	-	dB
		mute; f_i = 100 Hz; note 3	-	55	-	dB
		standby; f_i=100 Hz; note 3	-	80	-	dB
$\|Z_i\|$	input impedance		45	68		kΩ
$V_{n(o)}$	noise output voltage	on; R_S = 0 Ω; note 5	-	220	400	μV
		on; R_S = 10 kΩ; note 6	-	230	-	μV
		mute; note 7	-	220	-	μV
α_{cs}	channel separation	note 8	-	70	-	dB
$\|\Delta G_v\|$	channel unbalance		-	-	1	dB
V_o	output signal in mute	note 9	-	-	400	μV
CMRR	common mode rejection ratio	$V_{i(CM)(rms)}$ = 1 V	-	75	-	dB

Note *) indirect measurement based on Rds_on measurement

Notes

1. Total Harmonic Distortion is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a lower order lowpass filter a significant higher value will be found, due to the switching frequency outside the audio band.
2. Output power measured across the loudspeaker load.
3. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 100 Hz; R_S = 0 Ω.
4. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 1 kHz; R_S = 0 Ω.
5. B = 22 Hz to 22 kHz; R_S = 0 Ω.
6. B = 22 Hz to 22 kHz; R_S = 10 kΩ.
7. B = 22 Hz to 22 kHz; independent of R_S.
8. P_o = tbf W; R_S = 0 Ω.
9. $V_i = V_{i(max)}$ = 1 V (RMS).

Mono BTL application

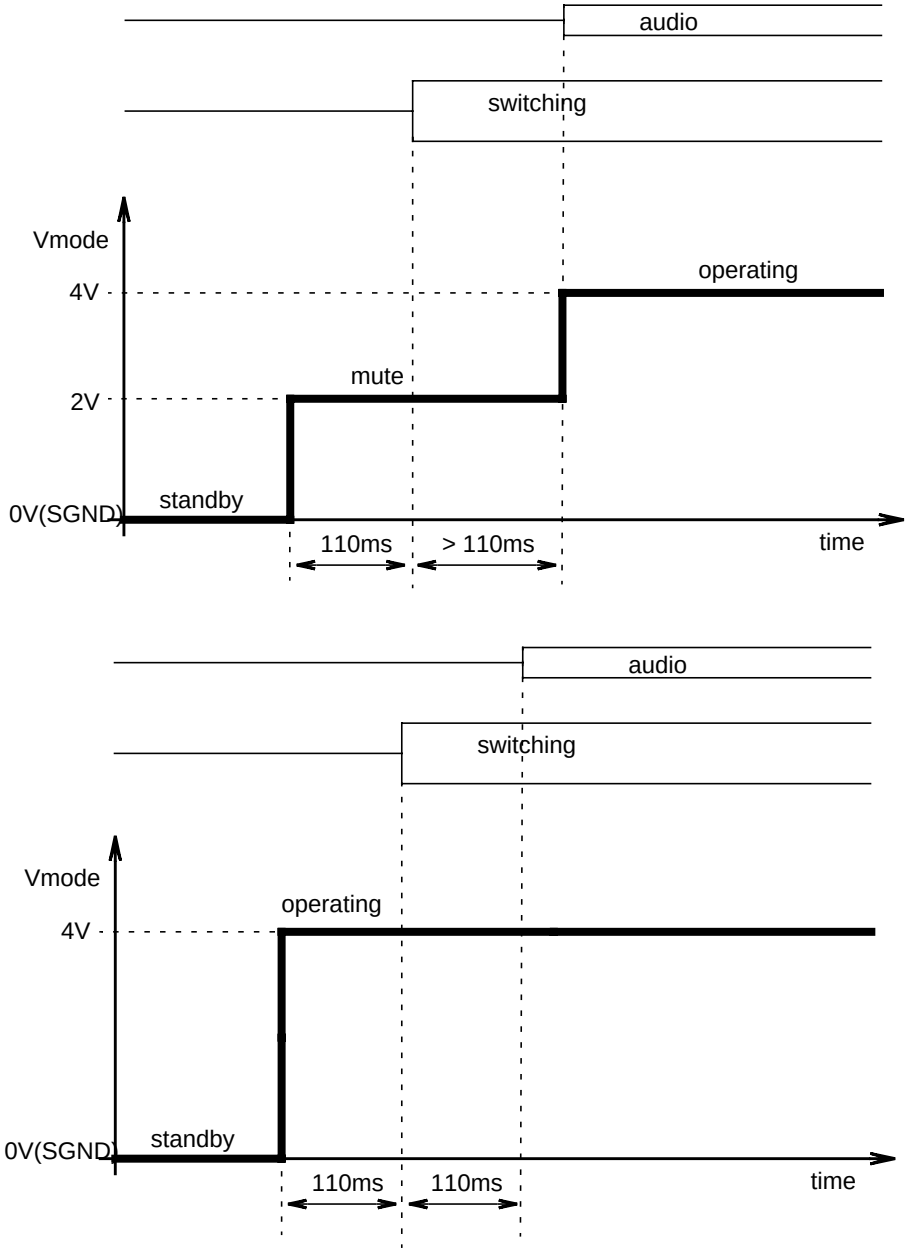
V_p = ±**21** V; f_i = 1 kHz; T_{amb} = 25 °C; measured in Fig. tbf; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power, R_{LOAD} = 8 ohm	V_p = ± 21V; THD = 0.5%	70 *)	80	-	W
		V_p = ± 21V; THD = 10%	80 *)	100	-	W
THD	total harmonic distortion	P_o = 1 W; note 1				
		f_i = 1 kHz	-	0.01	0.05	%
		f_i = 10 kHz	-	0.1	-	%
G_v	closed loop voltage gain		35	36	37	dB
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 3	-	49	-	dB
		on; f_i = 1 kHz; note 4	36	44	-	dB
		mute; f_i = 100 Hz; note 3	-	49	-	dB
		standby; f_i=100 Hz; note 3	-	80	-	dB
$\|Z_i\|$	input impedance		22	34		kΩ
$V_{n(o)}$	noise output voltage	on; R_S = 0 Ω; note 5	-	280	500	μV
		on; R_S = 10 kΩ; note 6	-	300	-	μV
		mute; note 7	-	280	-	μV
V_o	output signal in mute	note 8	-	-	500	μV
CMRR	common mode rejection ratio	$V_{i(CM)(rms)}$ = 1 V	-	75	-	dB

Notes

1. Total Harmonic Distortion is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a low order lowpass filter a significant higher value will be found, due to the switching frequency outside the audio band.
2. Output power measured across the loudspeaker load.
3. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 100 Hz; R_S = 0 Ω.
4. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 1 kHz; R_S = 0 Ω.
5. B = 22 Hz to 22 kHz; R_S = 0 Ω.
6. B = 22 Hz to 22 kHz; R_S = 10 kΩ.
7. B = 22 Hz to 22 kHz; independent of R_S.
8. $V_i = V_{i(max)}$ = 1 V (RMS).

*) indirect measured, based on Rds_on measurement



When switching from standby to mute there is a delay of 110ms before the output starts switching.
Audio signal is available after the mode pin has been set to operating, but not earlier than 220ms after switching to mute.

When switching from standby to operating there is a first delay of 110ms before the outputs starts switching.
After a second delay of 110ms the audio signal is available

Figure 7. Mode pin timing

14. Test information

To be finished

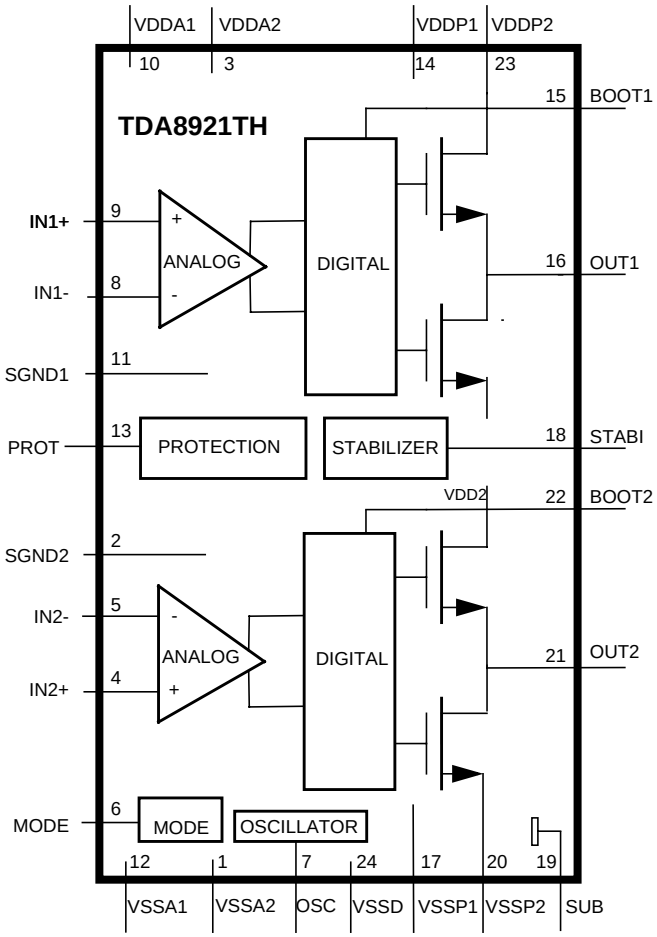


Figure 8. Test circuti

15. Application information

Reference design

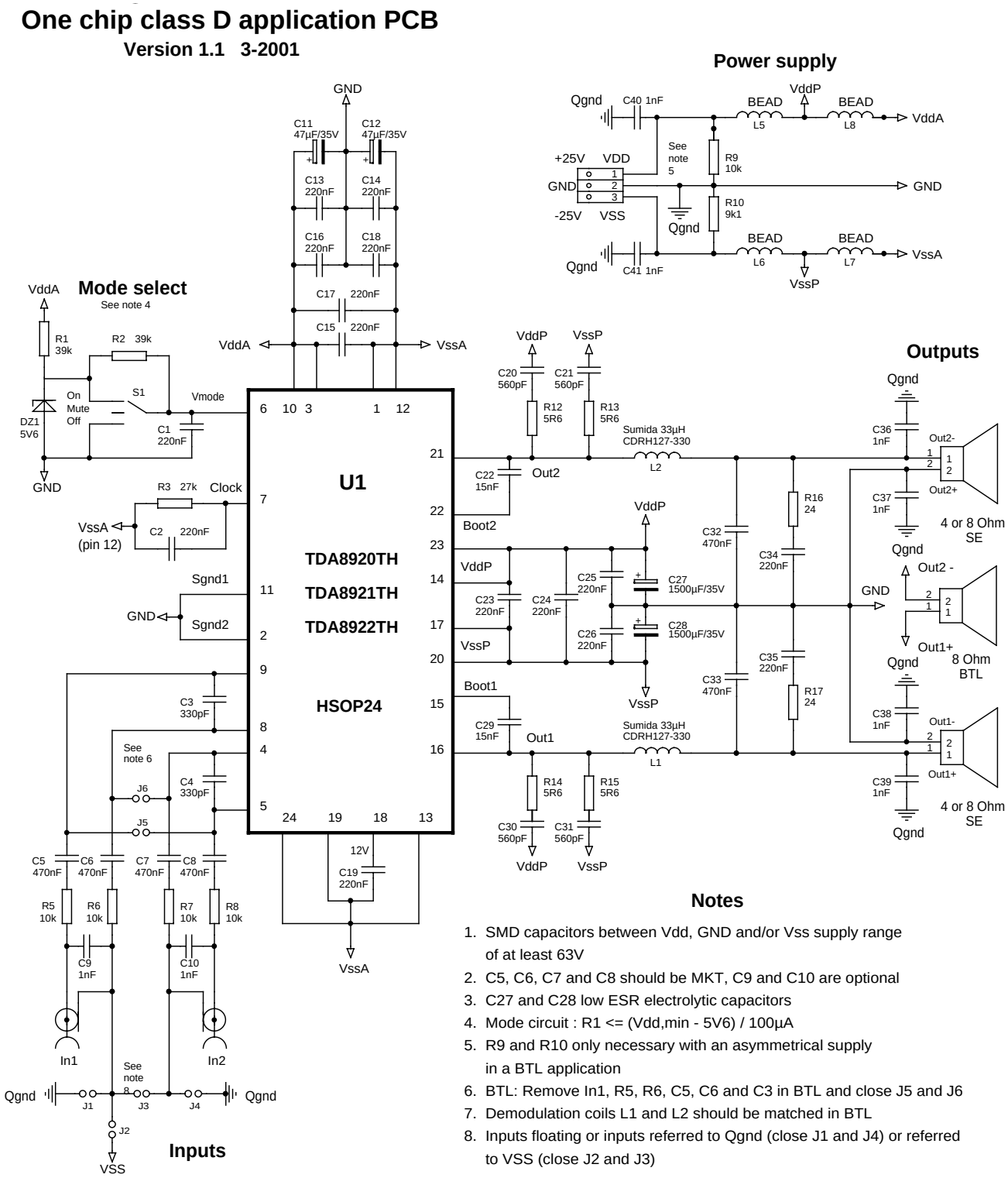


Fig.9 Application circuit for stereo single-ended application

BTL application
For using the system in mono BTL application (for more output power), the inputs of both channels must be connected in parallel. The phase of one the inputs must be inverted. In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

MODE pin
For correct operation the switching voltage at the mode pin should be de-bounced. If the mode pin is driven by a mechanical switch an appropriate debouncing low pass filter should be used. If the mode pin is driven by an electronic circuit or micro controller then it should remain for at least 100ms at the mute voltage level (V_{th1+}) before switching back to the standby voltage level.

External clock
See Fig. 10 for a external clock oscillator circuit.

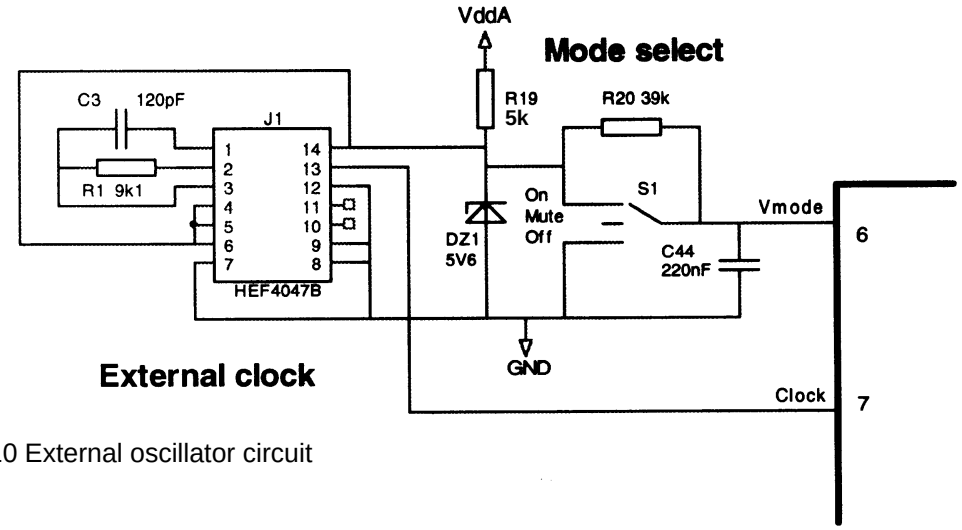


Fig.10 External oscillator circuit

Output power
The output power in several applications can be estimated using:

$$\text{for single ended:} \quad P_{out\_1\%} = \frac{\left(\frac{R_{LOAD}}{R_{LOAD} + R_{DS\_ON} + R_S} \cdot Vp \left(1 - t_{min} \cdot f_{osc} \right) \right)^2}{2 \cdot R_{Load}}$$

$$\text{the maximum current : } I_{out\hat{}} = \frac{Vp \left(1 - t_{min} \cdot f_{osc} \right)}{R_{LOAD} + R_{DS\_ON} + R_S} \quad \text{should not exceed 5 Amp}$$

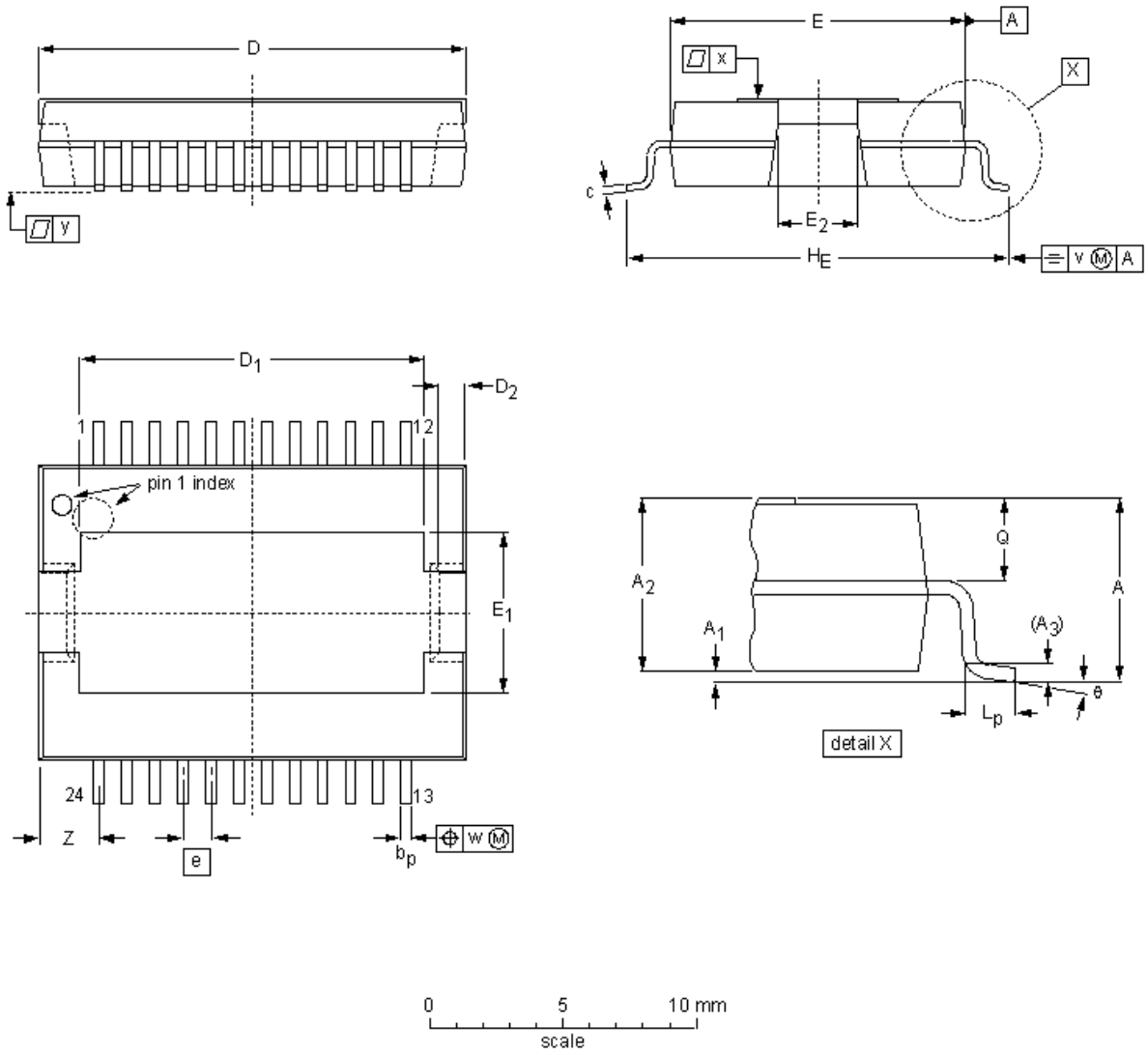
$$\text{for BTL} \quad : \quad P_{out\_1\%} = \frac{\left(\frac{R_{LOAD}}{R_{LOAD} + 2 \left(R_{DS\_ON} + R_S \right)} \cdot 2Vp \left(1 - t_{min} \cdot f_{osc} \right) \right)^2}{2 \cdot R_{Load}}$$

$$\text{the maximum current : } I_{out\hat{}} = \frac{2\,Vp \left(1 - t_{min} \cdot f_{osc} \right)}{R_{LOAD} + 2 \left(R_{DS\_ON} + R_S \right)} \quad \text{should not exceed 5 Amp}$$

While:
R_{LOAD} =Load impedance
Rs =Serie resistance of filter coil
Pout_1% =Output power just at clipping
Pout_10% = Output power at THD = 10%
Pout_10% =1.25 x Pout_1%

16. Package outline

HSOP24: plastic, heatsink small outline package; 24 leads **SOT566-**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.7	0.3 0.1	3.5 3.2	0.35	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.0	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.1	2.7 2.2	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT566-1						00-03-24