

TDA2510 ✓

CHROMINANCE COMBINATION FAIRCHILD LINEAR INTEGRATED CIRCUITS

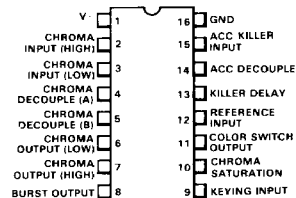
GENERAL DESCRIPTION — The TDA2510 is a monolithic integrated circuit designed for the chrominance function of a color television receiver. It is designed to interface directly with the TDA2521, using a minimum number of external components. The TDA2510 is constructed on a single silicon chip using the Fairchild Planar* epitaxial process.

- CHROMA AMPLIFIER WITH ACC
- CONTROL VOLTAGE AMPLIFIER
- BURST SEPARATOR
- COLOR KILLER AND COLOR KILLER VOLTAGE DETECTOR
- LINEAR ELECTRONIC POTENTIOMETER FOR SATURATION CONTROL
- SCHMITT TRIGGER FOR COLOR KILLER
- CHROMA DELAY LINE DRIVER STAGE
- COLOR BURST OUTPUT STAGE

ABSOLUTE MAXIMUM RATINGS

Supply voltage	15 V
Collector voltage of chroma output transistor (pin 7)	20 V
($P_D = 100$ mW max)	
Collector current of chroma output transistor (pin 7)	20 mA
Collector current of color killer output transistor (pin 11)	10 mA
Power dissipation	500 mW
Operating temperature range	-25°C to +60°C
Storage temperature range	-55°C to +125°C
Pin Temperature (Soldering 10 s)	260°C

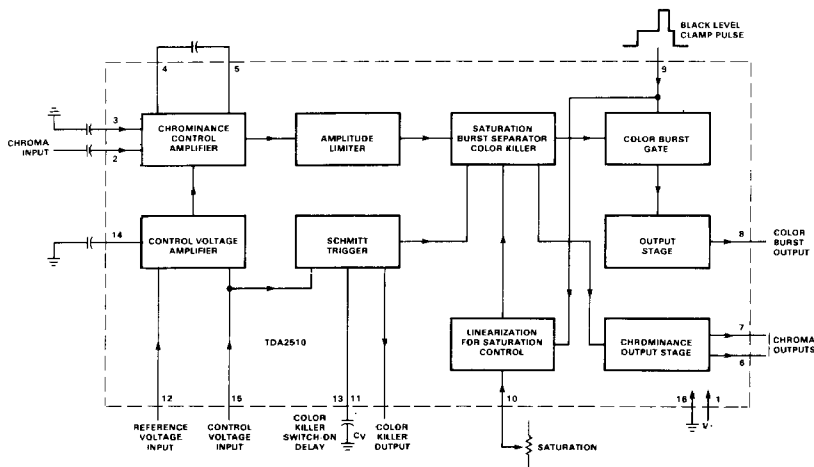
CONNECTION DIAGRAM 16-PIN DIP (TOP VIEW) PACKAGE OUTLINE 9B

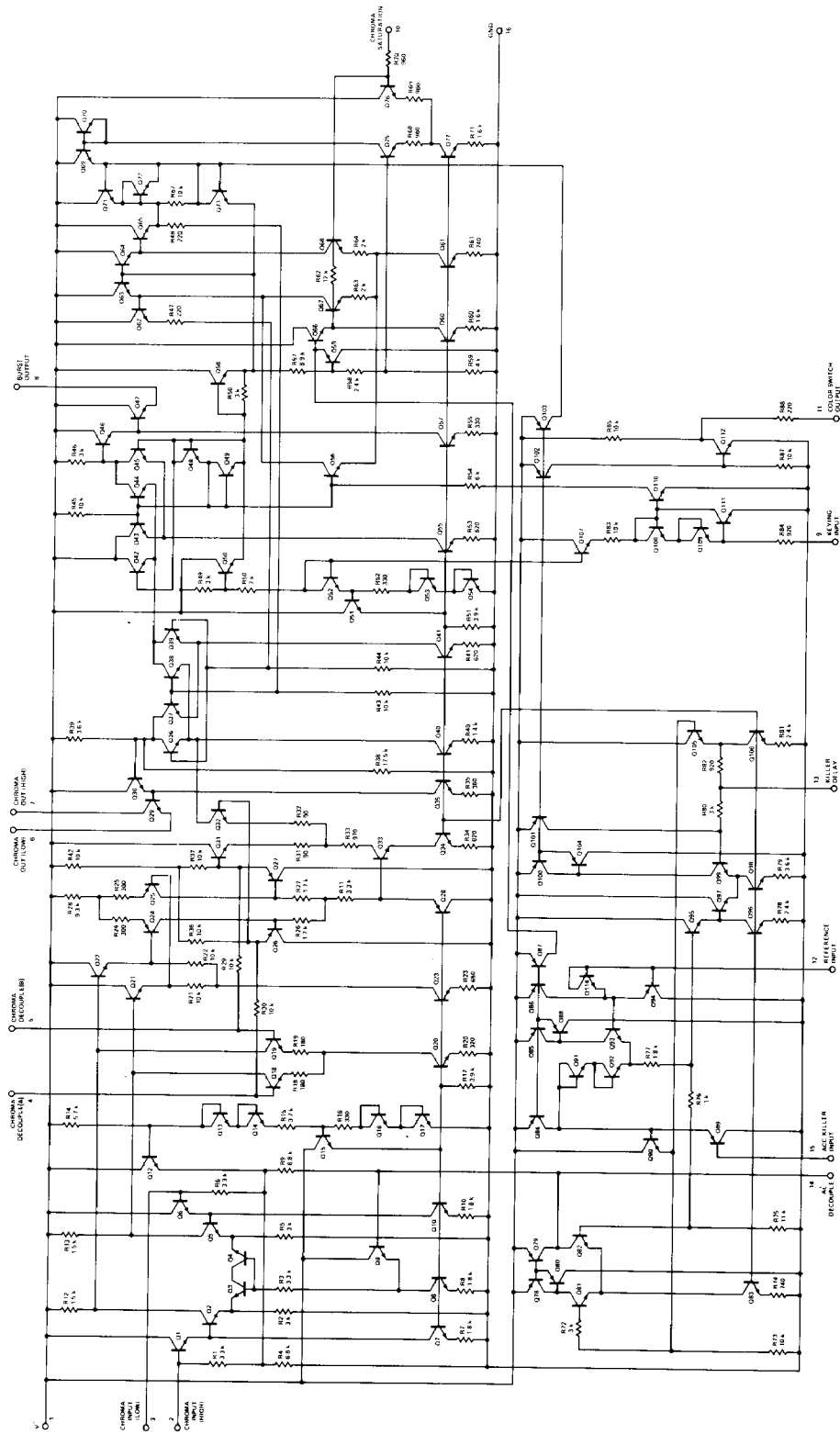


ORDER INFORMATION

TYPE	PART NO.
2510	TDA2510

BLOCK DIAGRAM





ELECTRICAL CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $V_+ = 12\text{ V}$, see test circuit unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Input (pin 2) V_{IN} (Symmetrical or Asymmetrical) Color bars (V_2 p-p) Input Voltage Range (V_2 p-p) Input Impedance (Z_2)	Note 1	-20 2.0	100	+6.0	mVp-p dB k Ω
Burst Output (Emitter Follower) (pin 8) DC Voltage at Burst Output (V_8) Burst Output (V_8 p-p) Burst Output Limiting Level	Note 1		9.0 0.5 1.5		V Vp-p Vp-p
Chroma Output (without Burst) (pin 6) DC Voltage at Chroma Output (V_6) Chroma Output (Color Bars) at nominal Saturation and Maximum contrast (V_6 p-p) Signal Plus Noise to Noise Ratio Saturation Control Range Phase Angle compared to Burst Output at Nominal Saturation Phase angle Shift during Saturation Control Range ± 6 to -10 dB	Note 2 Note 3		7.0 0.5		V Vp-p dB dB degrees degrees
Inputs for Control Voltage and Color Killer (pin 12, 15) Control Voltage (V_{15}) Input Voltage (Color On) V_{15} Input Voltage (Color Off) V_{15} Signal Suppression (Color Off) Control Input Impedance (Z_{15})	$V_{REF} =$ $V_{12} = 7\text{ V}$ $V_{12} = 7\text{ V}$ $V_{12} = 7\text{ V}$ $V_{12} = 7\text{ V}$		5.5	5.7	V V V dB k Ω
Saturation Control Input (pin 10) Voltage Range for Linear Control (V_{10}) Threshold Voltage for > 50 dB suppression Input Impedance (Z_{10})	Note 4	1.75 1.6	1.75 10	4.0	V V k Ω
Color Kill Switch Output (pin 11) Output Voltage (Color On) V_{11} Output Voltage (Color Off) V_{11} Internal Resistance			V_+ 10	0.5	V V k Ω
Burst Gating and Blanking Pulse (pin 9) Burst Gating and Blanking Pulse (positive or negative) ($\pm V_9$) Input Impedance (Z_9)		± 1.0	1.0	± 4.0	V k Ω
Color Killer Delay (pin 13) Delay Time as a Function of C_Y			24		ms/ μF

NOTES:

1. Burst output kept constant by ACC circuit at approximately 0.5 Vpp.
2. Nominal saturation is defined as maximum saturation - 6 dB, chroma/burst input ratio is approximately 2.
3. Signal plus noise to noise is calculated as V_{IN} (p-p)/6 (V_{noise} (rms)) for a standard color bar signal.
4. Saturation increases with increasing V_{10} .

APPLICATIONS AND TEST CIRCUIT

