Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543(A)/S6

Dual 16-bit low-cost economy DAC (relaxed version of TDA1543A)

GENERAL DESCRIPTION

The TDA1543(A)/S6 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as a low-cost economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in television systems and digital amplifiers.

The S6 version is a relaxed version of the TDA1543(A). The differences in performance between the S6 selection and the standard version are limited to only three parameters:

QUICK REFERENCE VALUES STANDARD VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	−70	dB
T_{amb}	operating ambient temperature range		−30	+85	°C
AI_{bias}	bias current gain		1.9	2.1	

QUICK REFERENCE VALUES S6 VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	−60	dB
T_{amb}	operating ambient temperature range		−20	+75	°C
AI_{bias}	bias current gain		1.85	2.1	

The other characteristics of the S6 version can be found in the data sheets of the TDA1543 and the TDA1543A.

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TDA1543A

Dual 16-bit DAC (economy version) (Japanese input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543A is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders and in digital amplifiers.

ORDERING INFORMATION

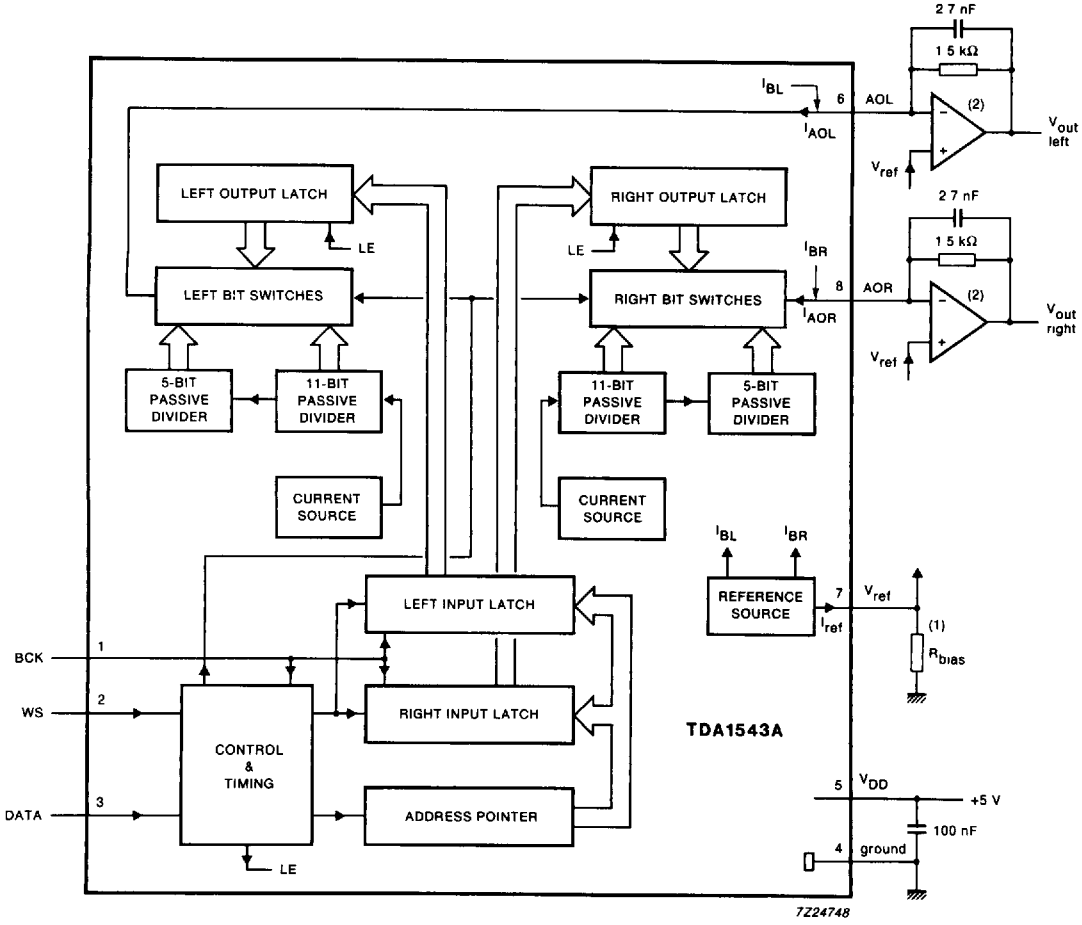
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543A	8	DIL	plastic	SOT97
TDA1543AT	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel output
V_{ref}	7	reference voltage output
AOR	8	right channel output

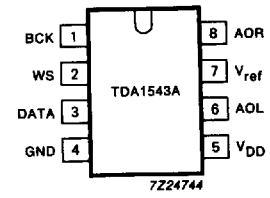


Fig.2(a) Pin configuration TDA1543A.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

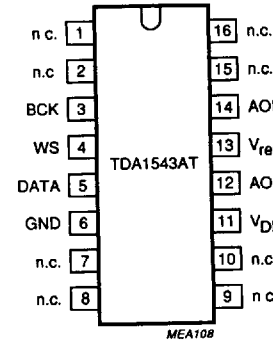
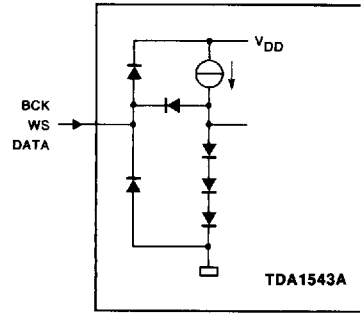
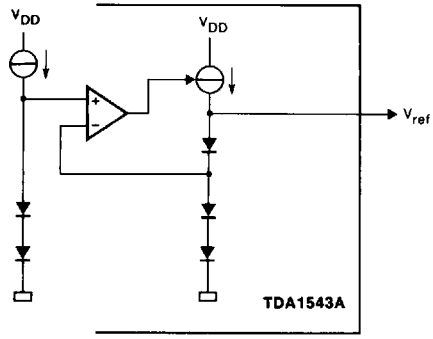


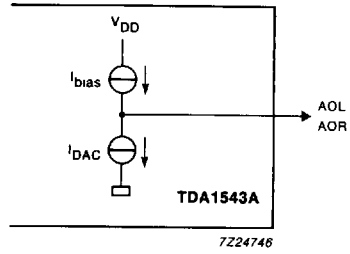
Fig.2(b) Pin configuration TDA1543AT.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (Japanese) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling*		–2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t_{HD} = 0 ns, this value has been fixed on 2 ns due to tolerances.

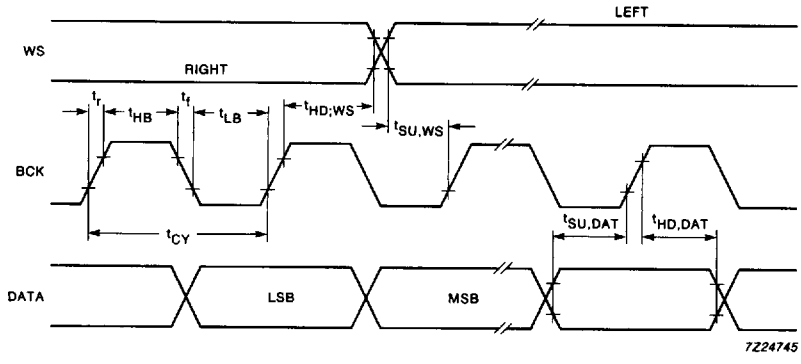


Fig.4 Format of input signals (Japanese format).

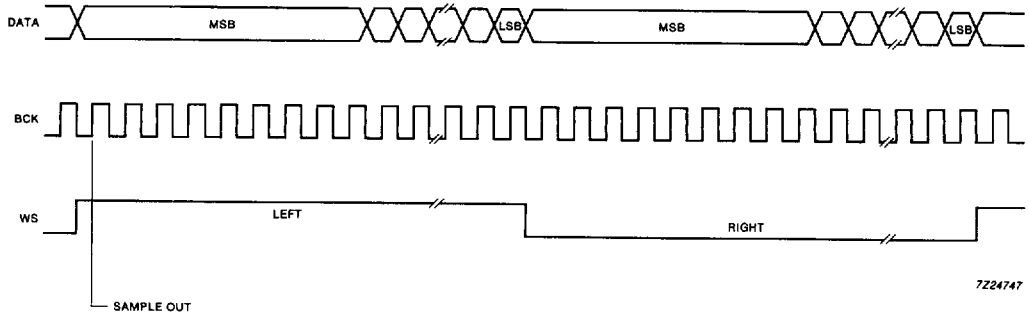
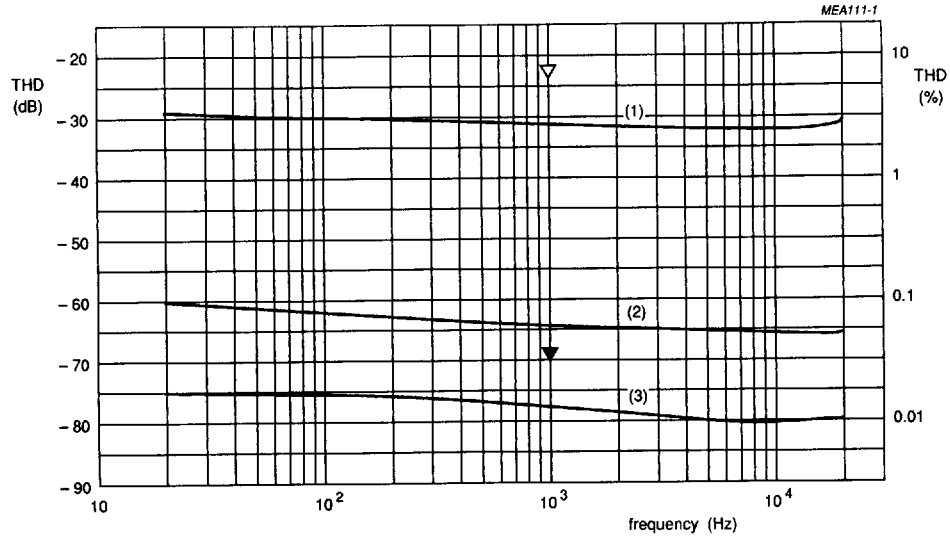


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.