GATING/FREQUENCY DIVIDER FOR ELECTRONIC MUSICAL INSTRUMENTS

The TDA1008 is a monolithic bipolar integrated circuit based on I^2L (integrated injection logic), with frequency dividers directly coupled to the gating system.

The outputs of the dividers, together with the input signal, are applied internally to nine gate inputs. By activating a key input, five successive signals out of the nine are selected and transferred to the outputs. Five key inputs are available, each selecting a different combination; e.g. 16^1, 8^1, 4^1, 2^1 and 1^1. The output signal level is proportional to the voltage applied to the key inputs. By connecting RC combinations to the key inputs, sustain of the output signal is easily obtained. The duration of the sustained signal can be adjusted by connecting a variable voltage to the appropriate terminal (pin 7).

In electronic organs using a top octave synthesizer directly coupled to twelve TDA1008 circuits, only one busbar per manual is needed to obtain five octave-related tones per key.

The tone output signals are symmetrical around a fixed d.c. voltage, thereby avoiding key clicks.

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_{P1-16}	typ.	12 V
Supply voltage divider (pin 13)	V_{P13-16}	typ.	6 V
Supply voltage tone outputs (pins 2, 3, 4, 5, 6)	V_{Ptone}	typ.	9 V
Input voltage; HIGH	V_{IH}	>	1,5 V
Input voltage; LOW	V_{IL}	<	0,4 V
Required key voltage (pins 8, 9, 10, 11, 12)	V_{K1} to V_{K5}	typ.	V_{P13-16}
Key input impedance (see note)	Z_{K1} to Z_{K5}	>	8 MΩ
Supply current (pin 1)			
all keys activated	I_1	typ.	13 mA
no activated keys	I_1	typ.	0 mA
Supply current (pin 13)	I_{13}	typ.	11 mA
Sustaining voltage range (pin 7)	V_{7sust}		0 to 2 V
Input frequency	f_i	<	100 kHz
Tone output signal voltage with one key activated	$V_{Q(p-p)}$	typ.	600 mV
Operating ambient temperature range	T_{amb}		0 to + 70 °C

Note
Key input impedance is determined by the voltage applied to pin 7. This impedance is stated at zero volt on pin 7.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

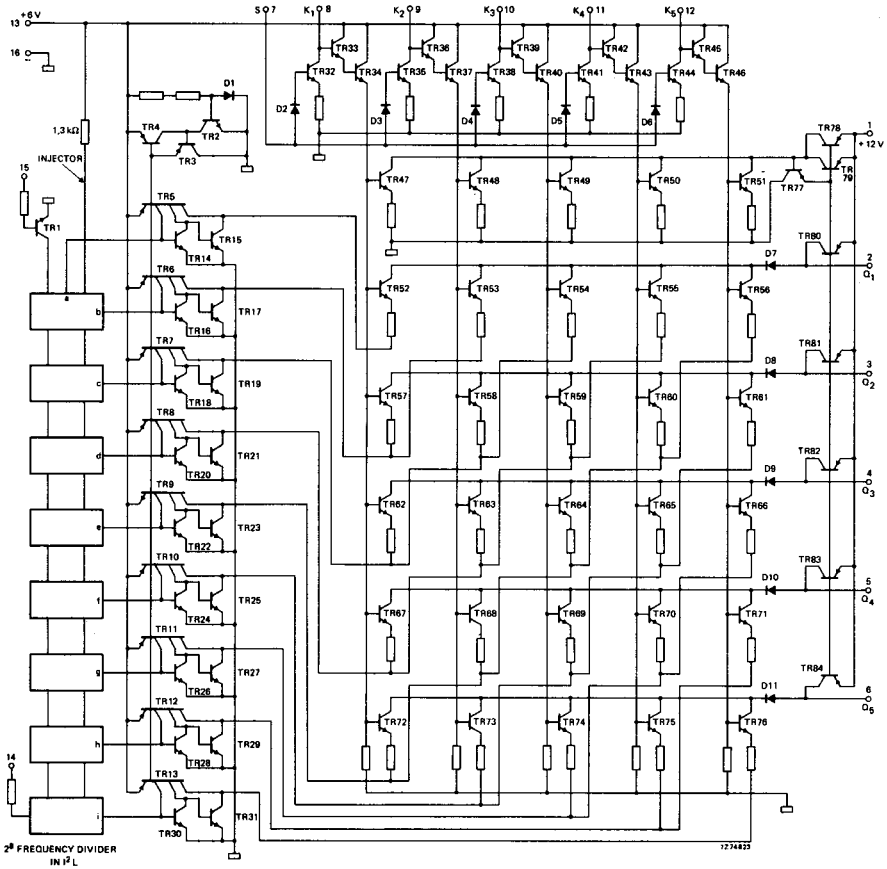


Fig. 1 Circuit diagram.

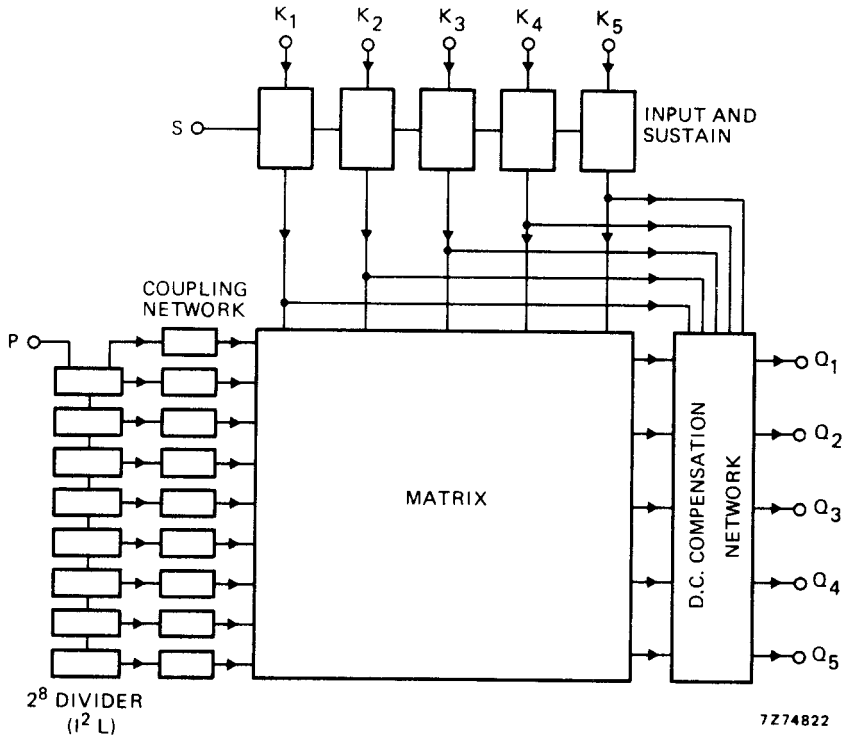


Fig. 2 Block diagram.

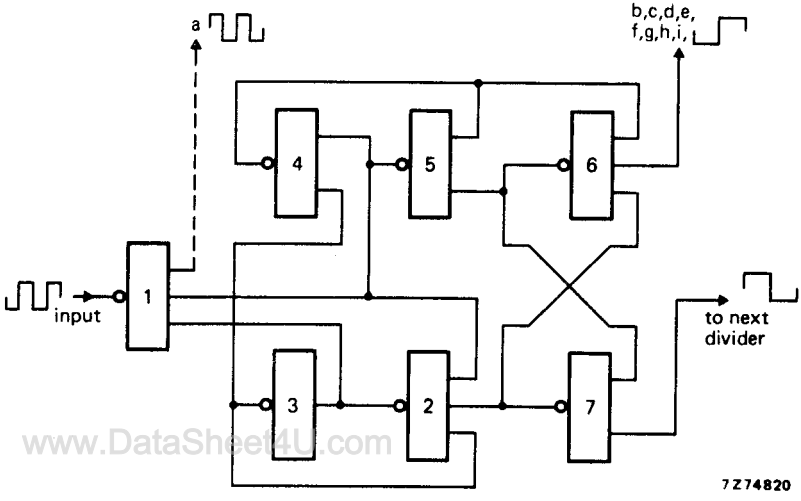


Fig. 3 Logic diagram of the I^2L 2-divider.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages			
pin 1	V_{P1-16}	max.	13 V
pin 13	V_{P13-16}	max.	6,5 V
pin 14	V_{P14-16}	max.	6,5 V
Input voltages			
K inputs (pins 8, 9, 10, 11, 12)	V_{K1} to V_{K5}	max.	V_{P13-16}
f_i input (pin 15)	V_{fi}	max.	15 V
S input (pin 7)	V_S	max.	2,5 V
Output voltages			
Q_1 to Q_5 (pins 2, 3, 4, 5, 6)	V_{Q1} to V_{Q5}	max.	12 V
Operating ambient temperature	see derating curve Fig. 4		
Storage temperature	T_{stg}		−25 to + 125 °C
Total power dissipation	see derating curve Fig. 4		

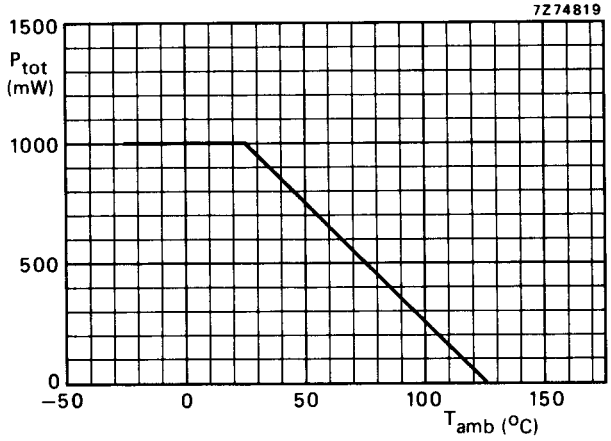


Fig. 4 Power derating curve.

CHARACTERISTICS

All voltages with reference to pin 16; all currents positive into the IC.

Supply voltage range			
pin 13	V_{P13-16}		5 to 6,5 V
pin 1	V_{P1-16}		10 to 13 V
pin 9	V_{P9-16}	see note 1	
Characteristics at T_{amb} = 25 °C; V_{P13-16} = 6 V; V_{P1-16} = 12 V; see Fig. 6.			
Supply current (pin 13)			
K-inputs at 6 V	I_{13}		7,5 to 16 mA
		typ.	11 mA
Supply current (pin 1)			
K-inputs at 6 V	I_1		8 to 16 mA
		typ.	12,7 mA
Input current at f_i (pin 15)			
V_{fi} = 6 V	I_{15}		100 to 200 μA
		typ.	150 μA
Input current K-inputs (pins 8, 9, 10, 11, 12)			
V_K = 6 V			
S-input connected to 0 V	I_K	typ.	150 nA
		<	750 nA
S-input connected to 2,0 V	I_K		80 to 150 μA
		typ.	100 μA
Input current S-input (pin 7)			
no key inputs activated	I_S	typ.	500 μA
all key inputs activated	I_S	typ.	10 μA
Output current Q-output (pins 2, 3, 4, 5, 6)			
V_Q = LOW (note 2)	$+I_Q$		230 to 450 μA
		typ.	300 μA
V_Q = HIGH (note 2)	$-I_Q$		230 to 450 μA
		typ.	300 μA
Output current pin 14	I_{14}	<	20 μA
Peak output voltage (pins 2, 3, 4, 5, 6) by activating one K-input only (Fig. 5)	V_{QM}	typ.	300 mV
Input frequency at pin 15 $V_{15HIGH} > 1,5$ V; $V_{15LOW} < 0,4$ V	f_i	<	100 kHz

Notes

1. This voltage has to be in the middle of V_{P1-16} and V_{13-16}.
2. To be multiplied by the number of activated K-inputs.

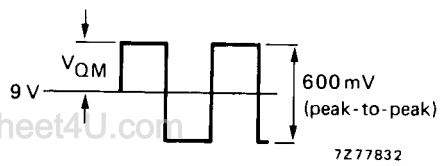


Fig. 5

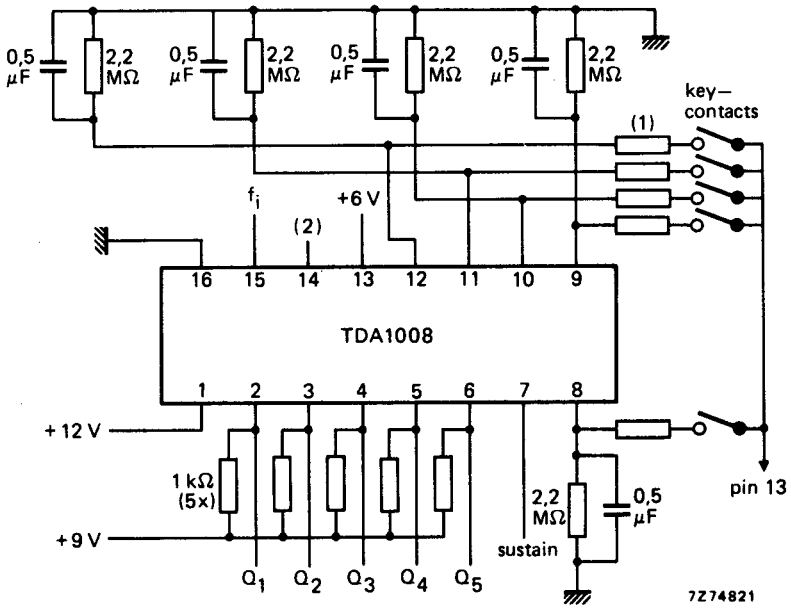
TRUTH TABLE

	K_1	K_2	K_3	K_4	K_5
Q_1	f_i	$f_i/2$	$f_i/4$	$f_i/8$	$f_i/16$
Q_2	$f_i/2$	$f_i/4$	$f_i/8$	$f_i/16$	$f_i/32$
Q_3	$f_i/4$	$f_i/8$	$f_i/16$	$f_i/32$	$f_i/64$
Q_4	$f_i/8$	$f_i/16$	$f_i/32$	$f_i/64$	$f_i/128$
Q_5	$f_i/16$	$f_i/32$	$f_i/64$	$f_i/128$	$f_i/256$

Activating 'one' key input only gives the notified output frequency.

By activating more key inputs at a time, the output amplitude will be the sum signal of the notified frequencies.

APPLICATION INFORMATION



(1) If required contact-current limiting resistors.

(2) a. Factory test point; ungated output from the final divider.

b. Can be used for obtaining very low frequencies (pedals). It should be connected to pin 13 (+ 6 V) via a resistor of minimum 300 kΩ to deliver the current I_{14}.

Fig. 6 Basic application diagram.