

# LTPS LCD Specification

Model Name: TD043MTEA2

<b>Customer Signature</b>
<b>Date</b>

This technical specification is subjected to change without notice

The information contained herein is the exclusive property of toppoly Optoelectronics corporation, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of toppoly Optoelectronics corporation.

---

**Table of Contents**

<b>NO.</b>	<b>Item</b>	<b>Page</b>
	Cover Sheet	1
	Table of Contents	2
	Record of Revision	3
1	Features	4
2	General Specifications	4
3	Input / Output Terminals	5
4	Absolute Maximum Ratings	11
5	Electrical Characteristics	12
6	Timing Chart	13
7	Optical Characteristics	15
8	Reliability	17
9	Handling Cautions	18
10	Mechanical Drawing	19
11	Packing Drawing	21

## Record of Revision

[illegible]

## 1. FEATURES

The 4.3" LCD module is the active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is applied with vertical and horizontal drivers built on the panel.

Both of horizontal and vertical scan are reversible and controlled by the parallel interface commands.

The product is designed for the requirement of the green product, and the specification complies with TPO's "Green Product Chemical Substance Specification Standard Hand Book".

## 2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	4.3	Inch
Aspect ratio	15:9	-
Display Type	Transmissive	-
Active Area (HxV)	93.6 x 56.16	mm
Number of Dots (HxV)	800 x RGB x480	Dot
Dot Pitch (HxV)	0.039 x 0.117	mm
Color Arrangement	Stripe	-
Color Numbers	16Million	-
Outline Dimension (HxVxT) *	100.6x68.45x4.1	mm
Weight	TBD	G

\*Exclude FPC and protrusions.

### 3. INPUT/OUTPUT TERMINALS

#### 3.1 TFT LCD Panel

Recommend connector: FH28-60S-0.5SH (51)

Pin	Symbol	I/O	Description	Remark
1	T1	D	Only for Toppoly test pin	
2	CGH	C	Capacitor for VGH(+8.5 V)(1 uF)	
3	CPL1	C	Capacitor for charge pump clock ( 0.2 uF)	
4	CPL2	C	Capacitor for charge pump clock ( 0.2 uF)	
5	VCOM	C	Capacitor for VCOM (2.2 uF)	
6	VD	I	Vertical sync input	
7	HD	I	Horizontal sync input	
8	DEN	I	Data Enable	
9	NCLK	I	Clock signal, latch data onto line latches	
10	B0	I	Blue data (LSB)	
11	B1	I	Blue data	
12	B2	I	Blue data	
13	B3	I	Blue data	
14	B4	I	Blue data	
15	B5	I	Blue data	
16	B6	I	Blue data	
17	B7	I	Blue data (MSB)	
18	GND	P	Ground	
19	G0	I	Green data (LSB)	
20	G1	I	Green data	
21	G2	I	Green data	
22	G3	I	Green data	
23	G4	I	Green data	
24	G5	I	Green data	
25	G6	I	Green data	
26	G7	I	Green data (MSB)	
27	VCC	P	Power supply (3.3 V) for digital circuit	
28	R0	I	Red data (LSB)	
29	R1	I	Red data	
30	R2	I	Red data	
31	R3	I	Red data	
32	R4	I	Red data	
33	R5	I	Red data	

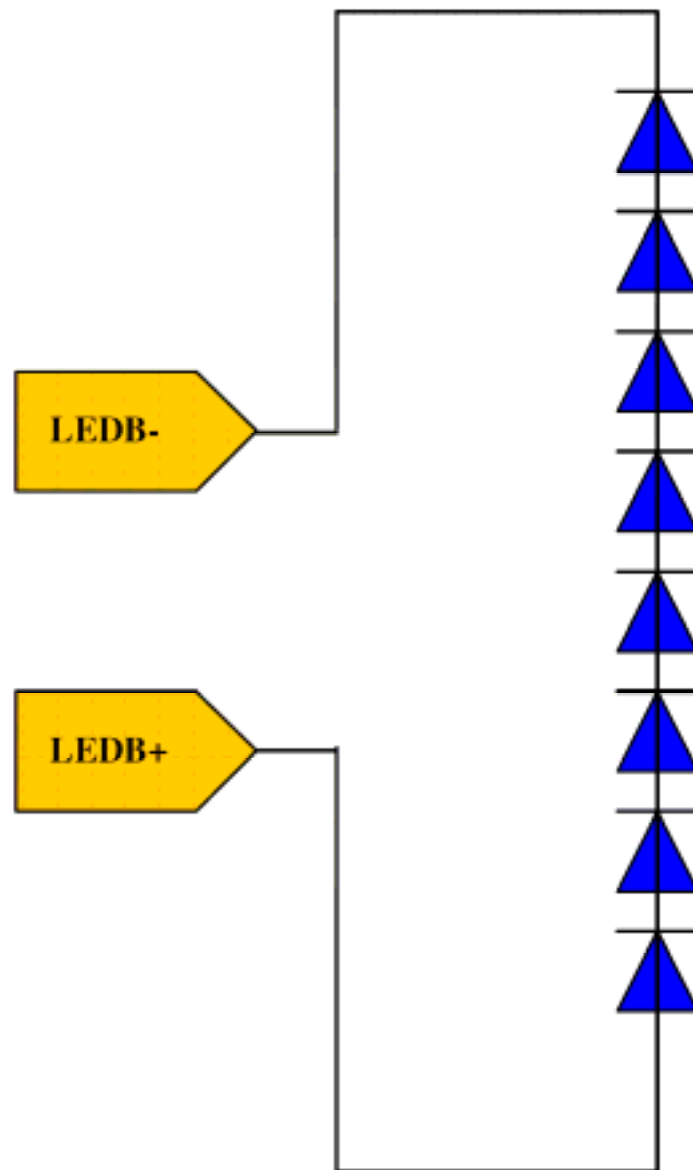
34	R6	I	Red data	
35	R7	I	Red data (MSB)	
36	VDDP	P	+5 V power supply for analog circuit	
37	VSS	P	Ground	
38	VDDN	P	-5 V power supply for analog circuit	
39	HVDE	I	Mode selection pin. HVDE="H" for SYNC(use HD +VD) mode, HVDE="L" for DE(use DEN) mode.	
40	GREST	I	Global reset pin	
41	STBY	I	Standby mode setting pin	
42	SCEN	I	Serial interface chip enable line	
43	SCL	I	Serial interface clock line	
44	SDA	I/O	Serial interface data line	
45	VCC	P	Power supply (3.3 V) for digital circuit	
46	FB	I	Main boost regulator feedback input( default:disable)	
47	GND	P	Ground	
48	VMP	C	Capacitor for +1.8 V power supply(2.2 uF)	
49	VMN	C	Capacitor for -1.8 V power supply(2.2 uF)	
50	C11	C	Capacitor for charge pump (DC/DC) circuit (1 uF)	
51	C12	C	Capacitor for charge pump (DC/DC) circuit (1 uF)	
52	CGL	C	Capacitor for VGL(-6.5V) (0.1 uF)	
53	Y_UP	I	For Touch panel Y_UP	Note 2
54	X_LEFT	I	For Touch panel X_LEFT	
55	Y_BOTTOM	I	For Touch panel Y_BOTTOM	
56	X_RIGHT	I	For Touch panel X_RIGHT	
57	LED A+	P	LEDA power: anode (no use)	Note 1
58	LED B+	P	LEDB power: anode	
59	LED B-	P	LEDB power: cathode	
60	LED A-	P	LEDA power: cathode (no use)	

I : Input O: Output P: Power C: Capacitor D: Dummy I/O : Input/Output

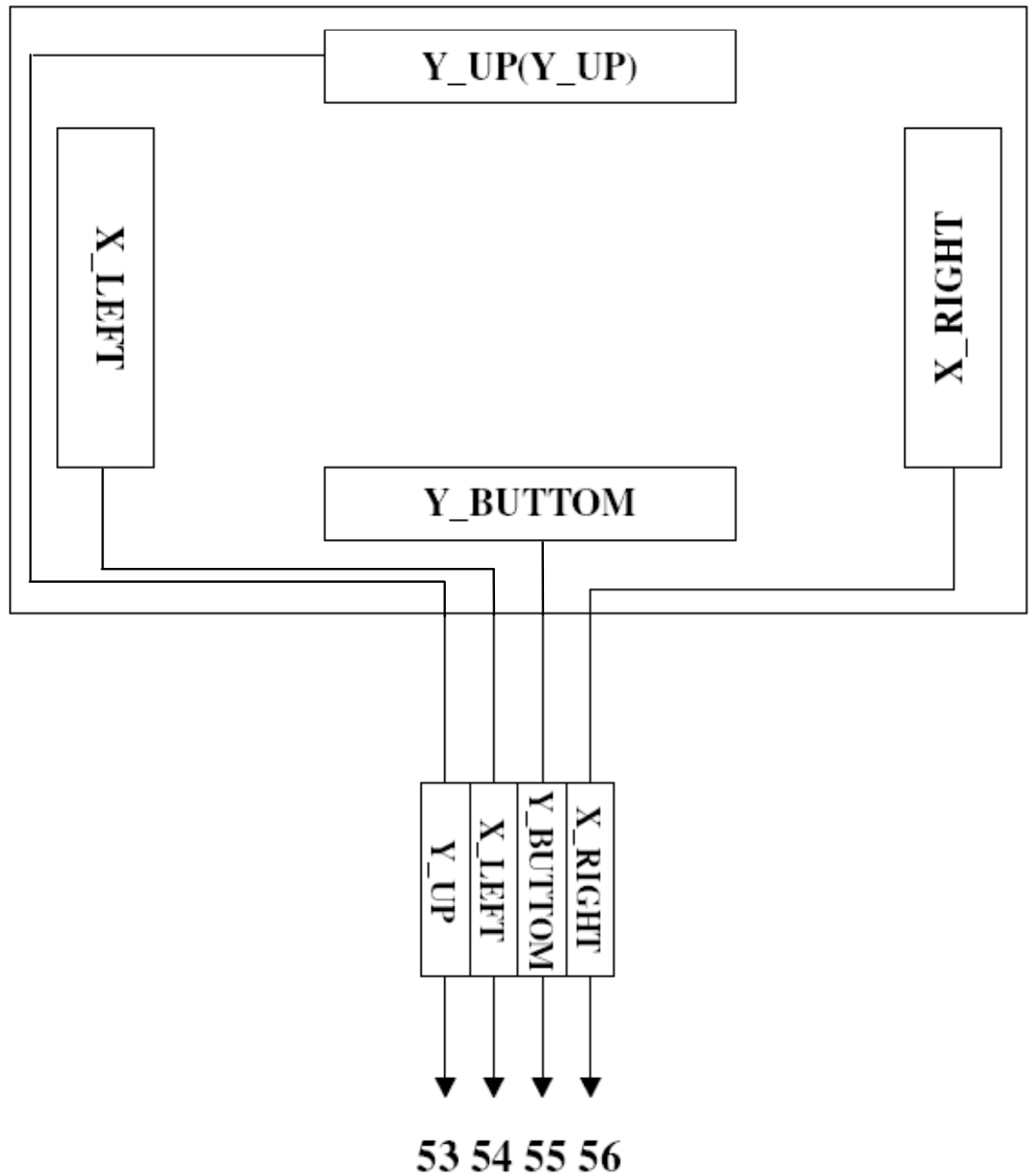
Note 1: The figure below shows the connection of backlight LED

Note 2: The figure below shows the connection of Touch panel.

Note 1: LEDA+ , LEDA- no use

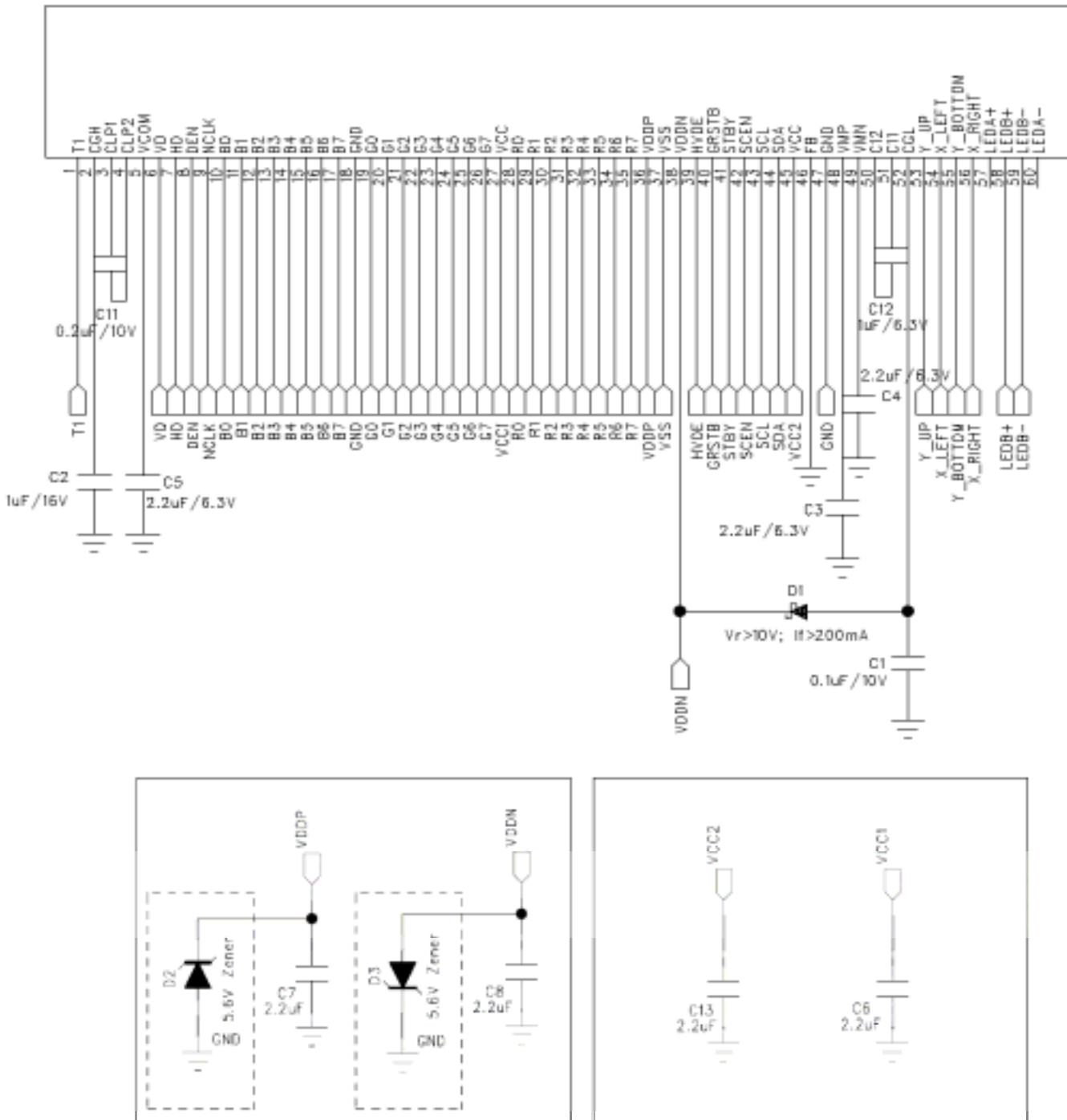


## TOP VIEW





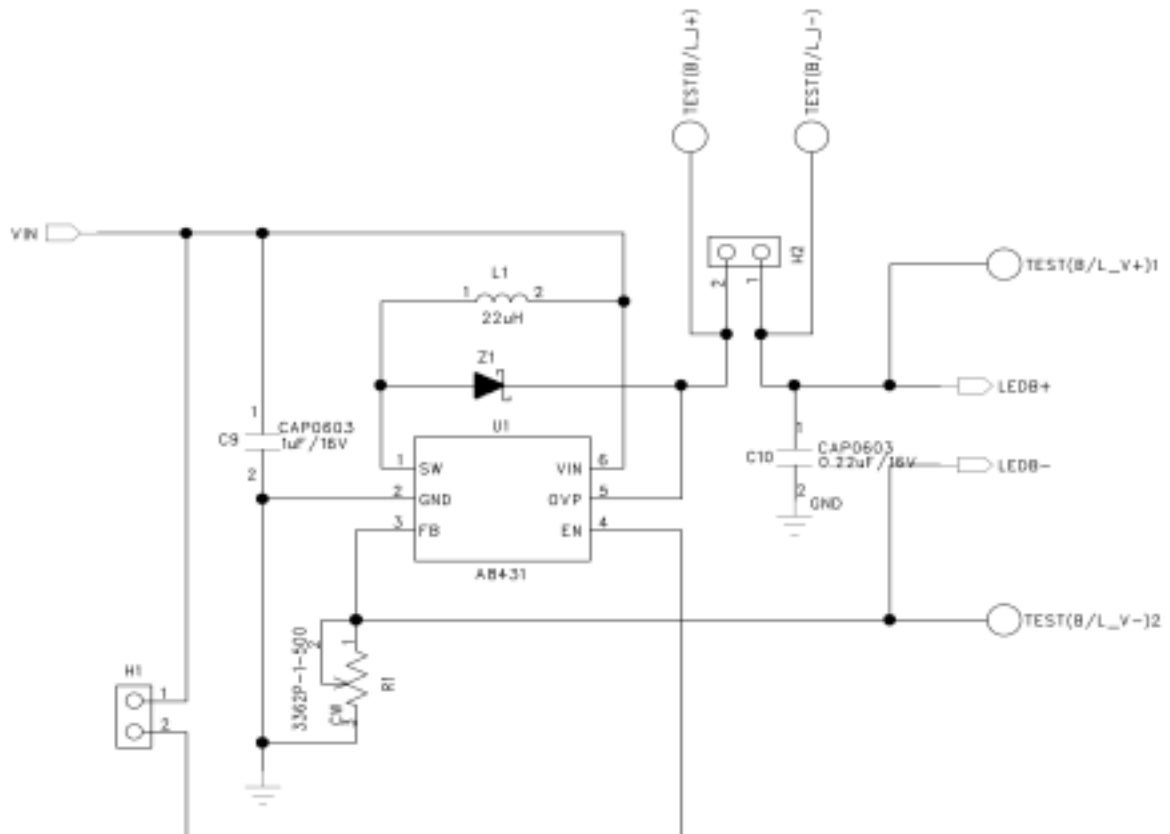
**Application circuit :**  
**For LCD module**



Recommendable Zener-Diode : PANJIT - BZT52 B5V6S

The Zener diode is used for protecting the voltage damping, spike or unclear power (have large noise etc.) to break down the driver IC on LCD module. If the LCD user can guarantee the voltage range of VDDP and VDDN will always lie in spec definition (please refer the 5. ELECTRICAL CHARACTERISTICS). The Zener-Diode is not necessary.

For LED backlight driver



#### 4. ABSOLUTE MAXIMUM RATINGS

Ta = 25

Item	Symbol	MIN	MAX	Unit	Remark
Digital Power Supply Voltage	VCC	-0.5	5.0	V	
Analog Power Supply Voltage (positive)	VDDP	-0.5	5.5	V	
Analog Power Supply Voltage (negative)	VDDN	-5.5	0.5	V	
Logic input voltage	V <sub>IN1</sub>	-0.3	VCC+0.3	V	VD, HD, DEN, NCLK, R[7:0], G[7:0], B[7:0], SDA, SCL, SCEN, STBY, GRSTB, HVDE
Back Light Forward Current	I <sub>F</sub>	18	23	mA	
Operating Temperature	T <sub>OPR</sub>	-20	+70		
Storage Temperature	T <sub>STG</sub>	-40	+85		

Please ensure that the power supply voltage (Digital & Analog) does not exceed the absolute maximum rating **in any condition** when the LCD module is operating. Or the driver IC on the LCD module can be broken.

## 5. ELECTRICAL CHARACTERISTICS

### 5.1. Driving TFT LCD Panel

GND=0V, Ta=25

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		VCC	2.7	3.3	3.6	V	
		VDDP	4.5	5.0	5.5	V	
		VDDN	-5.5	-5	-4.5	V	
Input Signal Voltage	Low Level	V <sub>IL</sub>	GND	-	0.2x VCC*	V	VD, HD, DEN, NCLK, R[7:0], G[7:0], B[7:0], SDA, SCL, SCEN, STBY, GRSTB, HVDE
	High Level	V <sub>IH</sub>	0.8x VCC*	-	VCC*	V	
Panel Power Consumption		W <sub>P</sub>	-	120	150	mW	Base on 800RGBx480

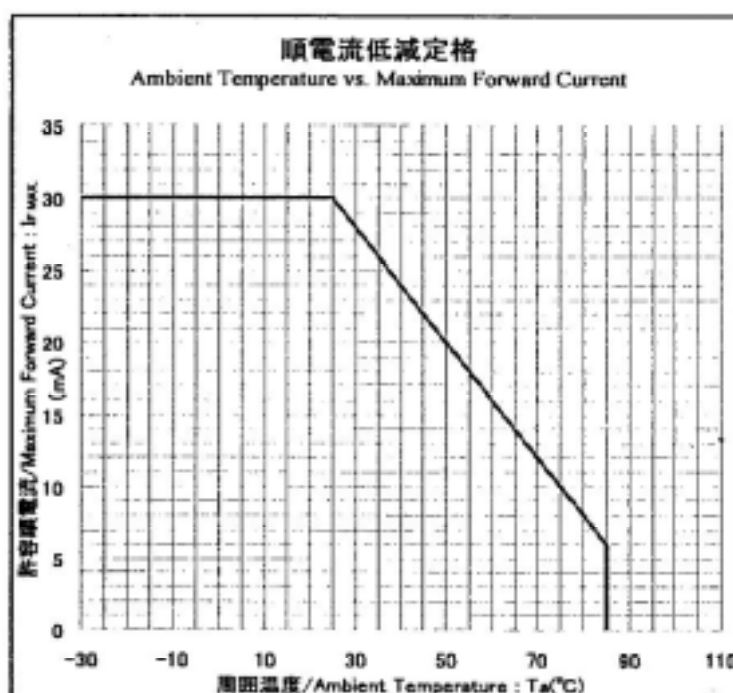
VCC\* =VCC (TYP)

### 5.2. Driving Backlight

Ta=25

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I <sub>f</sub>	18	20	23	mA	
Forward Current Voltage	V <sub>f</sub>	-	26.4	29.6	V	
Backlight Power Consumption	W <sub>BL</sub>	-	528	680.8	mW	

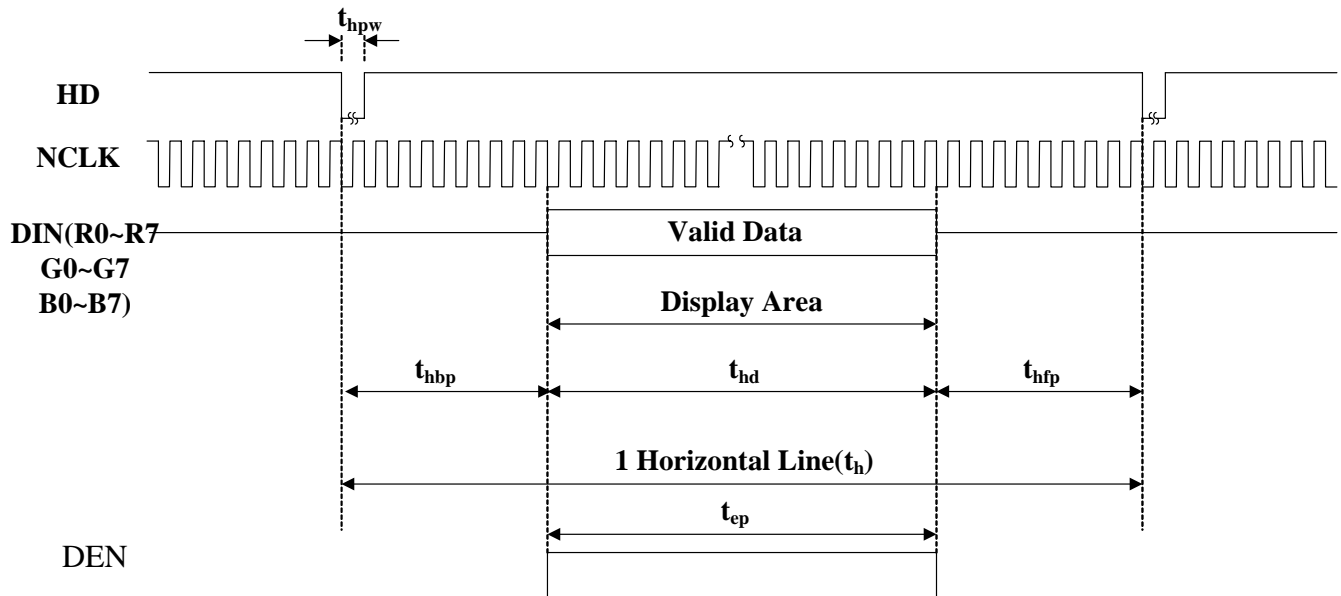
Backlight driving circuit is recommend as the fix current circuit.



## 6. TIMING CHART

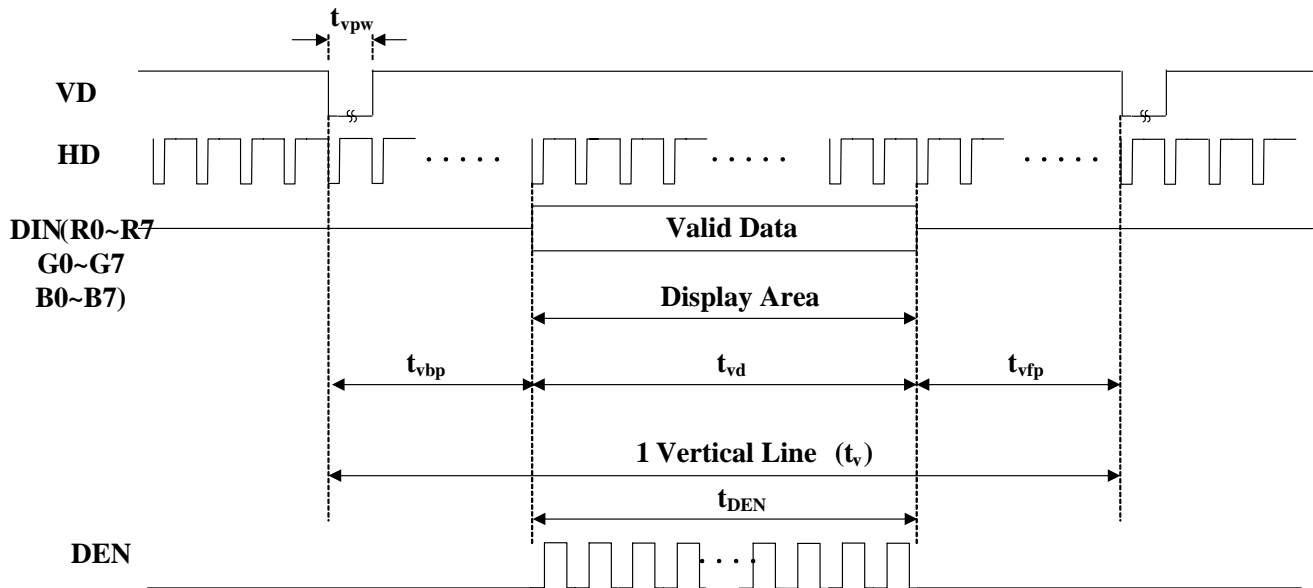
<Input timing >

--Horizontal--



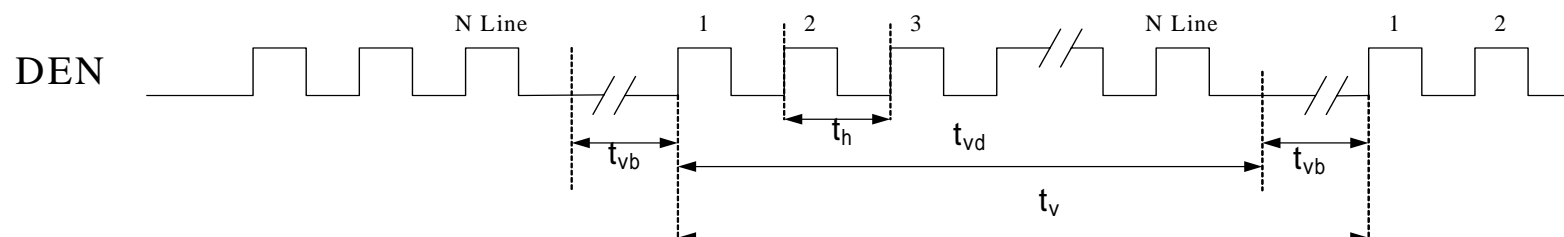
### Horizontal Input Data

Parameter		Symbol	800RGBx480	480RGBx272	400RGBx240	Unit
NCLK Frequency		$F_{NCLK}$	33.2	9	8.3	MHz
Horizontal valid data		$t_{hd}$	800	480	400	NCLK
1 Horizontal Line		$t_h$	1056	525	528	NCLK
HSYNC Pulse Width	Min.	$t_{hpw}$	1	1	1	NCLK
	Typ.					
	Max.					
Hsync blanking		$t_{hbp}$	216	43	108	NCLK
Hsync front porch		$t_{hfp}$	40	2	20	NCLK
DEN Enable Time		$t_{ep}$	800	480	400	NCLK



Parameter		Symbol	800RGBx480	480RGBx272	400RGBx240	Unit
Vertical valid data		$t_{vd}$	480	272	240	H
Vertical period		$t_v$	525	286	262	H
VSYNC Pulse Width	Min.	$t_{vpw}$	1	1	1	H
	Typ.					
	Max.					
Vertical back porch		$t_{vbp}$	35	12	20	H
Vertical front porch		$t_{vfp}$	10	2	2	H
Vertical blanking of DEN mode		$t_{vb}$	45	14	22	H
Total DEN in VD		$t_{DEN}$	480	272	240	H

**DEN mode (The DEN signal can instead of HD and VD signals for ASIC to identify the input data)**



## 7. OPTICAL CHARACTERISTICS

### 7.1 Optical Specification

Ta=25

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles		11 + 12	CR ≥ 10	150	170	-	Degree	Note 7-1
		21 + 22		150	170	-		
Contrast Ratio		CR	=0°	280	400	-		Note 7-2
Response Time	Rising	Tr		-	30	40	ms	Note 7-3
	Falling	Tf		-	10	15		
Luminance (If=23mA)		L		230	280	-	cd/m <sup>2</sup>	Note 7-4
Chromaticity	White	x <sub>w</sub>		0.26	0.31	0.36		Note 7-5
		y <sub>w</sub>		0.28	0.33	0.38		

### 7.2 Basic Measure Conditions

(1) Driving voltage

V<sub>cc</sub>= 3 V

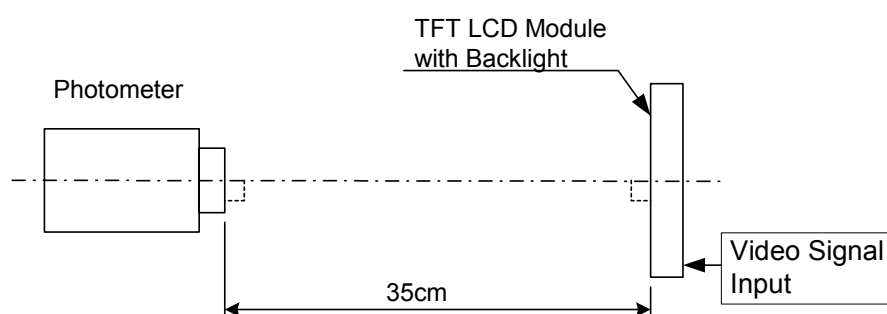
(2) Ambient Temperature: Ta=25

(3) Testing Point: Measure in the display center point and the test angle =0°

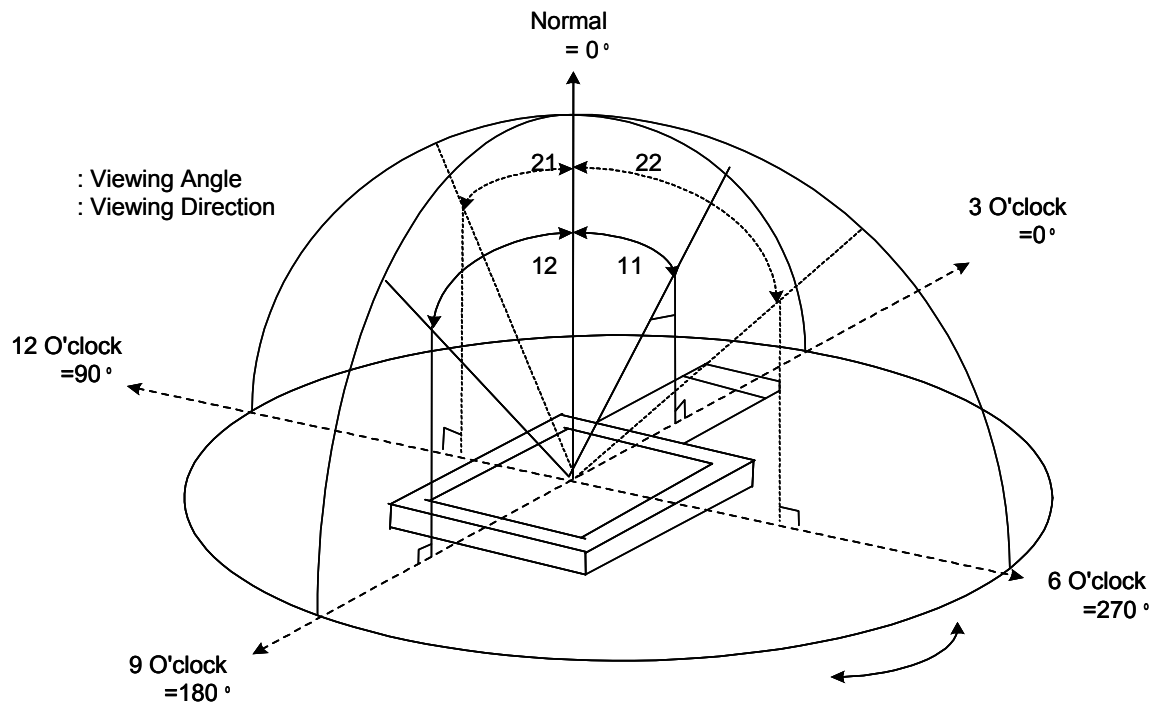
(4) LED Current: I<sub>F</sub>=23mA.

(5) Testing Facility

Environmental illumination: ≤ 1 Lux



Note 7-1: Viewing angle diagrams:

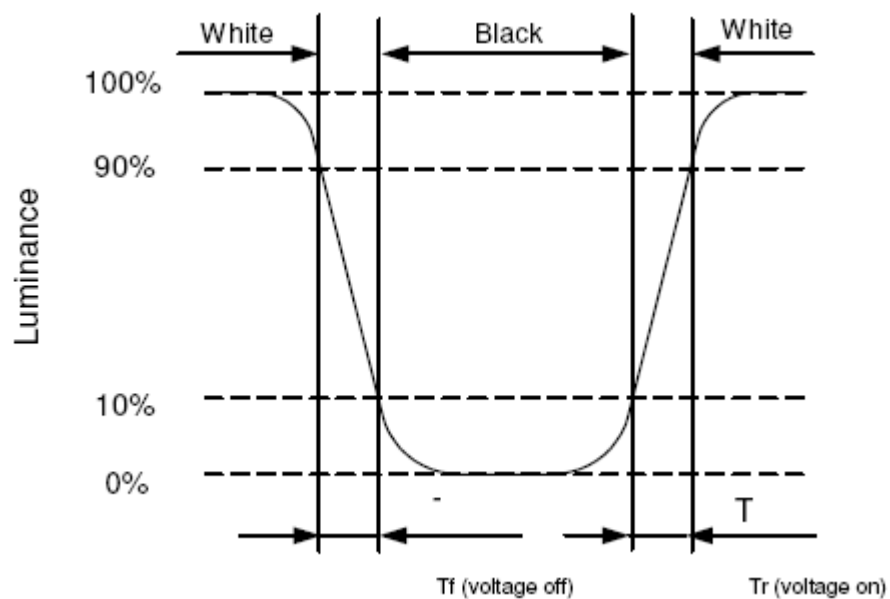


Note 7-2: Contrast Ratio:

Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-3: Definition of response time:



Note 7-4: Luminance:

Test Point: Display Center

Note 7-5: Chromaticity: The same test condition as Note 7-4.



## 8 RELIABILITY

No	Test Item	Condition
1	High Temperature Operation	Ta=+70 , 240hrs
2	High Temperature & High Humidity Operation	Ta=+40 ,95%RH, 240hrs
3	Low Temperature Operation	Ta=-20 , 240hrs
4	High Temperature Storage (non-operation)	Ta=+85 , 240hrs
5	Low Temperature Storage (non-operation)	Ta=-40 , 240hrs
6	Thermal Shock (non-operation)	-30 <-- --> +70 , 50 cycles, (30 min) (30 min)
7	Terminal Discharge (non-operation)	C=150pF, R=330 ohm; Discharge:Air: +/-15kV; Contact: +/-8kV 5 times/Point; 5 points/ Panel
8	Vibration (non-operation)	Frequency:10~55Hz; Amplitude:1.5mm Sweet Time: 11min Test Time: 2hrs for each direction of X,Y,Z
9	Shock (non-operation)	Acceleration: 100G; Period:6ms Directions: +/-X; +/-Y; +/-Z; Cycles: Once
10	Pin Activation Test(Touch Panel)	Hit 1000000 times with a silicon rubber of R8 HS60 Hitting Force:250g Hitting Speed:3 time/sec.
11	Writing Friction Resistance Test (Touch Panel)	Pen:0.8R Polyacetal stylus Load:250g Speed: 3 strokes/sec Stroke: 35mm 100000 times.

Ta: Ambient Temperature,

## 9 HANDLING CAUTIONS

### 9.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommend ESD strategy

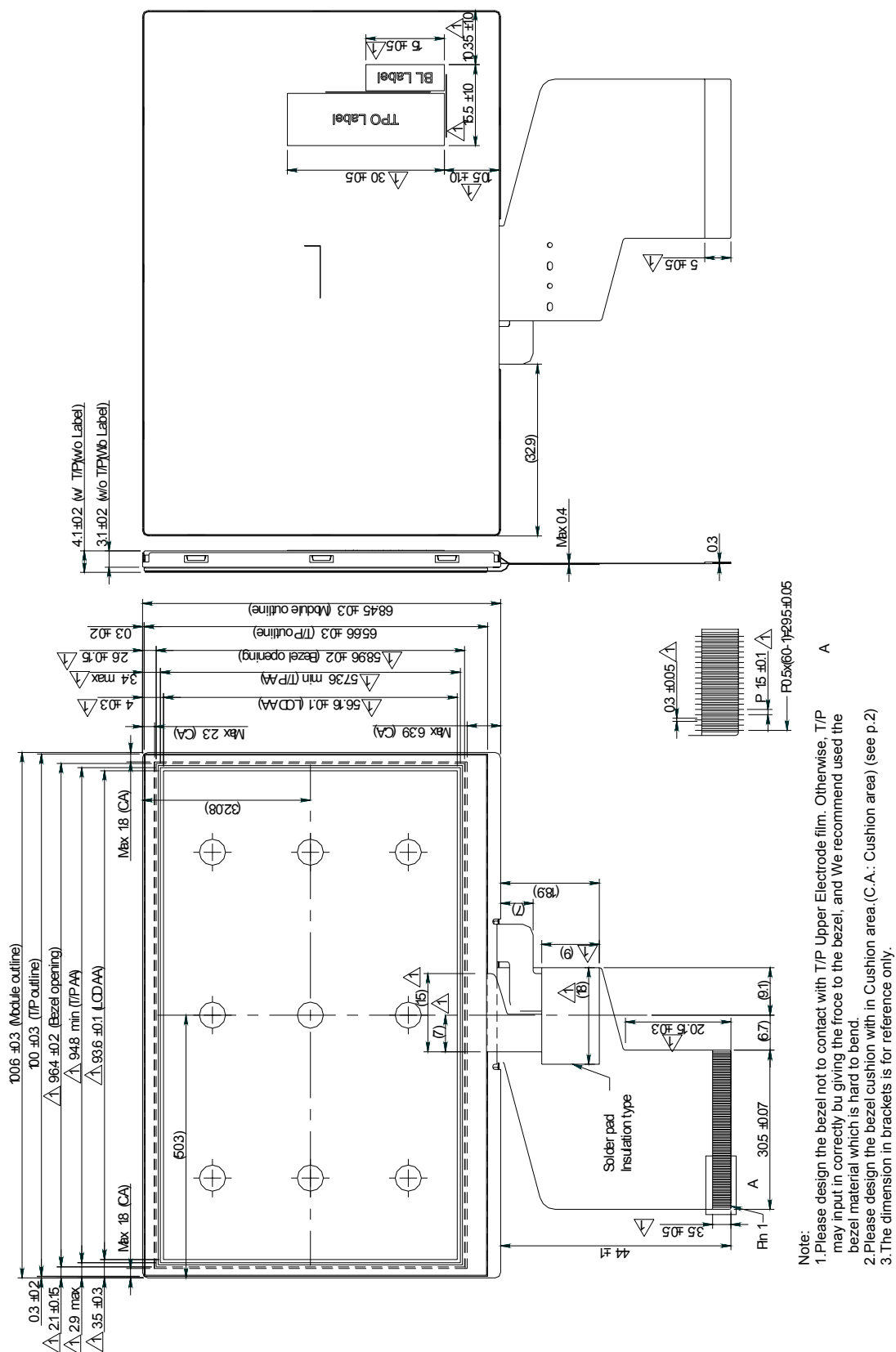
- (1) In handling LCD panel, please wear non-charged material gloves. And the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.
- (2) The machine and working table for the panel should have ESD prohibition strategy.
- (3) In handling the panel, ionize flowing decrease the charge in the environment is necessary.
- (4) In the process of assembly the module, shield case should connect to the ground.

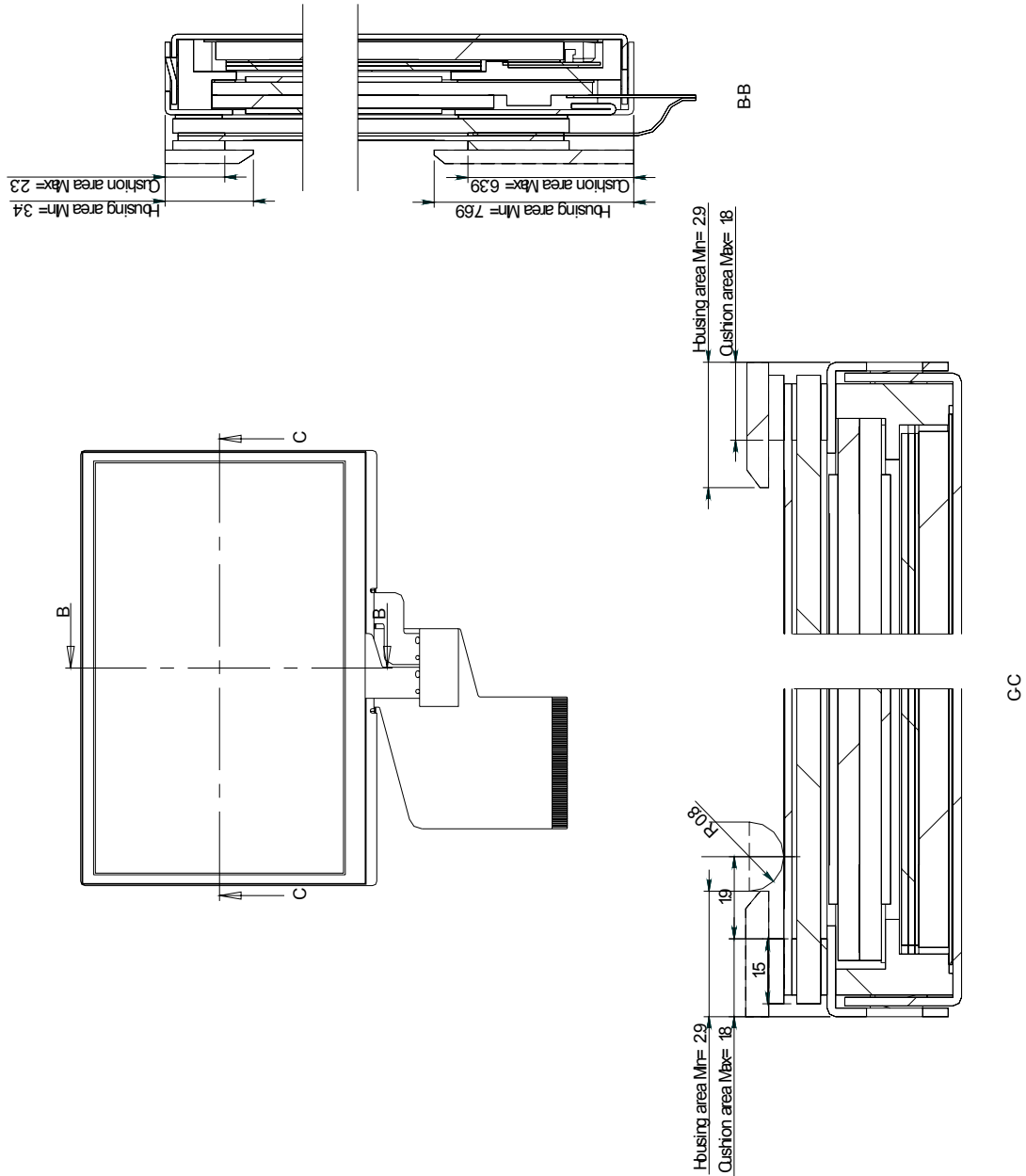
### 9.2 Environment

- (1) Working environment of the panel should in the clean room.
- (2) The front polarizer is easy damaged, handle it carefully and do not scratch it by sharp material.
- (3) Panel has polarizer protective film in the surface please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

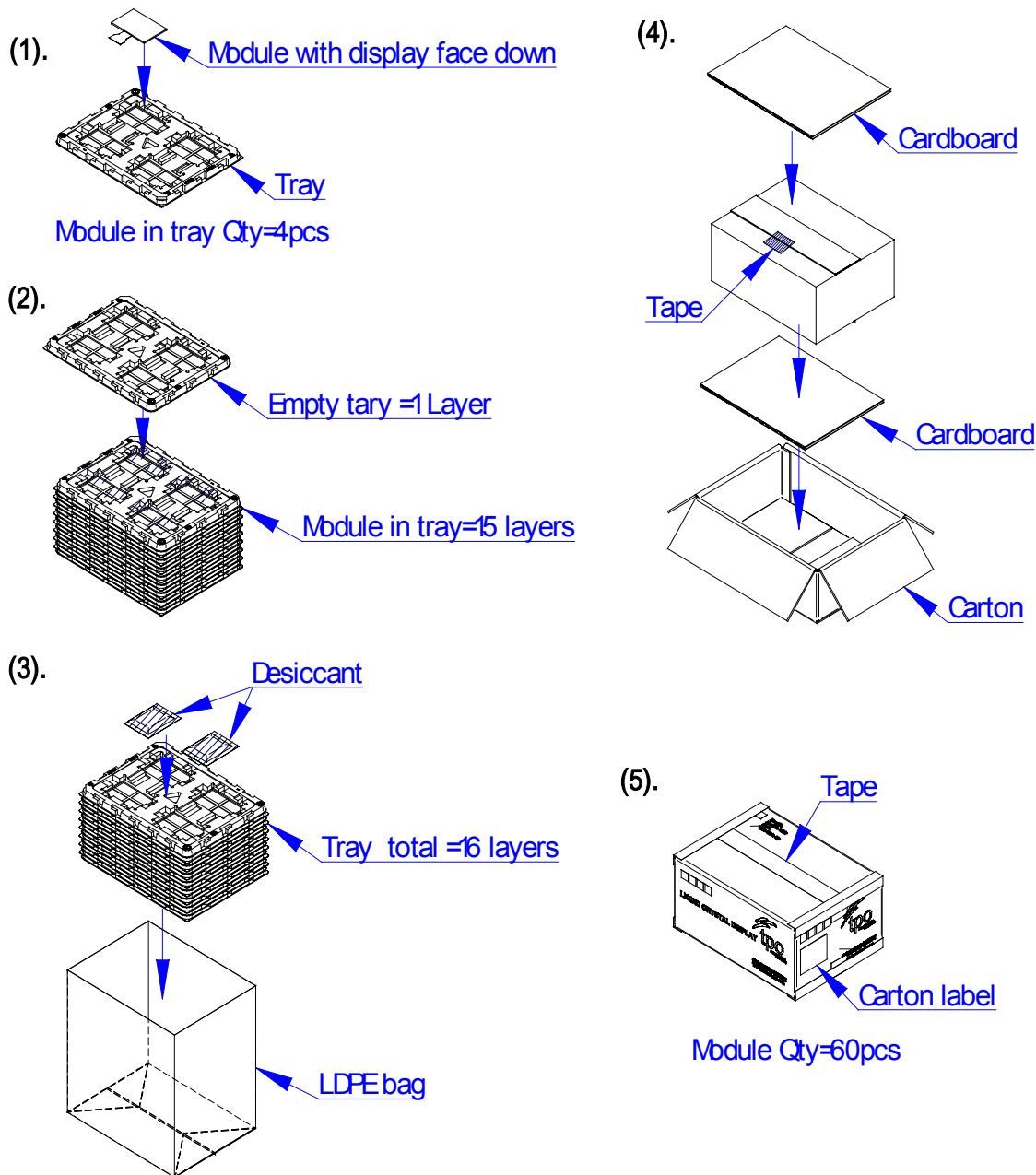
### 9.3 Others

- (1) Turn off the power supply before connecting and disconnecting signal input cable.
- (2) The connection area of FPC and panel is very weak, do not handle panel only by FPC or bend FPC.
- (3) Water drop on the surface or condensation as panel power on will corrode panel electrode.
- (4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.
- (5) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.





## 11 Packing Drawing



### 4.3" module (TD043MTEA2) delivery packing method

- (1). Module packed into tray cavity (with Module display face down).
- (2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.  
2pcs desiccant put above the empty tray
- (3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.
- (4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton.  
Put 1pc cardboard above the package unit.
- (5). Carton tapping with adhesive tape.