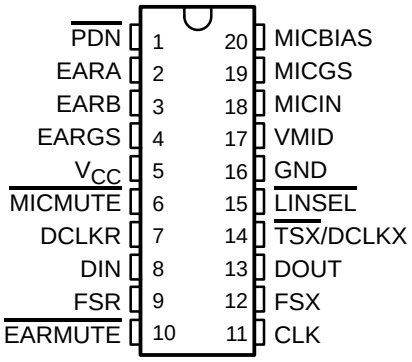
SLWS001 – D4091, JUNE 1993

- **Single 5-V Operation**
- **Low Power Consumption:**
  Operating Mode . . . 55 mW Typ
  Standby Mode . . . 8 mW Typ
  Power-Down Mode . . . 3 mW Typ
- **Combined ADC, DAC, and Filters**
- **Extended Variable-Frequency Operation**
  Pass-Band up to 10 kHz
- **Electret Microphone Bias Reference Voltage Available**
- **Directly Drives a Piezo Speaker**
- **Compatible With All DSPs**
- **Selectable Between 8-Bit, μ-Law Companded and 13-Bit Linear Conversion**
- **Programmable Volume Control in Linear Mode**
- **Designed for Standard 2.048-MHz Master Clock for U.S. Analog, U.S. Digital, CT2, Battery-Powered Telephones**

DW OR N PACKAGE
(TOP VIEW)



description

The general-purpose audio interface for digital signal processors (DSPs) is designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) together with transmit and receive filtering for voice-band audio systems. In particular, cellular telephone systems are targeted; however, this integrated circuit can function in several systems, including digital audio, multimedia telecommunications, noise cancellation, and other data acquisition.

The converted data is available in two formats. The formats are pin selectable between companded and linear. When the device is in the companded mode, data is transmitted and received in eight-bit words. When the linear mode is selected, 13 bits of data are sent and received, padded with trailing zeros or volume control bits to provide a 16-bit word.

The transmit section is designed to directly interface with an electret microphone element. A reference voltage equal to $V_{CC}/2$, called VMID, is used to develop the midlevel virtual ground for all the amplifier circuits and the microphone bias circuit. A reference voltage called MICBIAS can be used to supply bias current for the microphone. The microphone input signal (MICIN) is buffered and amplified with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through antialiasing and band-pass filters. The filtered signal is then input to a compressing analog-to-digital converter (COADC) if companded mode is selected; otherwise, the analog-to-digital converter performs a linear conversion.

Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

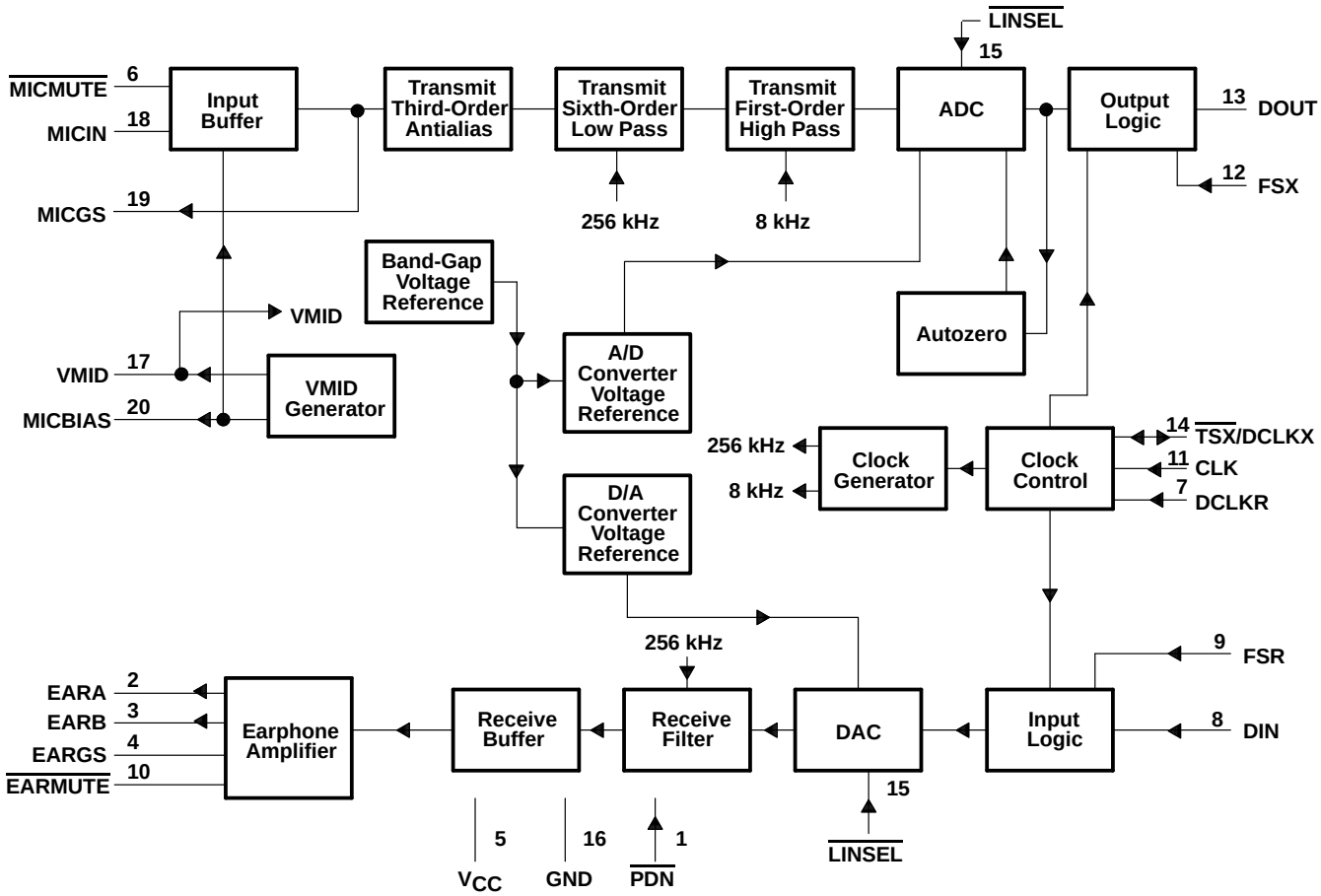
description (continued)

The receive section takes a frame of serial data on DIN and converts it to analog through an expanding digital-to-analog converter (EXDAC) if the companded mode is selected; otherwise, a linear conversion is performed. The analog signal then passes through switched-capacitor filters, which provide out-of-band rejection, (sin x)/x correction functions, and smoothing. The filtered signal is sent to the earphone amplifier. The earphone amplifier has a differential output with adjustable gain that is designed to minimize static power dissipation.

A single on-chip, high-precision band-gap circuit generates all voltage references, eliminating the need for external reference voltages.

The TCM320AC46 device is characterized for operation from 0°C to 70°C.

functional block diagram



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
CLK	11	I	In the fixed-data-rate mode, CLK is the master clock input as well as the transmit and receive data clock input. In the variable-data-rate mode, CLK serves only as the master clock input.
DCLKR	7	I	Selects fixed- or variable-data-rate operation. When DCLKR is connected to V_{CC}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{CC}, the device operates in the variable-data-rate mode and DCLKR becomes the receive data clock.
DIN	8	I	Receive data input. Input data is clocked in on consecutive negative transitions of the receive data clock, which is CLK for a fixed data rate and DCLKR for a variable data rate.
DOUT	13	O	Transmit data output. Transmit data is clocked out on consecutive positive transitions of the transmit data clock, which is CLK for a fixed data rate and DCLKX for a variable data rate.
EARA	2	O	Earphone output. EARA forms a differential drive when used with the EARB signal.
EARB	3	O	Earphone output. EARB forms a differential drive when used with the EARA signal.
EARGS	4	I	Earphone gain set input of feedback signal for the earphone output. The ratio of an external potential divider network connected across EARA and EARB adjusts the power amplifier gain. Maximum gain occurs when EARGS is connected to EARB, and minimum gain occurs when EARGS is connected to EARA. Earphone frequency response correction is performed using an external RC filter.
$\overline{\text{EARMUTE}}$	10	I	Earphone output mute control signal. When $\overline{\text{EARMUTE}}$ is low, the output amplifier is disabled and no audio is sent to the earphone.
FSR	9	I	Frame synchronization clock input for receive channel. In the variable-data-rate mode, FSR must remain high for the duration of the time slot. The receive channel enters the standby state when FSR is TTL low for five frames or longer. The device enters a production test-mode condition when either FSR or FSX is held high for five frames or longer.
FSX	12	I	Frame synchronization clock input for transmit channel. FSX operates independently of, but in an analogous manner to, FSR. The transmit channel enters the standby state when FSX is low for five frames or longer. The device enters a production test-mode condition when either FSX or FSR is held high for five frames or longer.
GND	16		Ground return for all internal analog and digital circuits
$\overline{\text{LINSEL}}$	15	I	Linear selection input. When low, $\overline{\text{LINSEL}}$ selects linear coding/decoding. When high, $\overline{\text{LINSEL}}$ selects companded coding/decoding. The companded mode is μ-law.
MICBIAS	20	O	Bias voltage equal to VMID for the electret microphone
MICGS	19	O	Output of the internal microphone amplifier. MICGS used as the feedback to set the microphone amplifier gain. If sidetone is required, it is accomplished by connecting a series network between MICGS and EARGS.
MICIN	18	I	Electret microphone input to the internal microphone amplifier
$\overline{\text{MICMUTE}}$	6	I	Microphone input mute control signal. When $\overline{\text{MICMUTE}}$ is active (low), the input amplifier is disabled, the microphone current is switched off, and zero code is transmitted.
$\overline{\text{PDN}}$	1	I	Power-down input. When low, the device powers down to reduce power consumption.
$\overline{\text{TSX}}$/DCLKX	14	I/O	Transmit time slot strobe (active-low output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this is an open-drain output that pulls to ground and is used as an enable signal for a 3-state buffer. In the variable-data-rate mode, DCLKX becomes the transmit data clock input.
V_{CC}	5		5-V supply voltage for all internal analog and digital circuits
VMID	17	O	V_{CC}/2 bias voltage reference. An external, low-leakage, high-frequency 1-μF capacitor should be connected to VMID for filtering.

general information

system reliability features

The device should be powered up and initialized as follows:

1. GND is applied.
2. V_{CC} is applied.
3. All clocks are connected.
4. TTL high is applied to $\overline{\text{PDN}}$.
5. FSX and/or FSR synchronization pulses are applied.

Even though the device is heavily protected against latch-up, it is still possible to cause it to latch-up under certain improper power conditions where excess current is forced into or out of one or more terminals. To assure that latch-up will not occur, it is good design practice to put a reverse-biased Schottky diode between V_{CC} (power supply) and GND.

On the transmit channel, digital outputs DOUT and $\overline{\text{TSX}}$ are held in the high-impedance state for approximately four frames (500 μs) after power up or application of V_{CC}. After this delay, DOUT, $\overline{\text{TSX}}$, and signaling are functional and occur in the proper time slot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. To further enhance system integrity, DOUT and $\overline{\text{TSX}}$ are placed in the high-impedance state after an interruption of CLK.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to $\overline{\text{PDN}}$. In the absence of a signal, $\overline{\text{PDN}}$ is internally pulled up to a high logic level and the device remains active. In the power-down mode, the average power consumption is reduced to 3 mW.

The standby modes give the user the options of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held low. For transmit-only operation, FSX is pulsed and FSR is held low. For receive-only operation, FSR is pulsed and FSX is held low. In the standby mode with both transmit and receive on standby, power consumption is reduced to 8 mW. See Table 1 for power-down and standby procedures.

Table 1. Power-Down and Standby Procedures

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power on	$\overline{\text{PDN}}$ = high, FSX = pulses, FSR = pulses	55 mW	Digital outputs active but not loaded
Power down	$\overline{\text{PDN}}$ = low, FSX/FSR = X/X	3 mW	$\overline{\text{TSX}}$ and DOUT in the high-impedance state
Entire device on standby	FSX = low, FSR = low, $\overline{\text{PDN}}$ = high	8 mW	$\overline{\text{TSX}}$ and DOUT in the high-impedance state
Only transmit on standby	FSX = low, FSR = pulses, $\overline{\text{PDN}}$ = high	20 mW	$\overline{\text{TSX}}$ and DOUT in the high-impedance state within 5 frames
Only receive on standby	FSR = low, FSX = pulses, $\overline{\text{PDN}}$ = high	20 mW	Digital outputs active but not loaded

fixed-data-rate timing

Fixed-data-rate timing is selected by connecting DCLKR to V_{CC}. It uses the master clock (CLK), frame synchronization clocks (FSX and FSR), and the $\overline{\text{TSX}}$ output. FSX and FSR are inputs that set the sampling frequency. Data is transmitted on DOUT on the positive transitions of CLK following the rising edge of FSX. Data is received on DIN on the falling edges of CLK following FSR. A D/A conversion is performed on the received digital word, and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter. The data word is eight bits long in the companded mode and sixteen bits long in the linear mode.

variable-data-rate timing

Variable-data-rate timing is selected by connecting DCLKR to the receive data clock. In this mode, the master clock (CLK) controls the switched-capacitor filters, while data transfer into DIN and out of DOUT is controlled by DCLKR and DCLKX, respectively. This allows the data to be transferred into and out of the device at any rate up to the frequency of the master clock. DCLKR and DCLKX must be synchronous with CLK.

While the FSX input is high, data is transmitted from DOUT on consecutive positive transitions of DCLKX. Similarly, while the FSR input is high, the data word is received at DIN on consecutive negative transitions of DCLKR. The transmitted data word at DOUT is repeated in all remaining time slots in the frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the data word to be transmitted more than once per frame, is available only with variable-data-rate timing.

asynchronous operations

In order to avoid crosstalk problems associated with special interrupt circuits, the design includes separate converters, filters, and voltage references on the transmit and receive sides to allow completely independent operation of the two channels. In either timing mode, the master clock, data clock, and time slot strobe must be synchronized at the beginning of each frame.

precision voltage references

A precision band-gap reference voltage is generated internally and is used to supply all the references required for operation of both the transmit and receive channels. The gain in each channel is trimmed during the manufacturing process. This process ensures very accurate, stable gain performance over variations in supply voltage and device temperature.

conversion laws

The TCM320AC46 provides μ-law companding operation. The linear mode utilizes a 13-bit 2s complement format.

transmit operation

microphone input

The microphone input amplifier is designed to simplify interface to electret-type microphone elements as shown in Figure 1. The VMID buffer circuit provides a voltage (MICBIAS) equal to $V_{CC}/2$ as a reference for the microphone amplifier and a bias voltage to the electret microphone. The microphone amplifier output (MICGS) is used in conjunction with a feedback network to the amplifier inverting input (MICIN) to set the amplifier gain. VMID is brought out to provide a place to filter the VMID voltage.

microphone mute function

The $\overline{\text{MICMUTE}}$ input disables the microphone amplifier and attenuates the signal on the MICGS output to a level that is 80 dB or more down from the signal on the MICIN input. $\overline{\text{MICMUTE}}$ also causes the digital circuitry to transmit all zero code on DOUT.

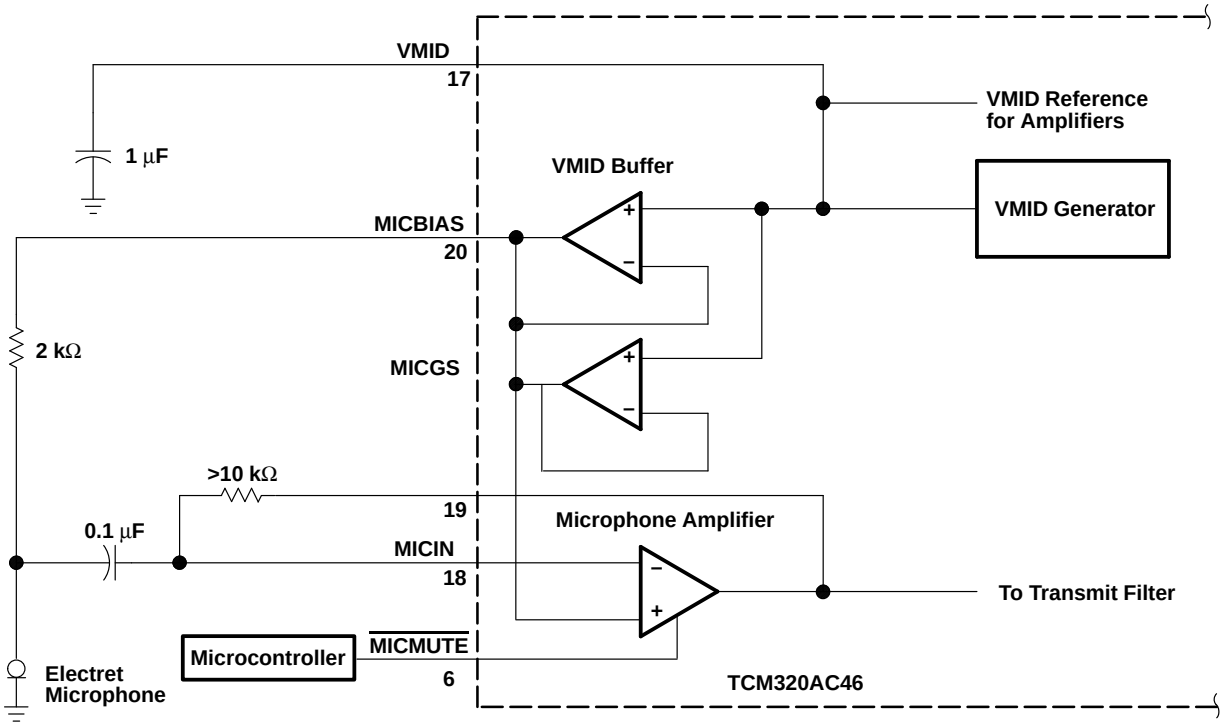


Figure 1. Typical Microphone Interface

transmit filter

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched-capacitor section of the transmit filter.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample-and-hold capacitor. The encoder performs an analog-to-digital conversion on a switched-capacitor array. Digital data representing the sample is transmitted on the first eight or 16 data clock cycles of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder using the sign-bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder.

data word structure

The data word is eight bits long in the companded mode. All eight bits represent one audio data sample. The sign bit is the first bit transmitted.

The data word is 16 bits long in the linear mode. The first 13 bits comprise the audio data sample, and the last three bits are volume control in the receive direction (DIN) and zeros in the transmit direction (DOUT). The sign bit is transmitted first.

receive operation

decoding

In the companded mode, the serial data word is received at DIN on the first eight clock cycles in fixed-data rate and the last eight clock cycles in variable-data rate. The serial data word is received at DIN on the first 13 clock cycles in the linear mode. Digital-to-analog conversion is performed, and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides pass-band flatness. The filter contains the required compensation for the (sin x)/x response of such decoders.

receive buffer

The receive buffer contains the volume control.

earphone amplifier

The earphone amplifier has a balanced output to allow maximum flexibility in output configuration. The output amplifier is designed to directly drive a piezo earphone in the differential configuration without any additional external components. The output can also be used to drive a single-ended load with the output signal voltage centered around $V_{CC}/2$.

The receive-channel output level can be adjusted between specified limits by connecting an external resistor network to EARGS.

receive data format

Eight bits of data are received in the companded mode and are valid. The sign bit is the first bit received (see Table 2).

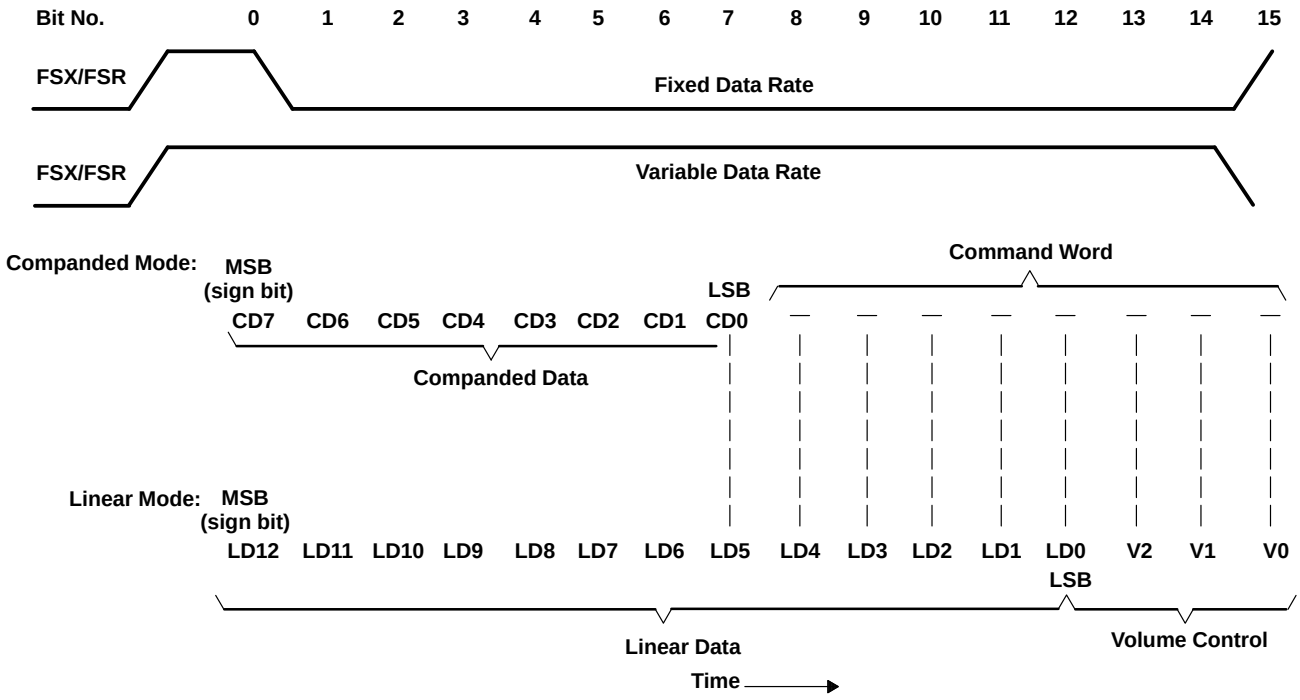
Sixteen bits of data are received in the linear mode. The first 13 bits are the D/A code, and the remaining three bits form the volume control word (see Table 2). The volume control function is actually an attenuation control where the first bit received is the most significant. The maximum volume occurs when all three volume control bits are zero. Eight levels of attenuation are selectable in 3-dB steps, giving a maximum attenuation of 21 dB, when all bits are 1s. The volume control bits are not latched into the device and must be present in each received data word.

Table 2. Receive Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
0	CD7	LD12
1	CD6	LD11
2	CD5	LD10
3	CD4	LD9
4	CD3	LD8
5	CD2	LD7
6	CD1	LD6
7	CD0	LD5
8	–	LD4
9	–	LD3
A	–	LD2
B	–	LD1
C	–	LD0
D	–	V2
E	–	V1
F	–	V0

relationship between data word and frame sync

Volume control and other control bits always follow the PCM data in time:



where:

CD7–CD0 = Data word when in companded mode
— = Unused bits in companded mode
V2, V1, V0 = Volume (attenuation control) 000 = maximum volume, 3 dBm0
111 = minimum volume, –18 dBm0
LD12–LD0 = Data word when in linear mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range at DOUT, V_O . . . . . –0.3 V to 7 V
Input voltage rangeat DIN, V_I . . . . . –0.3 V to 7 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage value is with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions (see Note 2)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (see Note 3)	4.5	5.5	V
High-level input voltage, V_{IH}	2.2		V
Low-level input voltage, V_{IL}		0.8	V
Load resistance between EARA and EARB, R_L (see Note 4)	50		Ω
Load capacitance between EARA and EARB, C_L (see Note 4)		113	nF
Operating free-air temperature, T_A	0	70	°C

NOTES: 2. To avoid possible damage to these CMOS devices and resulting reliability problems, the following sequence should be followed when applying power:
1. Connect to GND.
2. Connect V_{CC}.
3. Connect the input signals.

When removing power, follow the preceding steps in reverse order.
3. Voltages at analog inputs and outputs and V_{CC} are with respect to GND.
4. R_L and C_L should not be applied simultaneously.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

supply current, f_{DCLKR} or f_{DCLKX} = 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating	$\overline{PDN}$ is high with CLK signal present		14	mA
		Power down	$\overline{PDN}$ is low for 500 μs		1.5	
		Standby – both	$\overline{PDN}$ is high with FSX and FSR missing for 500 μs		2.5	
		Standby – one	$\overline{PDN}$ is high with FSX and FSR missing for 500 μs		10	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	I_{OH} = –3.2 mA, V_{CC} = 5 V	2.4	4.6		V
V_{OL}	Low-level output voltage		I_{OL} = 3.2 mA, V_{CC} = 5 V		0.2	0.4	V
I_{IH}	High-level input current	Any digital input	V_I = 2.2 V to V_{CC}			20	µA
I_{IL}	Low-level input current	Any digital input	V_I = 0 to 0.8 V			20	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

microphone interface‡

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage at MICIN		V_I = 0 to 5 V			±15	mV
I_{IB}	Input bias current at MICIN					±200	nA
B_1	Unity-gain bandwidth, open loop at MICIN				1		MHz
C_i	Input capacitance at MICIN					5	pF
A_V	Large-signal voltage amplification at MICGS					10000	V/V
	Output level at MICGS with $\overline{\text{MICMUTE}}$ active		V_I = 4 V			–80	dBm0
$I_{O(max)}$	Maximum output current	VMID		1			µA
		MICBIAS		1			mA

speaker interface‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{IL}	Input leakage at EARGS	V_I = 0 to 5 V			±300	nA
$V_{O(PP)}$	AC output voltage peak-to-peak				3	V_{PP}
V_{OO}	Output offset voltage at EARA, EARB (single-ended)	Relative to GND		100		mV
R_o	Output resistance at EARA, EARB			1		Ω
$I_{O(max)}$	Maximum output current	R_L = 600 Ω			±8	mA
A_V	Large-signal voltage amplification			4		V/V
	Gain change	$\overline{\text{EARMUTE}}$ low, max level when muted	–80			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ All parameters are measured between MICIN and GND (unless otherwise noted).

transmit gain and dynamic range, companded or linear mode, μ-law or A-law, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 5 and 6)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit reference-signal level (0 dB) (see Note 7)	Linear mode selected		1.001	Vrms
	Companded mode selected, μ-law		0.982	
Overload-signal level	Linear mode selected		4	V_{PP}
	Companded mode selected, μ-law		4	
Absolute gain error	0-dB input signal		±2	dB
Gain error with input level relative to gain at –10 dB	MICIN to DOUT at 3 dBm0 to –40 dBm0		±0.8	dB
	MICIN to DOUT at –41 dBm0 to –50 dBm0		±2	
	MICIN to DOUT at –51 dBm0 to –55 dBm0		±2.5	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

transmit filter transfer, linear mode or μ-law selected, over recommended ranges of supply voltage and free-air temperature, CLK = 2.048 MHz, FSX = 8 kHz (see Note 6)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input amplifier set for unity gain, noninverting maximum gain output signal at MICIN is 0 dB	Input signal = 50 Hz	–10	0	dB
		Input signal = 200 Hz	–1.8	0	
		Input signal = 300 Hz to 3 kHz		±0.35	
		Input signal = 3.3 kHz	–0.55	0.2	
		Input signal = 3.4 kHz	–2.8	0	
		Input signal = 4 kHz		–11	
		Input signal ≥4.6 kHz		–30	

transmit idle channel noise and distortion, companded mode, μ-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	MICIN connected to MICGS through a 10-kΩ resistor		27	dBrnC0
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –30 dBm0	32		dB
	MICIN to DOUT at –31 dBm0 to –40 dBm0	25		
	MICIN to DOUT at–41 dBm0 to –45 dBm0	18		

transmit idle channel noise and distortion, linear mode, over recommended ranges of supply voltage and operating free-air temperature (see Notes 6 and 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise	MICIN connected to MICGS through a 10-kΩ resistor		–60	dB
Transmit signal-to-distortion ratio with sine-wave input	MICIN to DOUT at 0 dBm0 to –6 dBm0	47		dB
	MICIN to DOUT at –7 dBm0 to –12 dBm0	42		
	MICIN to DOUT at –13 dBm0 to –18 dBm0	38		
	MICIN to DOUT at –19 dBm0 to –24 dBm0	30		
	MICIN to DOUT at –25 dBm0 to –45 dBm0	15		

NOTES: 5. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
6. The input amplifier is set for inverting unity gain.
7. This reference-level signal, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 2 V.
8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).

receive gain and dynamic range, linear mode, μ-law or A-law, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive reference-signal level (0 dB) (see Note 11)	Linear mode selected		0.751	Vrms
	Companded mode selected, μ-law		0.736	
Overload-signal level	Linear mode selected		3	V_{PP}
	Companded mode selected, μ-law		3	
Absolute gain error	0-dB input signal		±2	dB
Gain error with output level relative to gain at –10 dBm0	DIN to EARA and EARB at 3 dBm0 to –40 dBm0		±0.8	dB
	DIN to EARA and EARB at –41 dBm0 to –50 dBm0		±2	
	DIN to EARA and EARB at –51 dBm0 to –55 dBm0		±2.5	
Gain variation	V_{CC} ±10%, T_A = 0°C to 70°C		±0.5	dB

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz	Input signal at DIN is 0 dBm0	Input signal = < 200 Hz		0.35	dB
		Input signal = 200 Hz	–0.8	0.35	
		Input signal = 300 Hz to 3 kHz		±0.35	
		Input signal = 3.3 kHz	–0.55	0.2	
		Input signal = 3.4 kHz	–2	0	
		Input signal = 4 kHz		–11	
		Input signal > 4.6 kHz		–28	

receive idle channel noise and distortion, companded mode, μ-law, over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise, C-message weighted	DIN = 11111111		17	dBrnC0
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –30 dBm0	32		dB
	DIN to EARA and EARB at –31 dBm0 to –40 dBm0	25		
	DIN to EARA and EARB at –41 dBm0 to –45 dBm0	18		

receive idle channel noise and distortion, linear mode over recommended ranges of supply voltage and operating free-air temperature (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Receive noise	DIN = 00000000(linear)		–60	dB
Receive signal-to-distortion ratio with sine-wave input	DIN to EARA and EARB at 0 dBm0 to –6 dBm0	48		dB
	DIN to EARA and EARB at –6 dBm0 to –12 dBm0	42		
	DIN to EARA and EARB at –13 dBm0 to –18 dBm0	38		
	DIN to EARA and EARB at –19 dBm0 to –24 dBm0	30		
	DIN to EARA and EARB at –25 dBm0 to –45 dBm0	14		

NOTES: 8. Transmit noise, linear mode: 200 μVrms is equivalent to –74 dB (referenced to device 0-dB level).
9. Receive output is measured differentially in the maximum gain configuration. To set the output amplifier for maximum gain, EARGS is connected to EARB and the output is taken between EARA and EARB. All output levels are (sin x)/x corrected.
10. Unless otherwise noted, the digital input is a word stream generated by passing a 0-dB sine wave at 1020 Hz through an ideal encoder where 0 dB is defined as the zero reference.
11. This reference-signal level is measured at the speaker output of the receive channel with the gain of the output speaker amplifier set to unity.

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Supply voltage rejection ratio, transmit channel	Idle channel, supply signal = 100 mVrms, f = 0 to 30 kHz (measured at DOUT)		–30		dB
Supply voltage rejection ratio, receive channel	Idle channel, supply signal = 100 mVrms, EARGS connected to EARB, f = 0 to 30 kHz (measured differentially between EARA and EARB)		–30		dB
Crosstalk attenuation, transmit-to-receive (differential)	MICIN = 0 dB, f = 1.02 kHz, unity transmit gain, EARGS connected to EARB, measured differentially between EARA and EARB	55			dB
Crosstalk attenuation, receive-to-transmit	DIN = 0 dBm0, f = 1.02 kHz, unity transmit gain, measured at DOUT	55			dB

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 2, 3, 4, and 5)

		MIN	TYP†	MAX	UNIT
t_t	Transition time, CLK and DCLK			10	ns
	Duty cycle, CLK	45%	50%	55%	
	Duty cycle, DCLK	45%	50%	55%	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 3)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	20	468	ns
$t_{h(FSX)}$	Hold time, FSX	20	468	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see Figure 2)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	20	468	ns
$t_{h(FSR)}$	Hold time, FSR	20	468	ns
$t_{su(DIN)}$	Setup time, DIN	20		ns
$t_{h(DIN)}$	Hold time, DIN	20		ns

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 5)

		MIN	MAX	UNIT
$t_{su(FSX)}$	Setup time, FSX	40	$t_{c(DCLKX)}$–40	ns
$t_{h(FSX)}$	Hold time, FSX	35	$t_{c(DCLKX)}$–35	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see Figure 4)

		MIN	MAX	UNIT
$t_{su(FSR)}$	Setup time, FSR	40		ns
$t_{h(FSR)}$	Hold time, FSR	35	$t_{c(DCLKR)}-35$	ns
$t_{su(DIN)}$	Setup time, DIN	30		ns
$t_{h(DIN)}$	Hold time, DIN	30		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode, C_L = 0 to 10 pF (see Figures 2 and 3)

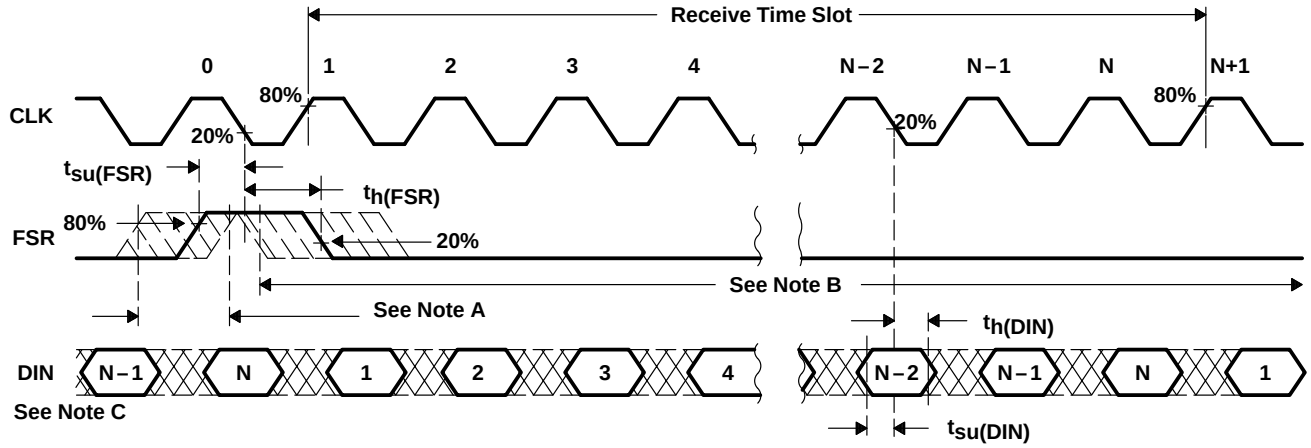
		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From CLK bIt 1 high to DOUT bit 1 valid			35	ns
t_{pd2}	From CLK high to DOUT valid, bits 2 to n			35	ns
t_{pd3}	From CLK bit n low to DOUT bit n Hi-Z		30		ns
t_{pd4}	From CLK bit 1 high to $\overline{TSX}$ active (low)	R_{pullup} = 1.24 kΩ		40	ns
t_{pd5}	From CLK bit n low to FSX inactive (high)	R_{pullup} = 1.24 kΩ	30		ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Figures 4 and 5)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd6}	FSX high to DOUT bit 1 valid	C_L = 0 to 10 pF		30	ns
t_{pd7}	DCLKX high to DOUT valid, bits 2 to n	C_L = 0 to 10 pF		40	ns
t_{pd8}	FSX low to DOUT bit n Hi-Z		20		ns

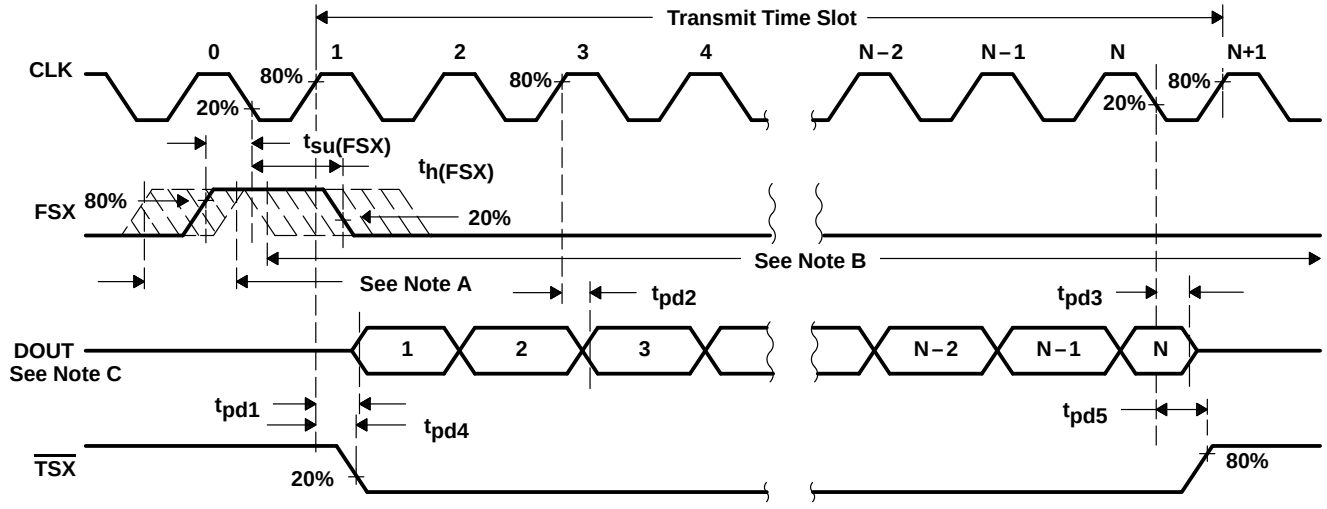
PARAMETER MEASUREMENT INFORMATION

All timing parameters are referenced to V_{IH} and V_{IL}. Bit 1 = MSB (most significant bit) and is clocked in first on DIN or clocked out first on DOUT. Bit n = LSB (least significant bit) and is clocked in last on DIN or is clocked out last on DOUT. N = 8 for the companded mode, and N = 16 for the linear mode.



NOTES: A. This window is allowed for FSR high.
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

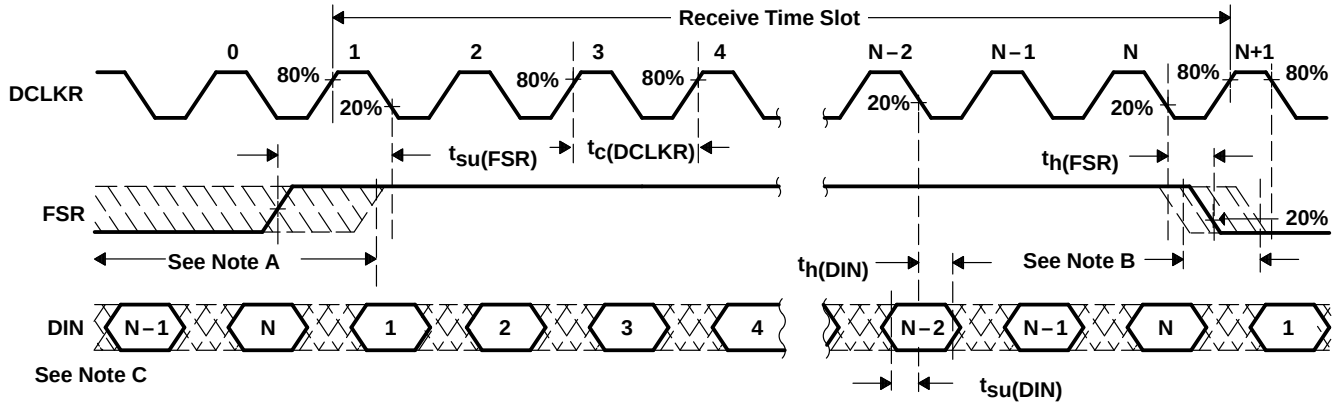
Figure 2. Fixed-Data-Rate, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low ($t_{h(FSX)}$ max determined by data collision considerations).
C. Transitions are measured at 50%.

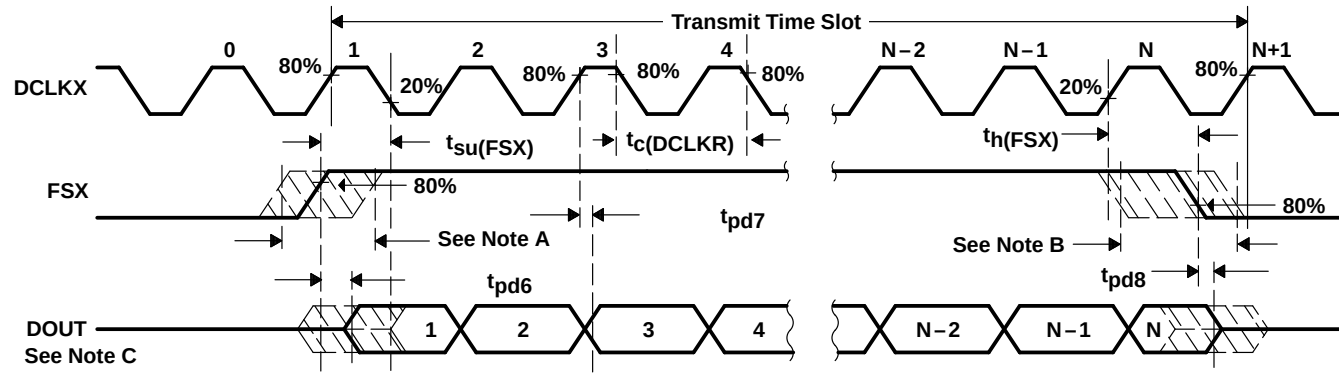
Figure 3. Fixed-Data-Rate, Transmit Side Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This window is allowed for FSR high ($t_{su(FSR)}$ max determined by data collision considerations).
B. This window is allowed for FSR low.
C. Transitions are measured at 50%.

Figure 4. Variable-Data-Rate, Receive Side Timing Diagram



NOTES: A. This window is allowed for FSX high.
B. This window is allowed for FSX low without data repetition.
C. Transitions are measured at 50%.

Figure 5. Variable-Data-Rate, Transmit Side Timing Diagram

APPLICATION INFORMATION

output gain set design considerations (see Figure 6)

EARA and EARB are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at EARA
V_{O-} at EARB
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to EARGS.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination R1 + R2 and R_L sets the total loading. The total capacitance at EARGS and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

APPLICATION INFORMATION

V_A represents the maximum available digital mW output response (V_A = 1.06 Vrms).

$$V_{OD} = A \times V_A$$

$$\text{where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

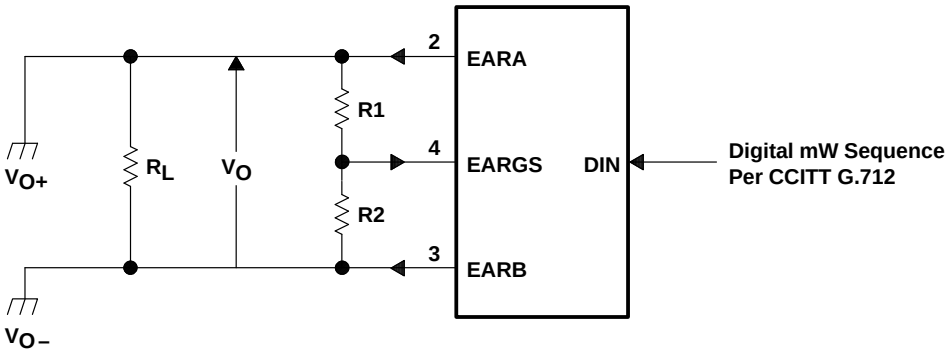


Figure 6. Gain-Setting Configuration

higher clock frequencies and sample rates

The TCM320AC46 is designed to work with sample rates up to 24 kHz where the frequency of the frame sync determines the sampling frequency. However, there is a fundamental requirement to maintain the ratio of master clock frequency, f_{CLK}, to frame sync frequency, f_{FSR}/f_{FSX}. This ratio for the device is 2.048 MHz/8 kHz or 256 master clocks per frame sync. For example, to operate the TCM320AC46 at a sampling rate of f_{FSR} and f_{FSX} equal to 16 kHz, f_{CLK} must be 256 times 16 kHz, or 4.096 MHz. If the TCM320AC46 is operated above an 8-kHz sample rate, however, it is expected that the performance will be degraded.

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