CMOS Digital Integrated Circuits Silicon Monolithic

TC7USB221WBG

1. Functional Description

- Dual SPDT USB Switch

2. General

The TC7USB221WBG is high-speed CMOS dual 1-2 multiplexer/demultiplexer. The low ON-resistance and the low capacitance of the switch allow connections to USB application.

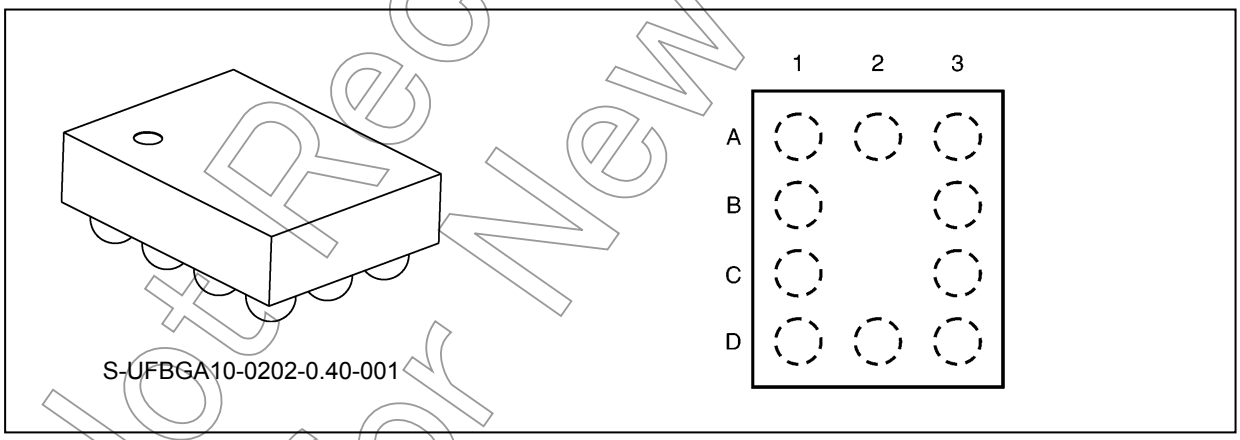
This device consists of dual individual two-inputs multiplexer/demultiplexer with common select input (S) and output enable ($\overline{OE}$). The D+/D- inputs is connected to the 1D+/1D- or 2D+/2D- outputs determined by the combination both the select input (S) and output enable ($\overline{OE}$). When the output enable ($\overline{OE}$) input is held high level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

3. Features

(1) Supply voltage: V_{CC} = 2.3 to 3.6 V
(2) Switch terminal ON-capacitance: $C_{I/O}$ = 7 pF Switch ON (typ.) @V_{CC} = 3.3 V
(3) ON-resistance: R_{ON} = 6.5 Ω (typ.) @V_{CC} = 3 V, V_{IS} = 0 V
(4) R_{ON} flatness: $R_{ON(flat)}$ = 1.6 Ω (typ.)@V_{CC} = 3 V
(5) Difference of ON-resistance between switches: ΔR_{ON} = 0.5 Ω (typ.)@V_{CC} = 3 V
(6) ESD performance: Machine model ≥ ±200 V, Human body model ≥ ±2000 V
(7) Power-down protection provided on all inputs and outputs.
(8) Package: WCSP10B

4. Packaging and Pin Assignment (Top View)



S-UFBGA10-0202-0.40-001

4.1. Pin Assignment

	1	2	3
A	1D+	V_{CC}	S
B	1D-	No Ball	D+
C	2D+	No Ball	D-
D	2D-	GND	$\overline{OE}$

5. Marking

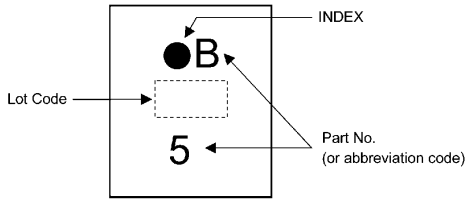


Fig. 5.1 Marking

6. Block Diagram

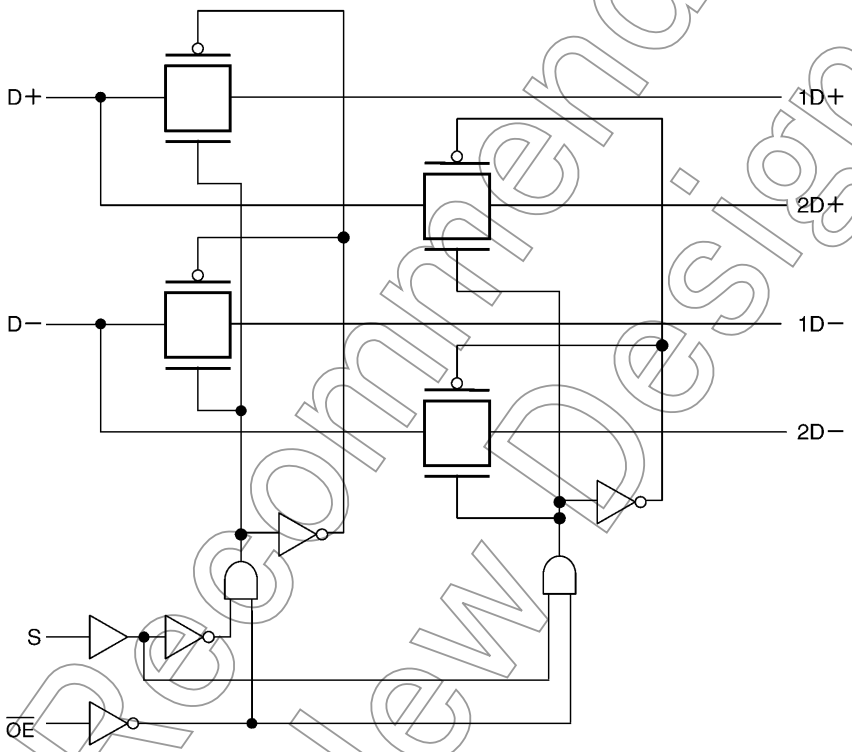


Fig. 6.1 Block Diagram

7. Principle of Operation

7.1. Truth Table

Input $\overline{OE}$	Input S	Function
L	L	D+ port = 1D+ port, D- Port = 1D- Port
L	H	D+ port = 2D+ port, D- Port = 2D- Port
H	X	Disconnect

8. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}		—	-0.5 to 4.6	V
Input voltage ($\overline{OE}$, S)	V_{IN}			-0.5 to 4.6	
Switch I/O voltage	V_S		V_{CC} = 0 V or Switch OFF	-0.5 to 4.6	
			Switch ON	0.5 to V_{CC} +0.5	
Clamp diode current	I_{IK}		Control input	-50	mA
			Switch	±50	
Switch I/O current	I_S		—	50	
Power dissipation	P_D			150	mW
V_{CC}/ground current	I_{CC}/I_{GND}			±100	mA
Storage temperature	T_{stg}			-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

9. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}		—	2.3 to 3.6	V
Input voltage ($\overline{OE}$, S)	V_{IN}			0 to 3.6	
Switch I/O voltage	V_S		V_{CC} = 0 V or Switch OFF	0 to 3.6	
			Switch ON	0 to V_{CC}	
Operating temperature	T_{opr}		—	-40 to 85	°C
Input rise time	dt/dv			0 to 10	ns/V
Input fall time				0 to 10	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND.

10. Electrical Characteristics

10.1. DC Characteristics (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage ($\overline{OE}$, S)	V_{IH}		—	2.3 to 3.6	0.46 × V_{CC}	—	—	V
Low-level input voltage ($\overline{OE}$, S)	V_{IL}		—	2.3 to 3.6	—	—	0.25 × V_{CC}	
Input leakage current ($\overline{OE}$, S)	I_{IN}		V_{IN} = 0 to 3.6 V	2.3 to 3.6	—	—	±1.0	μA
Power-OFF leakage current	I_{OFF}		V_{IN} = V_{IS} = 0 to 3.6 V	0	—	—	±5.0	
Switch OFF-state leakage current	I_{SZ}		V_{IS} = 0 to V_{CC}, $\overline{OE}$ = V_{CC}	2.3 to 3.6	—	—	±5.0	
ON-resistance	R_{ON}	(Note 1), (Note 2)	V_{IS} = 0 V, I_{IS} = 30 mA	3.0	—	6.5	10	Ω
			V_{IS} = 0.4 V, I_{IS} = 30 mA	3.0	—	7	11	
			V_{IS} = 3.0 V, I_{IS} = 30 mA	3.0	—	13	19	
Difference of ON-resistance between switches	ΔR_{ON}		V_{IS} = 0.4 V, 1.0 V, I_{IS} = 30 mA	3.0	—	0.5	—	
ON-resistance flatness	$R_{ON(flat)}$		V_{IS} = 0 V to 1.0 V, I_{IS} = 30 mA	3.0	—	1.6	—	
Quiescent supply current	I_{CC}		V_{IN} = V_{CC} or GND, I_{OUT} = 0 A	3.6	—	—	2.0	μA
	ΔI_{CC}		V_{IN} = 1.8 V (one input)	3.6	—	—	10.0	

Note 1: All typical values are at T_a = 25°C.

Note 2: Measured by the voltage drop between D+/D- and 1D+/1D-,2D+/2D- pins at the indicated current through the switch. On-resistance is determined by the lower of the voltages on the two pins.

10.2. AC Characteristics (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Propagation delay time	t_{PLH}/t_{PHL}	(Note 1)	C_L = 5 pF, See Fig. 11.1	3.3 ± 0.3	—	0.25	—	ns
Turn-ON time (S, $\overline{OE}$ to output)	t_{on}		R_L = 50 Ω, C_L = 5 pF, See Fig. 11.2		—	7.5	17	
Turn-OFF time (S, $\overline{OE}$ to output)	t_{off}				—	3.3	10	
Break before Make	TBBM		R_L = 50 Ω, C_L = 5 pF, See Fig. 11.3		2	—	7.0	
Skew of opposite transitions of the same output (t_{PHL} - t_{PLH})	$t_{SK(P)}$	(Note 1)	C_L = 5 pF, See Fig. 11.4		—	0.1	—	
Output skew (center port to any other port)	$t_{SK(O)}$	(Note 1)	C_L = 5 pF, See Fig. 11.5		—	0.1	—	

Note 1: Parameter guaranteed by design.

10.3. Analog Switch (Note) (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
OFF isolation (non-adjacent)	OIRR		R_T = 50 Ω, f = 240 MHz, See Fig. 11.6	3.3 ± 0.3	—	-36	—	dB
Crosstalk (non-adjacent)	Xtalk		R_T = 50 Ω, f = 240 MHz, See Fig. 11.7		—	-36	—	
-3dB Bandwidth	BW		R_L = 50 Ω, CL = 0 pF, See Fig. 11.8		—	820	—	MHz

Note: Parameter guaranteed by design.

10.4. Capacitive Characteristics (Note) (Unless otherwise specified, T_a = 25°C)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance ($\overline{OE}$, S)	C_{IN}		V_{IN} = 0 V	3.3	4	pF
Switch terminal OFF-capacitance (D+, D-)	$C_{I/O}$		$\overline{OE}$ = V_{CC}, V_{IS} = 0 V		4	
Switch terminal OFF-capacitance (1D+, 1D-, 2D+, 2D-)					3	
Switch terminal ON-capacitance			$\overline{OE}$ = GND, V_{IS} = 0 V		7	

Note: Parameter guaranteed by design.

11. AC Test Circuits and Waveforms

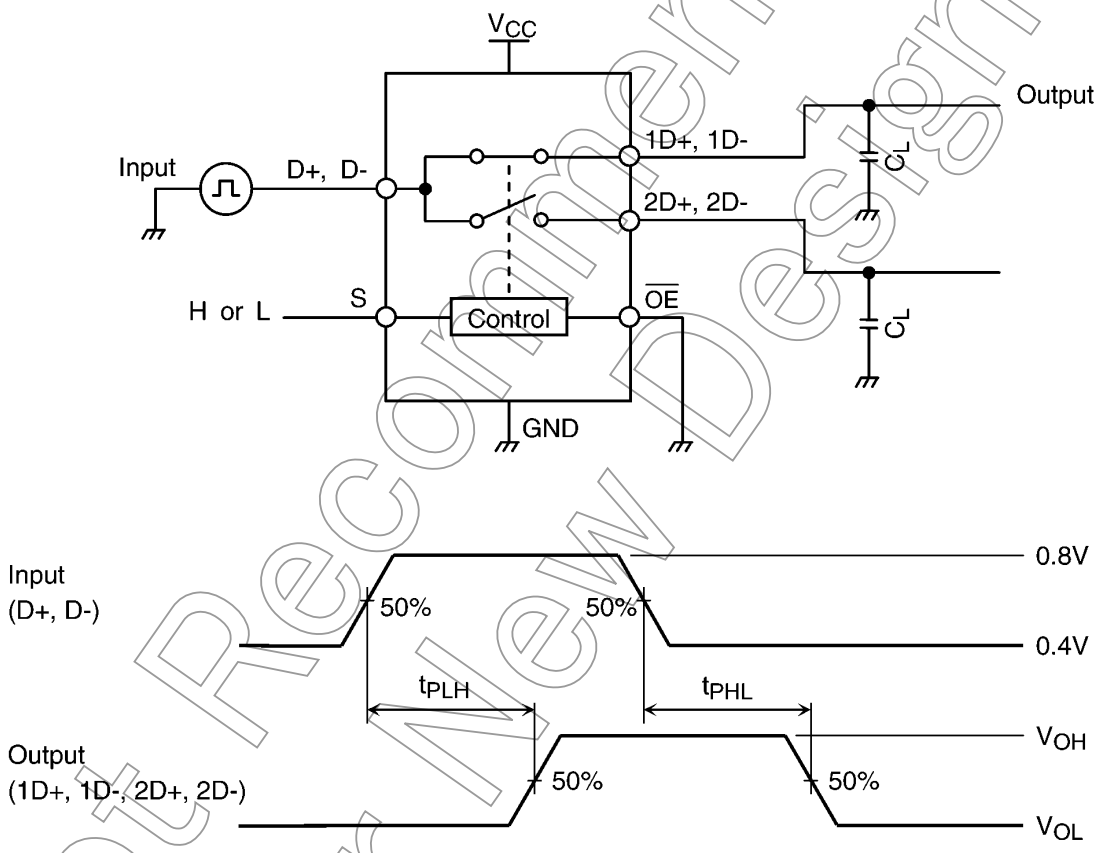


Fig. 11.1 Propagation Delay Time (t_{PLH}, t_{PHL})

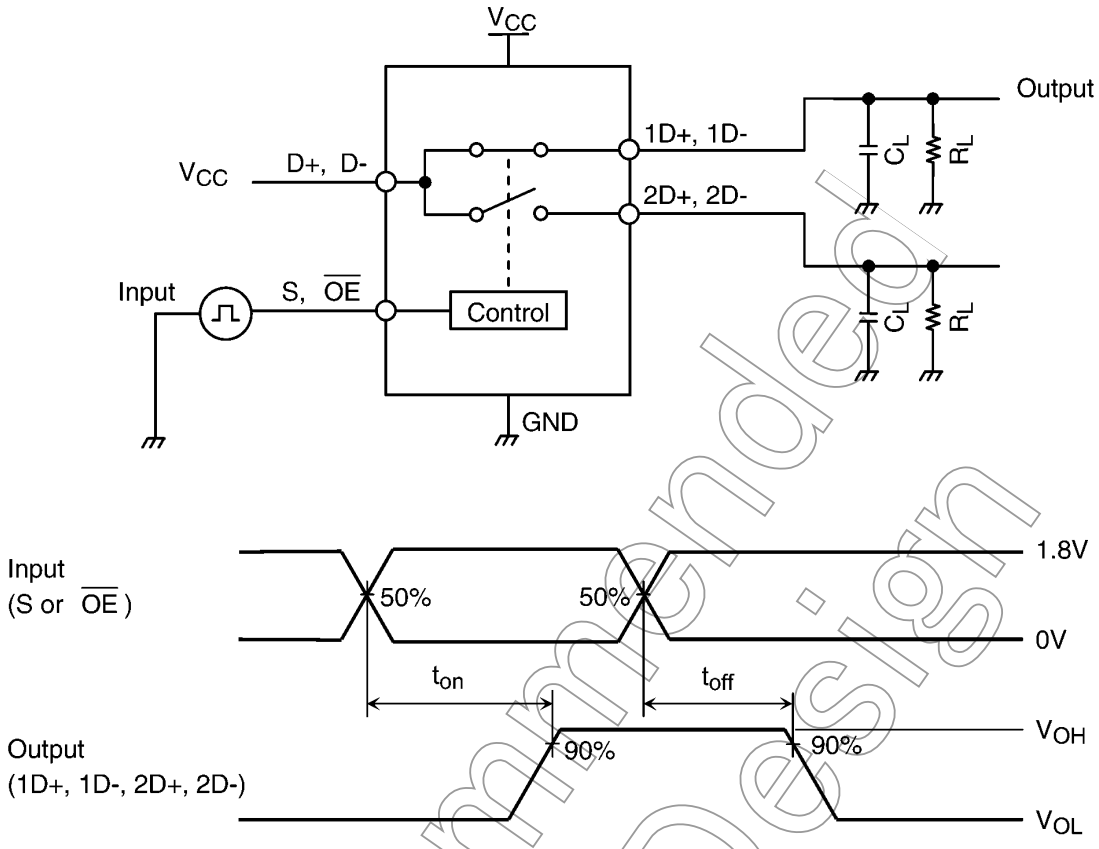


Fig. 11.2 Turn-ON and Turn-OFF Times (t_{on}, t_{off})

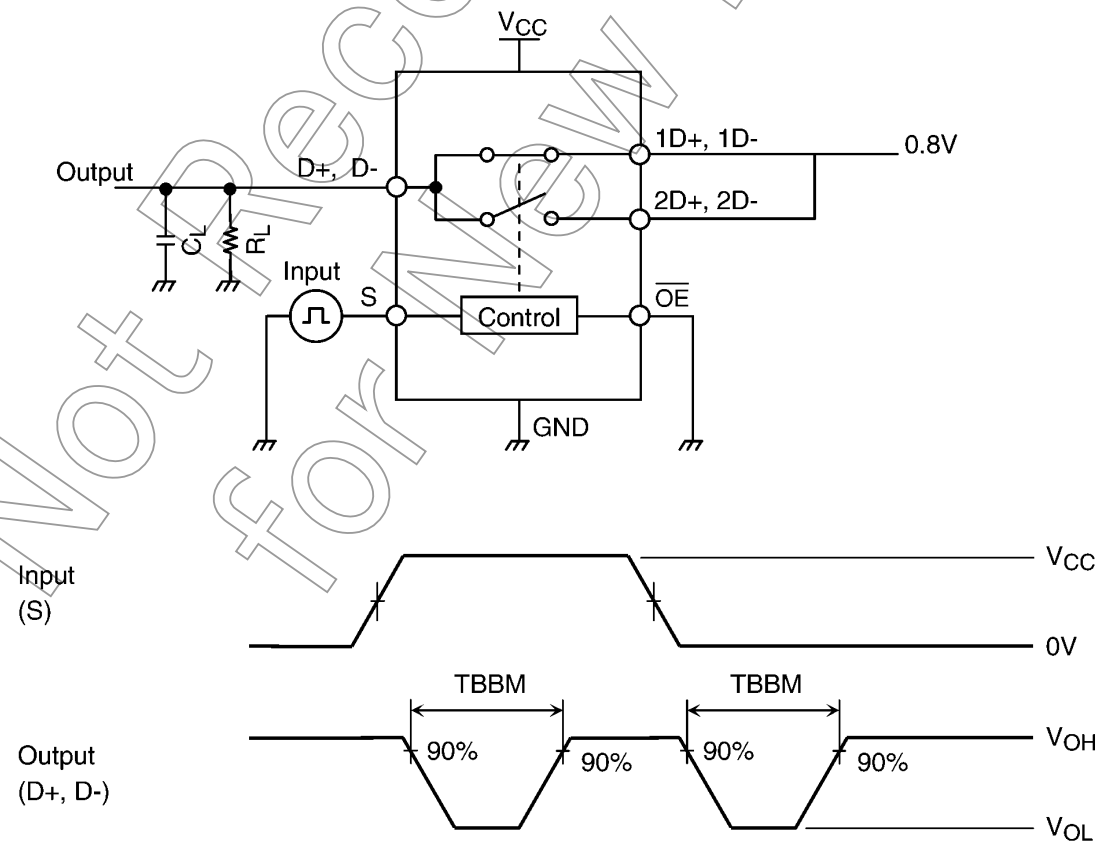


Fig. 11.3 Break Before Make (TBBM)

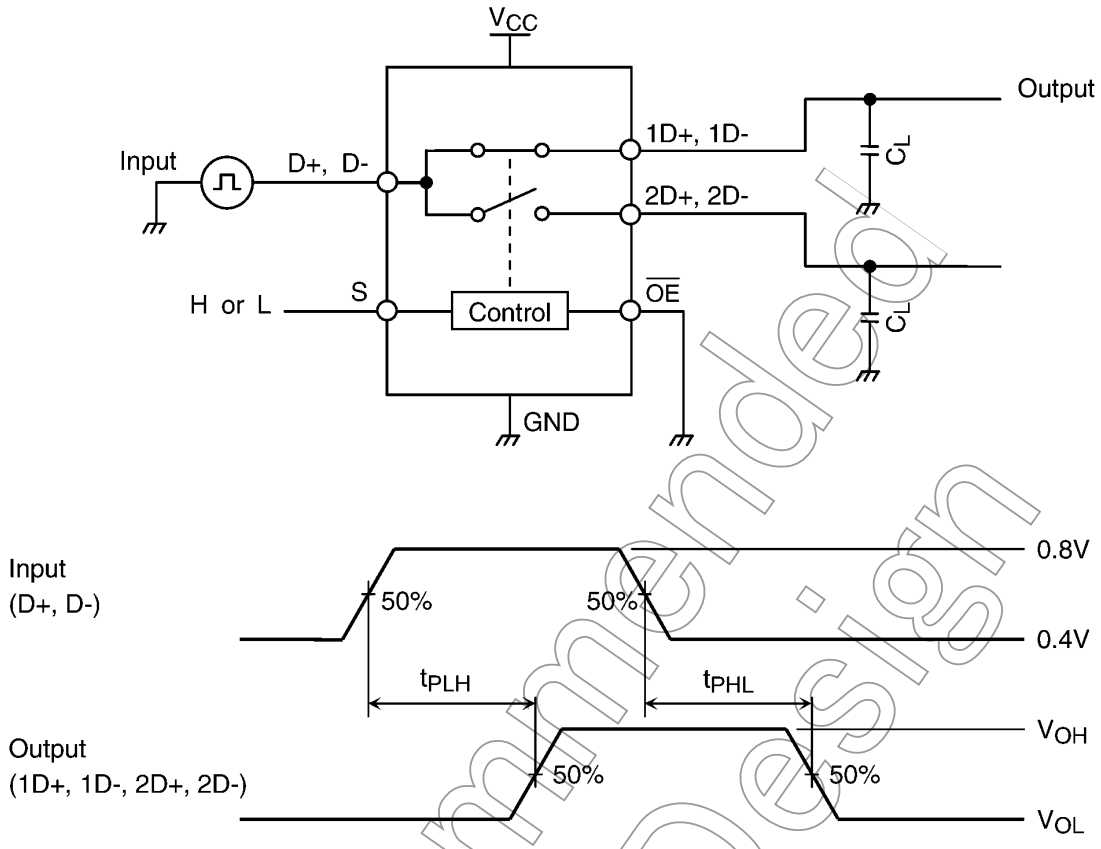


Fig. 11.4 Skew of opposite transitions of the same output (t_{PHL} - t_{PLH})

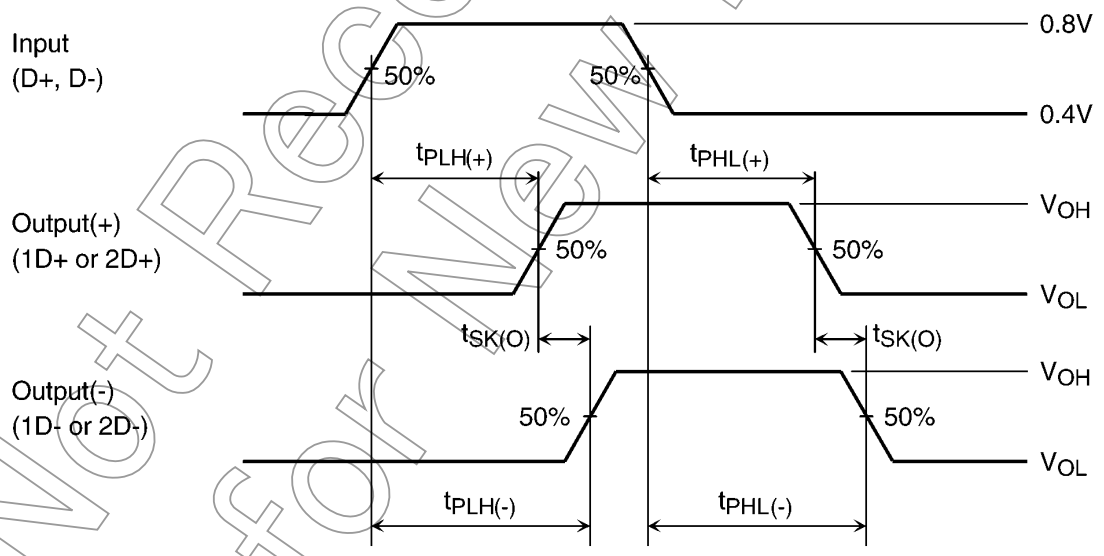


Fig. 11.5 Output Skew (center port to any other port)

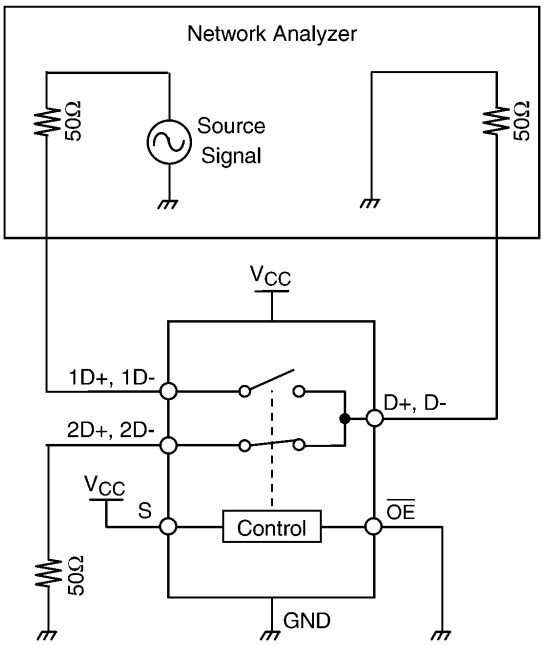


Fig. 11.6 OFF Isolation

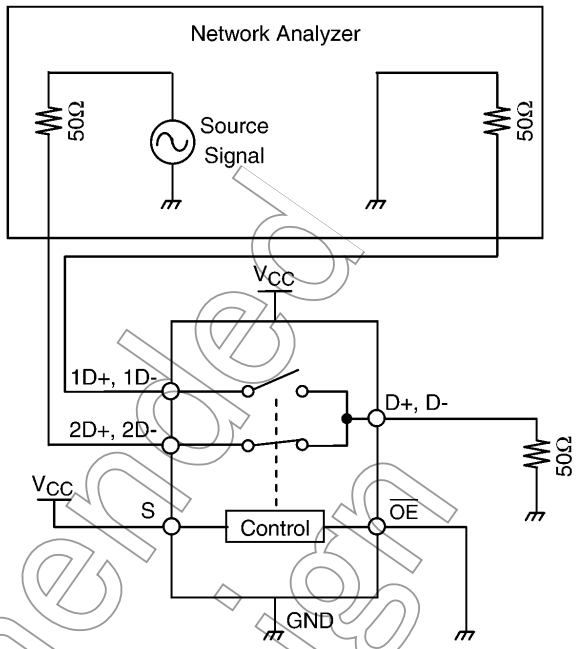


Fig. 11.7 Crosstalk

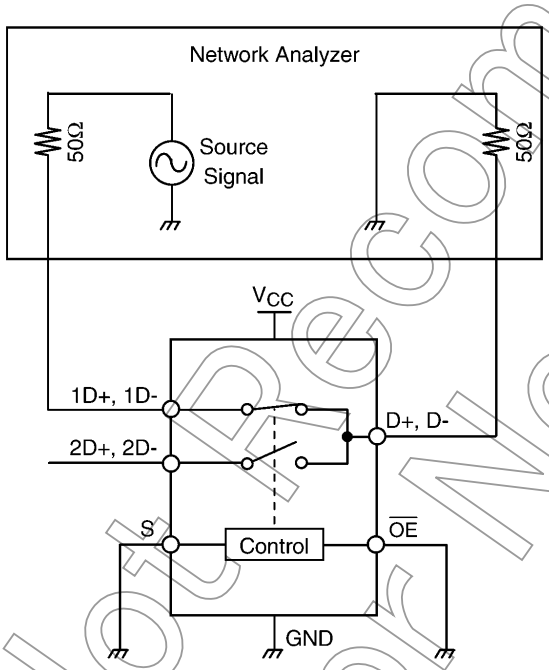


Fig. 11.8 -3dB Bandwidth

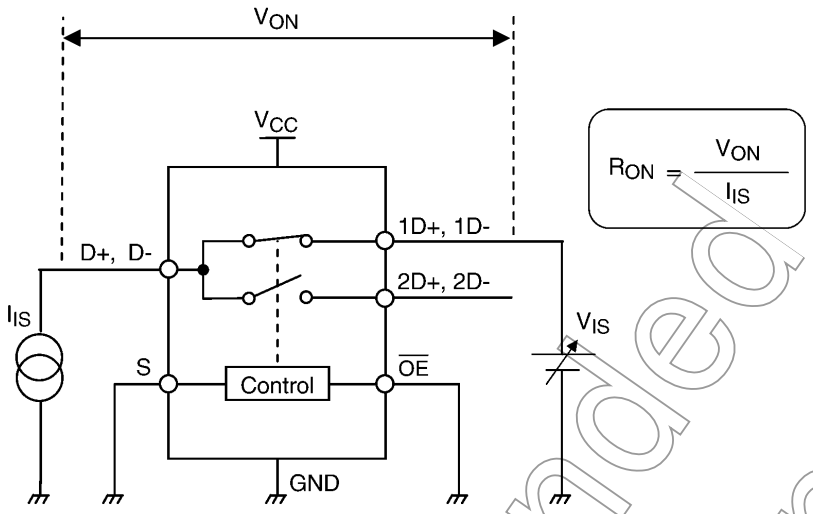


Fig. 11.9 ON-Resistance

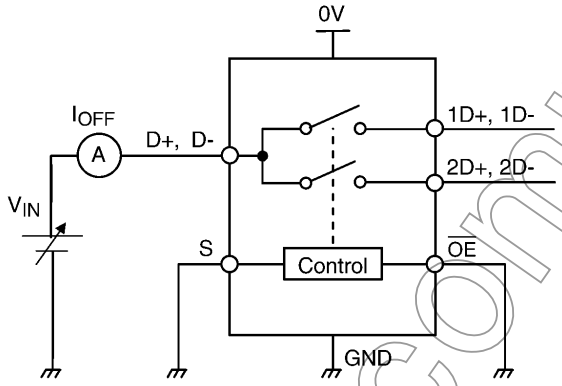


Fig. 11.10 Power-OFF Leakage Current

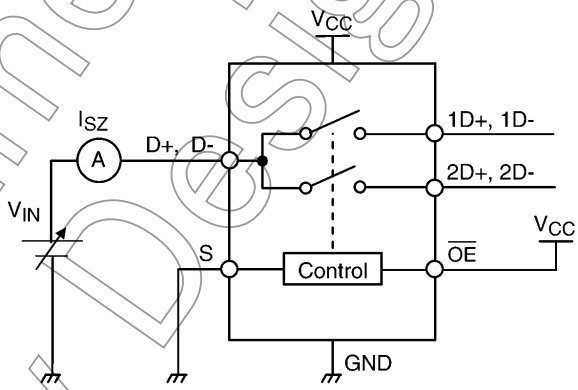
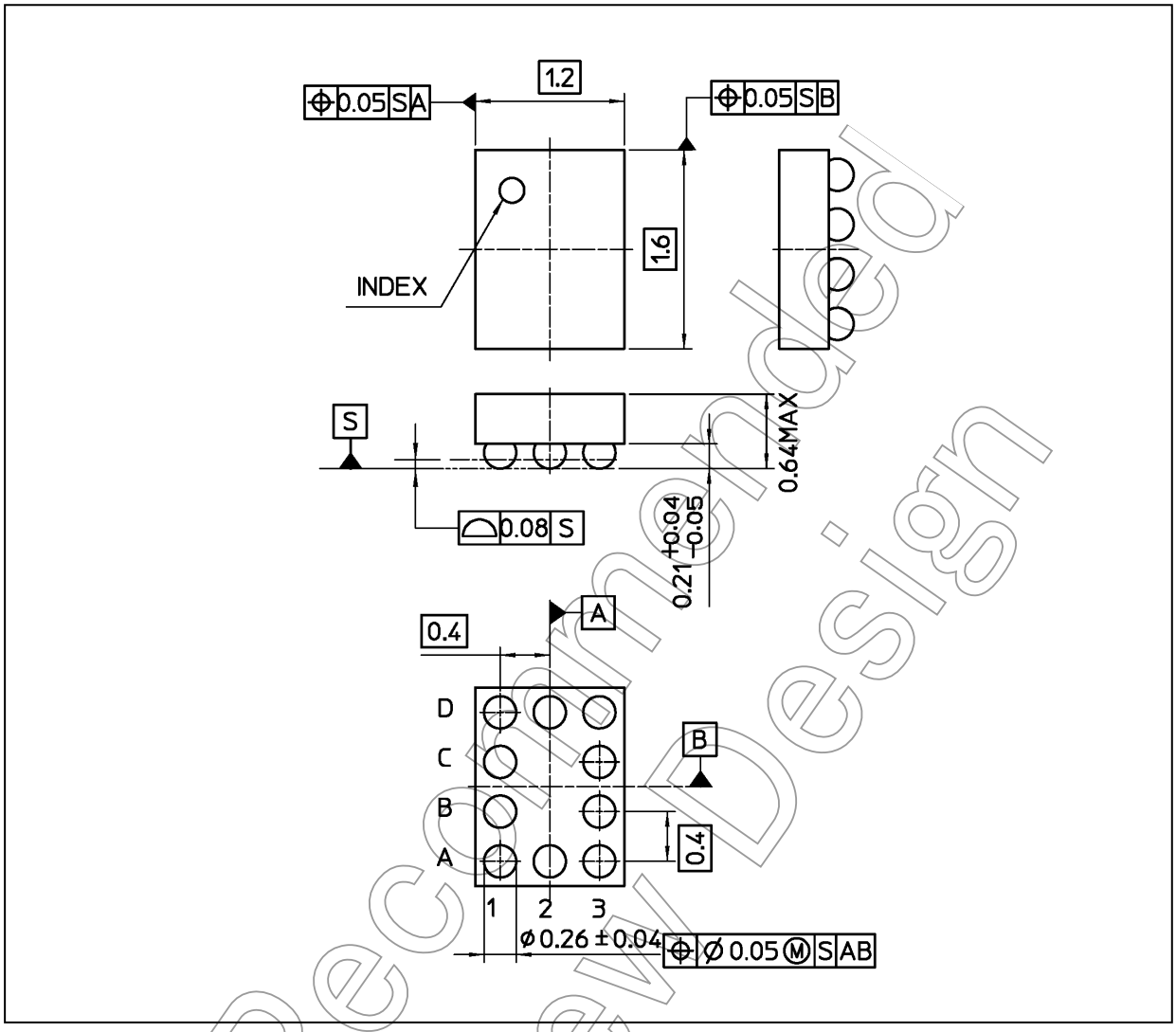


Fig. 11.11 Switch OFF-state leakage current

Package Dimensions

Unit: mm



This resins used in this product include no flame retardants.

Weight: 0.0025 g (typ.)

Package Name(s)
TOSHIBA: S-UFBGA10-0202-0.40-001
Nickname: WCSP10B

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