

TC74VHCT573AF, TC74VHCT573AFW, TC74VHCT573AFT

Octal D-Type Latch with 3-State Output

The TC74VHCT573A is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

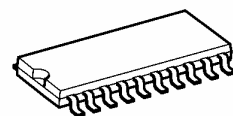
Note: Output in off-state

Features

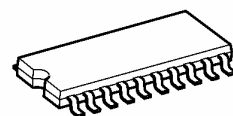
- High speed: $t_{pd} = 7.7$ ns (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs: $V_{IL} = 0.8$ V (max)
 $V_{IH} = 2.0$ V (min)
- Power down protection is provided on all inputs and outputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low noise: $V_{OLP} = 1.6$ V (max)
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 573 type.

Note: xxxFW (JEDEC SOP) is not available in Japan.

TC74VHCT573AF

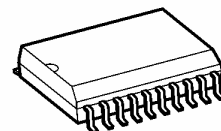


SOP20-P-300-1.27A



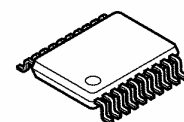
SOP20-P-300-1.27

TC74VHCT573AFW



SOL20-P-300-1.27

TC74VHCT573AFT

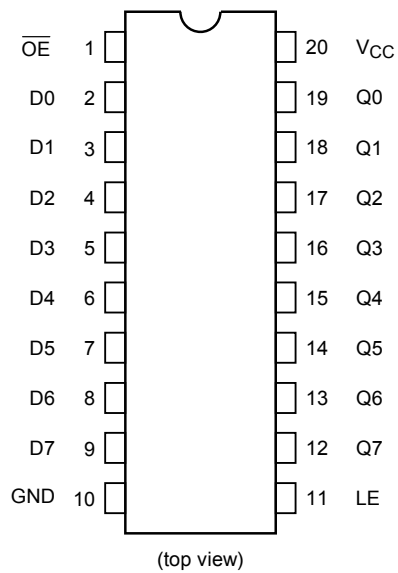


TSSOP20-P-0044-0.65A

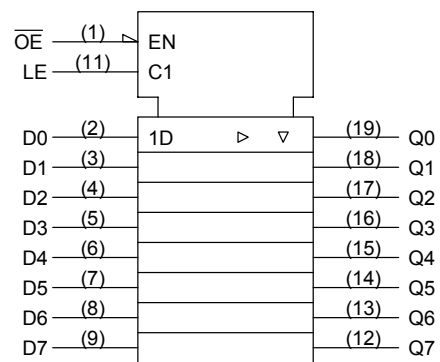
Weight

SOP20-P-300-1.27A	: 0.22 g (typ.)
SOP20-P-300-1.27	: 0.22 g (typ.)
SOL20-P-300-1.27	: 0.46 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

Pin Assignment



IEC Logic Symbol



Truth Table

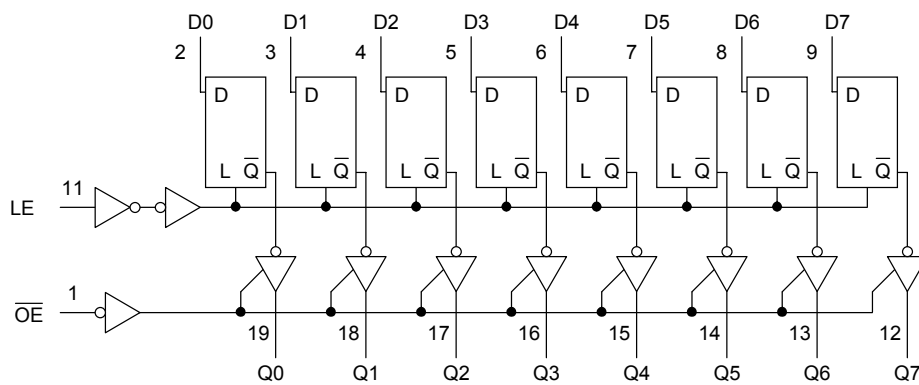
Inputs			Output
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20 (Note 4)	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: Output in off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5 (Note 2)	V
		0 to V_{CC} (Note 3)	
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 20	ns/V

Note 1: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Output in off-state

Note 3: High or low state

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
				V _{CC} (V)	Min	Typ.	Max	Min	Max
High-level input voltage	V _{IH}	—	4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V _{IL}	—	4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 µA	4.5	4.40	4.50	—	4.40	—
			I _{OH} = -8 mA	4.5	3.94	—	—	3.80	—
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	4.5	—	0.0	0.1	—	0.1
			I _{OL} = 8 mA	4.5	—	—	0.36	—	0.44
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	±0.25	—	±2.50	µA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	µA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0	µA
	I _{CCT}	Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND	5.5	—	—	1.35	—	1.50	mA
Output leakage current	I _{OPD}	V _{OUT} = 5.5 V	0	—	—	0.5	—	5.0	µA

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
				V _{CC} (V)	Typ.	Limit	
Minimum pulse width (LE)	t _w (H)	—	5.0 ± 0.5	—	6.5	8.5	ns
Minimum set-up time	t _s	—	5.0 ± 0.5	—	1.5	1.5	ns
Minimum hold time	t _h	—	5.0 ± 0.5	—	3.5	3.5	ns

AC Characteristics (input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (LE-Q)	t _{pLH}	—	5.0 ± 0.5	15	—	7.7	12.3	1.0	13.5	ns
	t _{pHL}			50	—	8.5	13.3	1.0	14.5	
Propagation delay time (D-Q)	t _{pLH}	—	5.0 ± 0.5	15	—	5.1	8.5	1.0	9.5	ns
	t _{pHL}			50	—	5.9	9.5	1.0	10.5	
3-state output enable time	t _{pZL}	R _L = 1 kΩ	5.0 ± 0.5	15	—	6.3	10.9	1.0	12.5	ns
	t _{pZH}			50	—	7.1	11.9	1.0	13.5	
3-state output disable time	t _{pLZ} t _{pHZ}	R _L = 1 kΩ	5.0 ± 0.5	50	—	8.8	11.2	1.0	12.0	ns
Output to output skew	t _{osLH} t _{osHL}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	C _{IN}	—			—	4	10	—	10	pF
Output capacitance	C _{OUT}	—			—	9	—	—	—	pF
Power dissipation capacitance	C _{PD}	(Note 2)			—	25	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 14 + 11 \cdot n$$

Noise Characteristics (input: $t_r = t_f = 3\text{ ns}$) (Note)

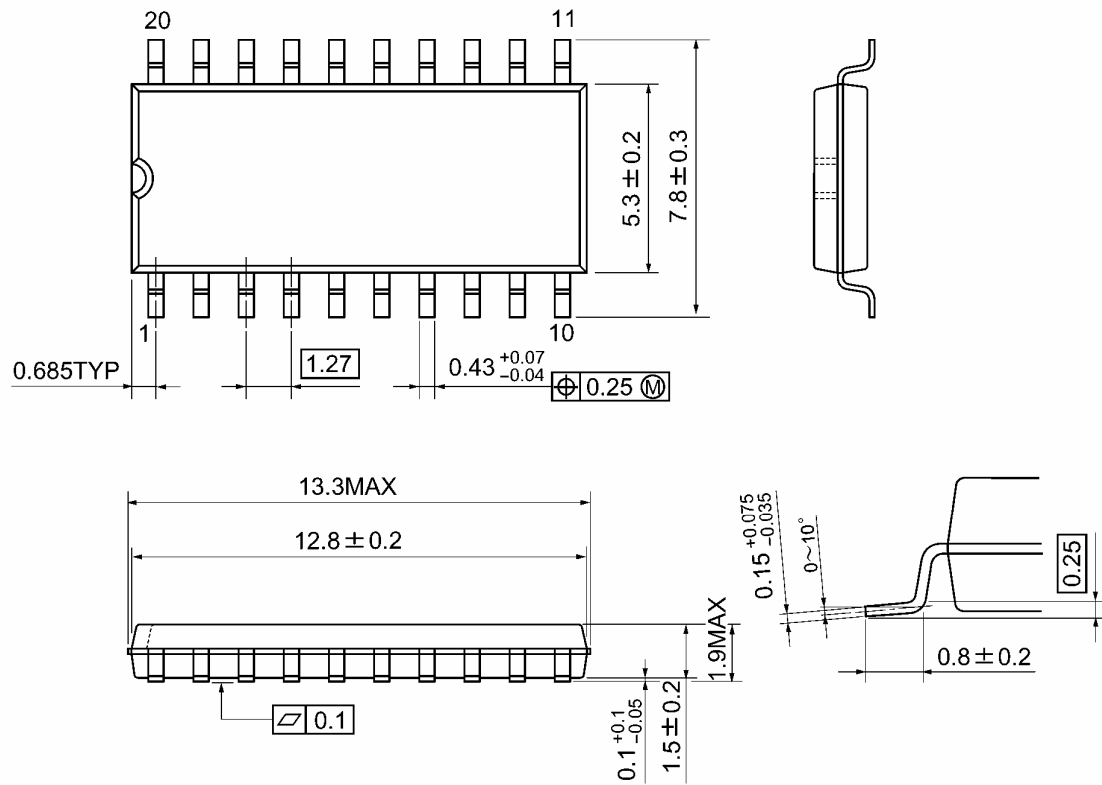
Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V _{CC} (V)	Typ.	Max	
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	1.1 (1.2)	1.5 (1.6)	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-1.1 (-1.2)	-1.5 (-1.6)	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	2.0	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	0.8	V

Note: The value in () only applies to JEDEC SOP (FW) devices.

Package Dimensions

SOP20-P-300-1.27A

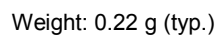
Unit: mm



Weight: 0.22 g (typ.)

SOP20-P-300-1.27

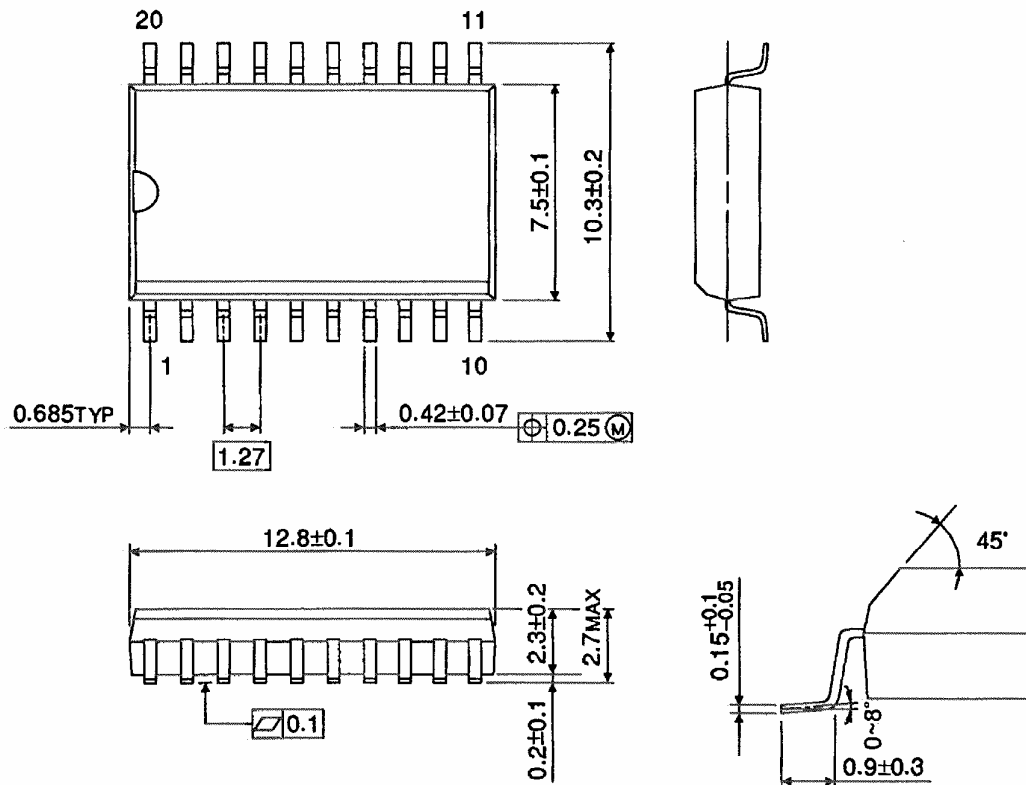
Unit : mm



Package Dimensions (Note)

SOL20-P-300-1.27

Unit : mm



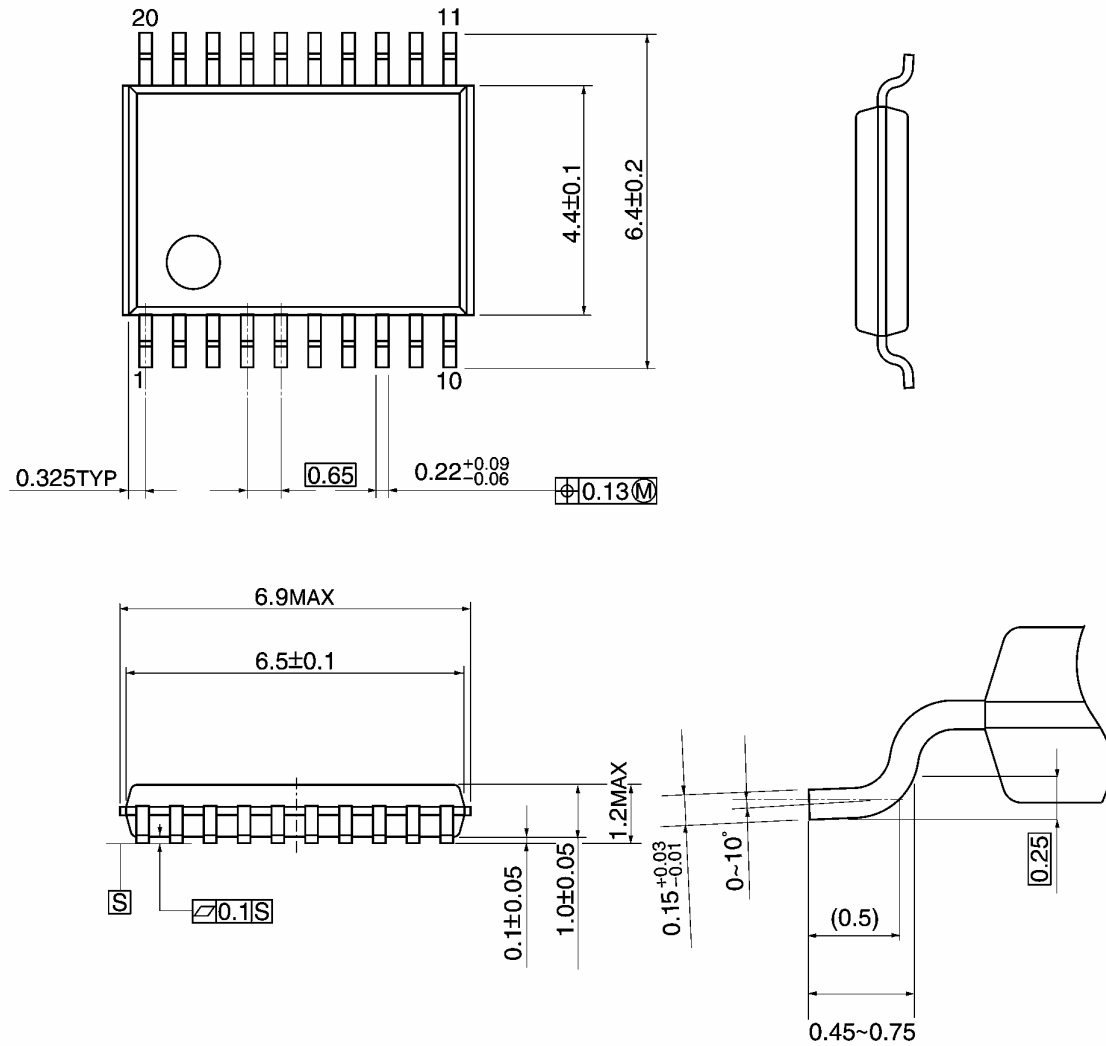
Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

Note: Lead (Pb)-Free Packages

SOP20-P-300-1.27A TSSOP20-P-0044-0.65A

RESTRICTIONS ON PRODUCT USE

060116EBA

- The information contained herein is subject to change without notice. 021023_D
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc. 021023_A
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk. 021023_B
- The products described in this document shall not be used or embedded to any downstream products of which manufacture, use and/or sale are prohibited under any applicable laws and regulations. 060106_Q
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of TOSHIBA or others. 021023_C
- The products described in this document are subject to the foreign exchange and foreign trade laws. 021023_E