

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC540F,TC74VHC540FW,TC74VHC540FT,TC74VHC540FK TC74VHC541F,TC74VHC541FW,TC74VHC541FT,TC74VHC541FK

Octal Bus Buffer

TC74VHC540F/FW/FT/FK

Inverted, 3-State Outputs

TC74VHC541F/FW/FT/FK

Non-Inverted, 3-State Outputs

The TC74VHC540/TC74VHC541 are advanced high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The TC74VHC540 is an inverting type, and the TC74VHC541 is a non-inverting type.

When either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

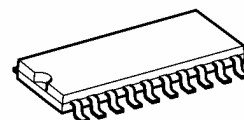
- High speed: $t_{pd} = 3.7$ ns (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2$ V to 5.5 V
- Low noise: $V_{OLP} = 1.2$ V (max)
- Pin and function compatible with 74ALS540/541

Weight

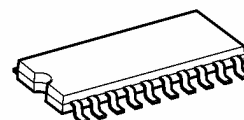
SOP20-P-300-1.27A	: 0.22 g (typ.)
SOP20-P-300-1.27	: 0.22 g (typ.)
SOL20-P-300-1.27	: 0.46 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

Note: xxxFW (JEDEC SOP) is not available in Japan.

TC74VHC540F, TC74VHC541F

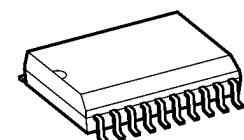


SOP20-P-300-1.27A



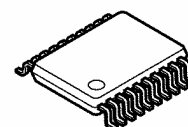
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TC74VHC540FW, TC74VHC541FW



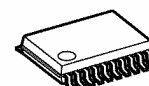
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TC74VHC540FT, TC74VHC541FT



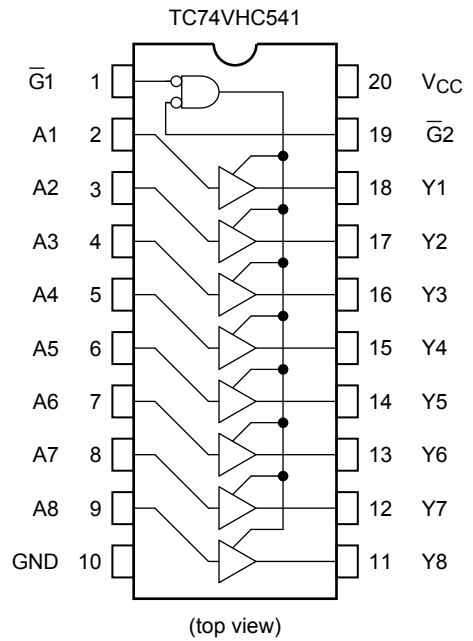
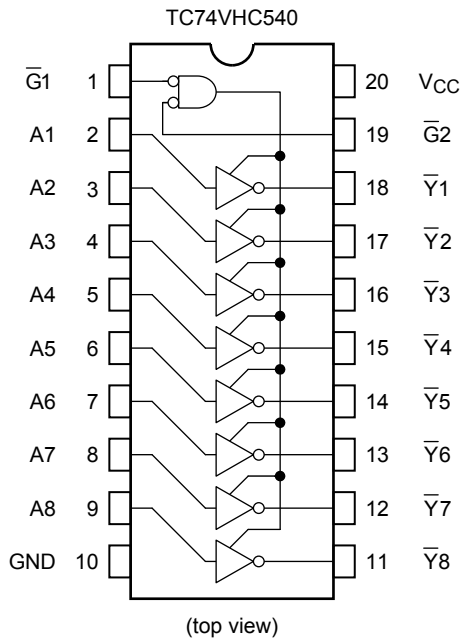
TSSOP20-P-0044-0.65A

TC74VHC540FK, TC74VHC541FK

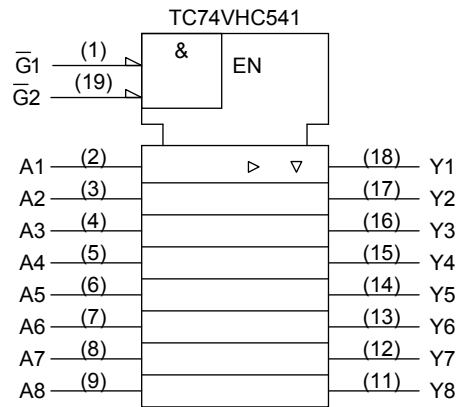
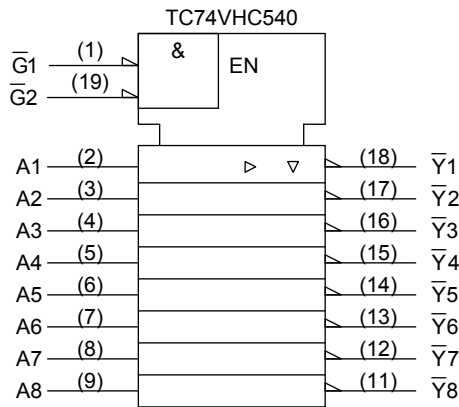


VSSOP20-P-0030-0.50

Pin Assignment



IEC Logic Symbol



Truth Table

Inputs			Outputs	
$\overline{G1}$	$\overline{G2}$	A_n	Y_n	$\overline{Y}_n$
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X: Don't care

Z: High impedance

Y_n : TC74VHC541

$\overline{Y}_n$: TC74VHC540

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low-level input voltage	V _{IL}	—		2.0 3.0 to 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—	
I _{OH} = -8 mA	4.5	3.94	—	—	3.80	—				
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
I _{OL} = 8 mA	4.5	—	—	0.36	—	0.44				
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.50	μA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (TC74VHC540)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	4.8	7.0	1.0	8.5	ns
				50	—	7.3	10.5	1.0	12.0	
			5.0 ± 0.5	15	—	3.7	5.0	1.0	6.0	
				50	—	5.2	7.0	1.0	8.0	
Propagation delay time (TC74VHC541)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	5.0	7.0	1.0	8.5	ns
				50	—	7.5	10.5	1.0	12.0	
			5.0 ± 0.5	15	—	3.5	5.0	1.0	6.0	
				50	—	5.0	7.0	1.0	8.0	
3-state output enable time	t_{pZL} t_{pZH}	R _L = 1 kΩ	3.3 ± 0.3	15	—	6.8	10.5	1.0	12.5	ns
				50	—	9.3	14.0	1.0	16.0	
			5.0 ± 0.5	15	—	4.7	7.2	1.0	8.5	
				50	—	6.2	9.2	1.0	10.5	
3-state output disable time	t_{pLZ} t_{pHZ}	R _L = 1 kΩ	3.3 ± 0.3	50	—	11.2	15.4	1.0	17.5	ns
			5.0 ± 0.5	50	—	6.0	8.8	1.0	10.0	
Output to output skew	t_{osHL} t_{osLH}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C _{IN}	—			—	4	10	—	10	pF
Output capacitance	C _{OUT}	—			—	6	—	—	—	pF
Power dissipation capacitance (Note 2)	C _{PD}	TC74VHC540			—	17	—	—	—	pF
		TC74VHC541			—	18	—	—	—	

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

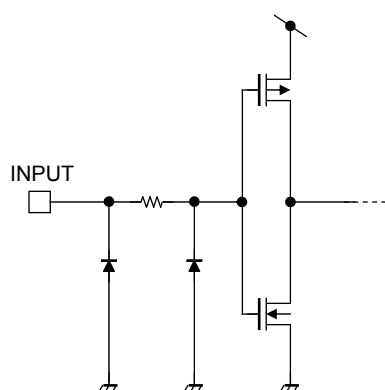
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$) (Note)

Characteristics	Symbol	Test Condition	Ta = 25°C		Unit
			V _{CC} (V)	Typ.	Limit
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.7 (0.9)	1.0 (1.2)
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.7 (-0.9)	-1.0 (-1.2)
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	3.5
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	1.5

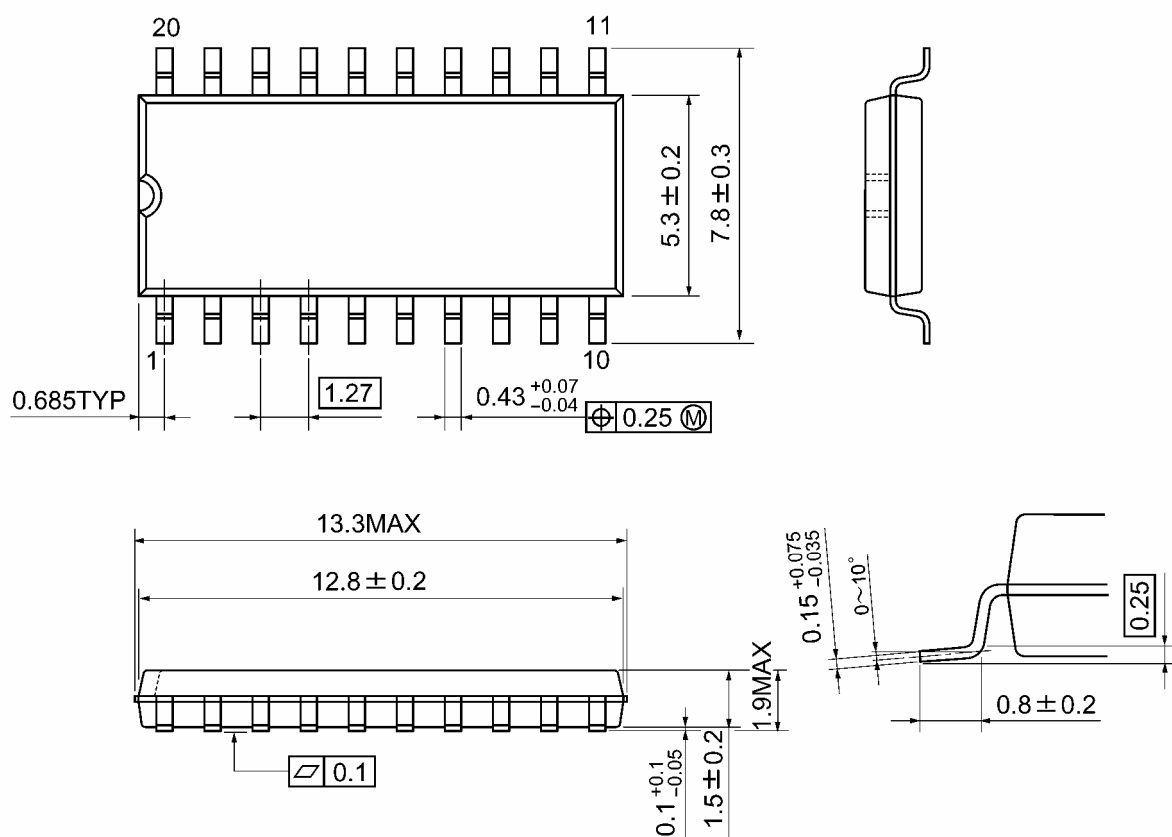
Note: The value in () only applies to JEDEC SOP (FW) devices.

Input Equivalent Circuit

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

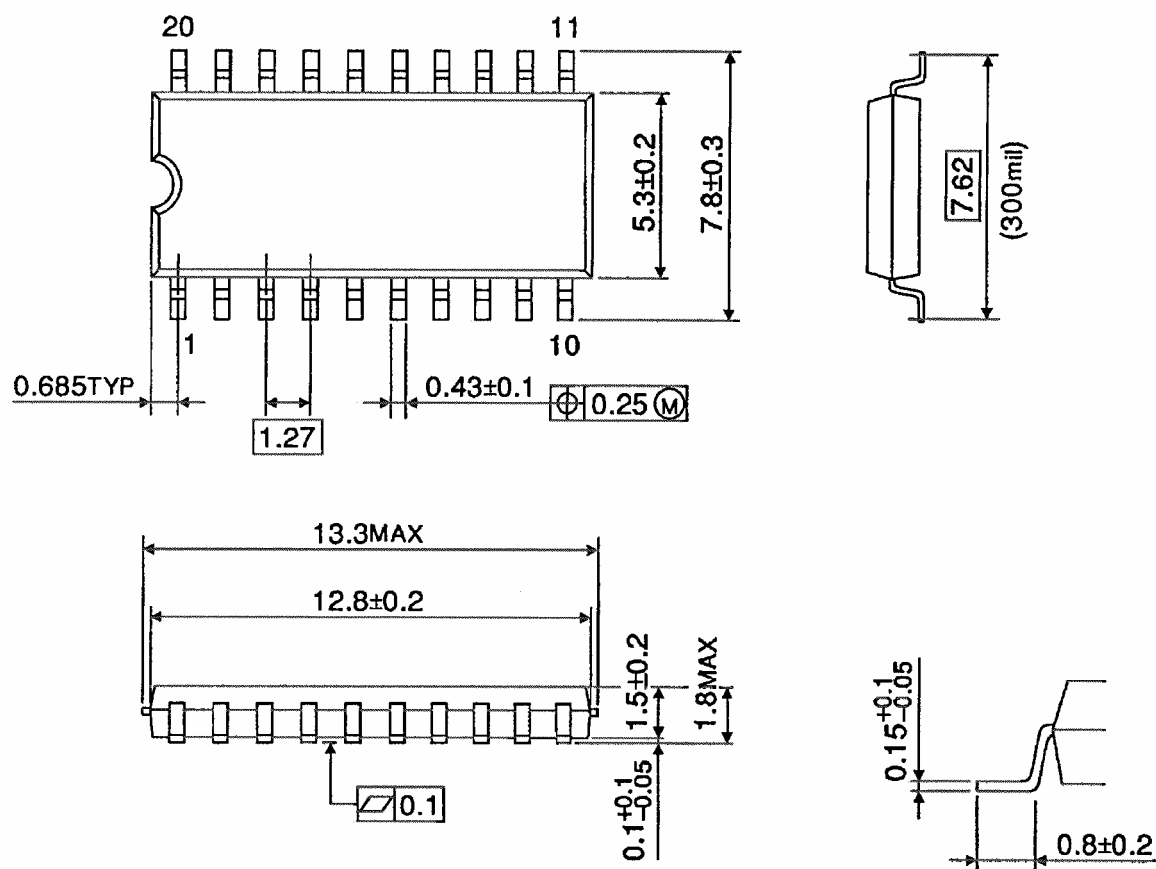


Weight: 0.22 g (typ.)

Package Dimensions

SOP20-P-300-1.27

Unit : mm

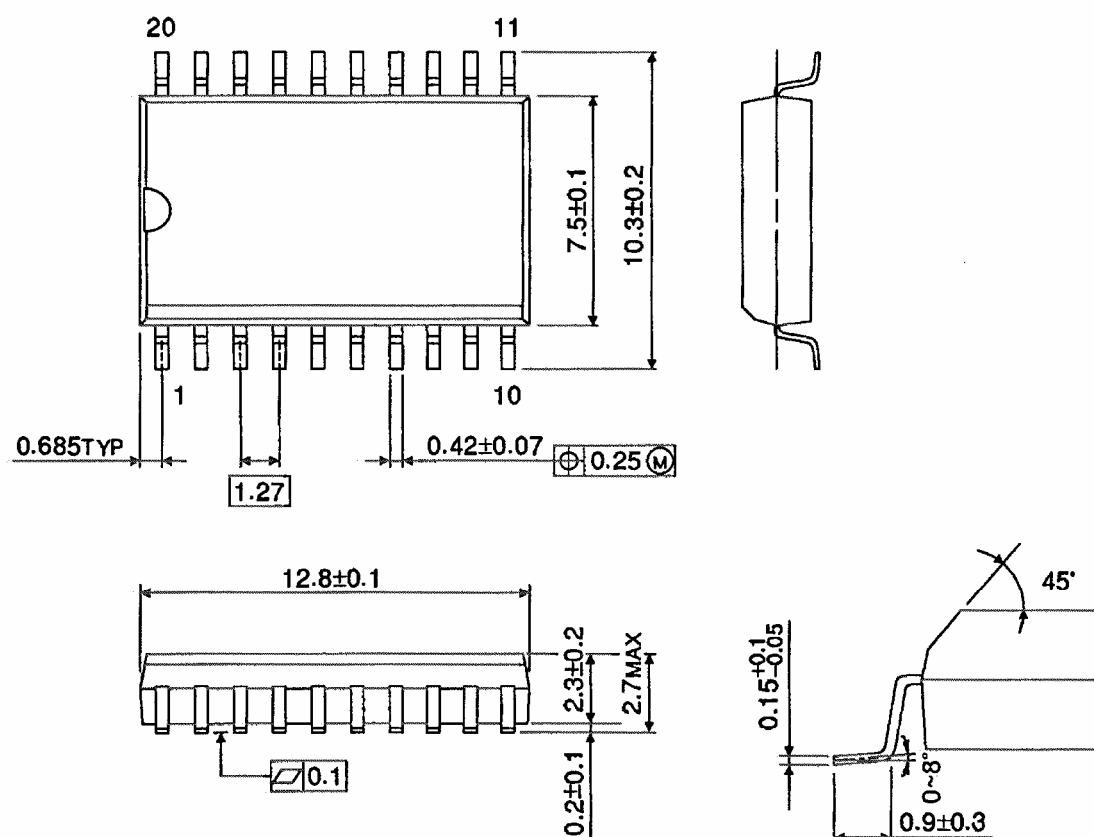


Weight: 0.22 g (typ.)

Package Dimensions (Note)

SOL20-P-300-1.27

Unit : mm



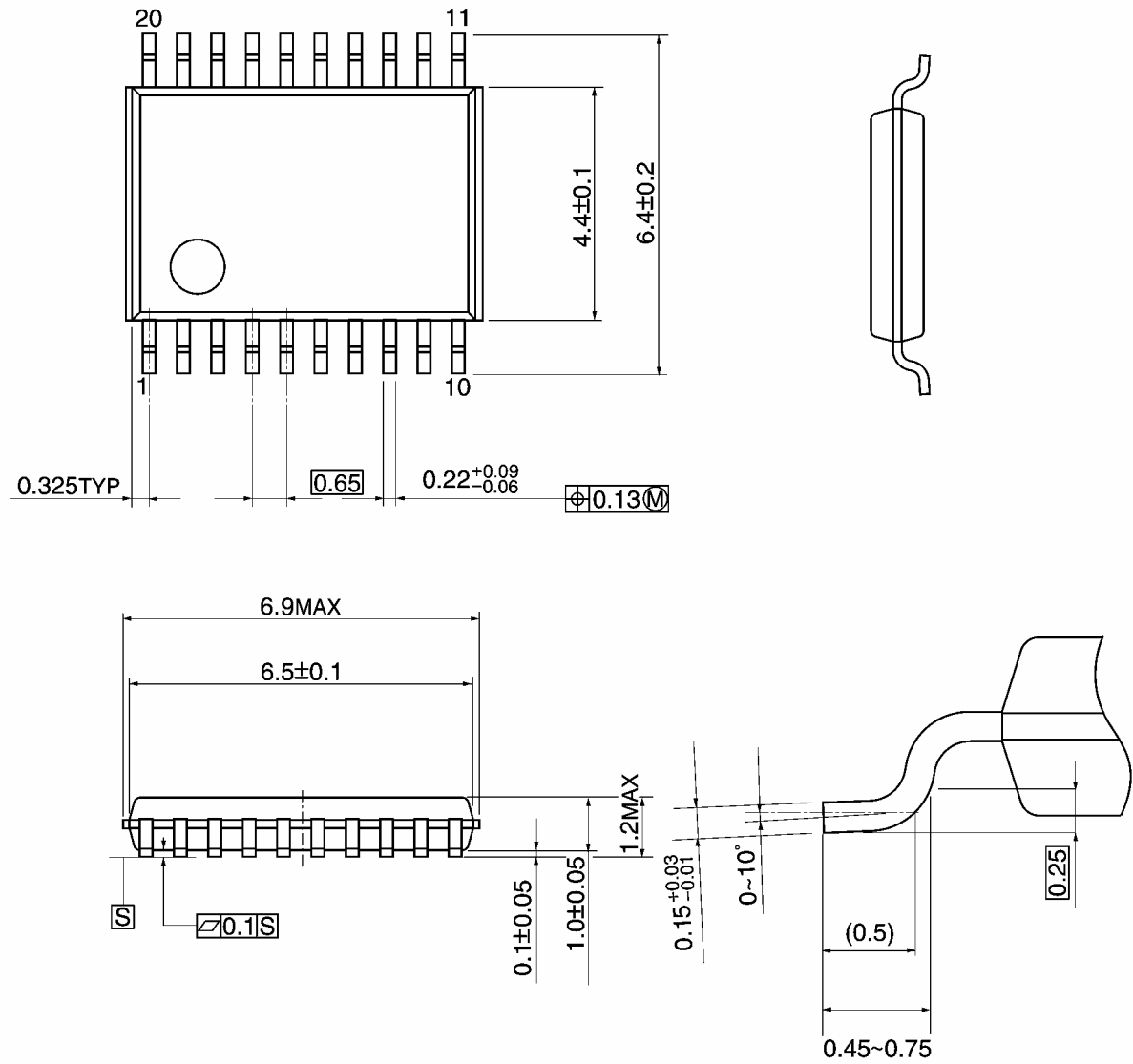
Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm

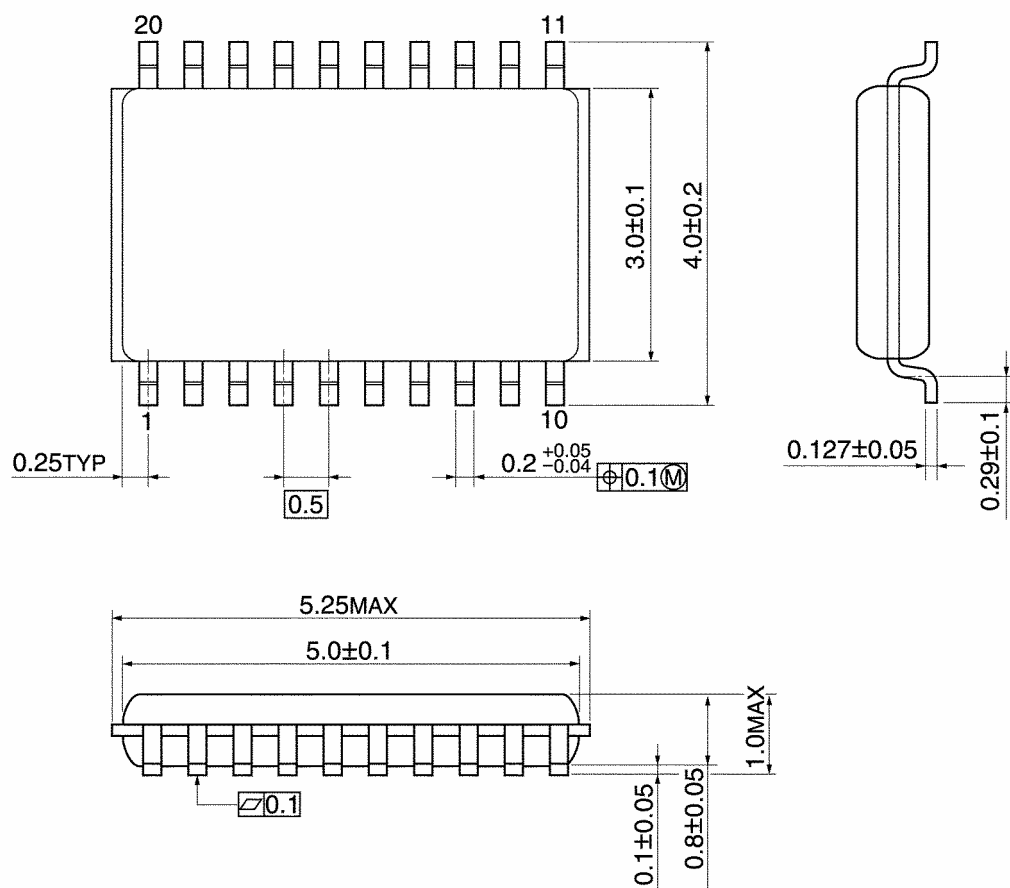


Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

Note: Lead (Pb)-Free Packages**SOP20-P-300-1.27A TSSOP20-P-0044-0.65A VSSOP20-P-0030-0.50****RESTRICTIONS ON PRODUCT USE**

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