

TC74VHC374F, TC74VHC374FW, TC74VHC374FT

Octal D-Type Flip Flop with 3-State Output

The TC74VHC374 is an advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

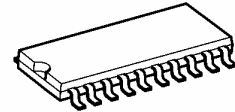
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

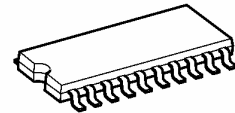
- High speed: $f_{max} = 185 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2 \text{ to } 5.5 \text{ V}$
- Low noise: $V_{OLP} = 0.9 \text{ V}$ (max)
- Pin and function compatible with 74ALS374

Note: xxxFW (JEDEC SOP) is not available in Japan.

TC74VHC374F

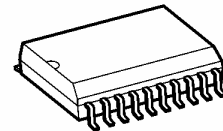


SOP20-P-300-1.27A



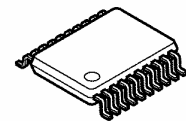
SOP20-P-300-1.27

TC74VHC374FW



SOL20-P-300-1.27

TC74VHC374FT

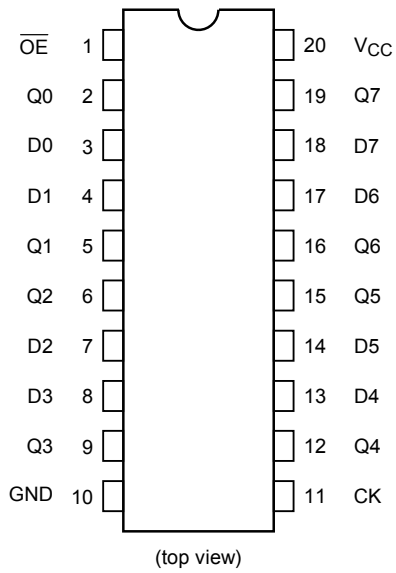


TSSOP20-P-0044-0.65A

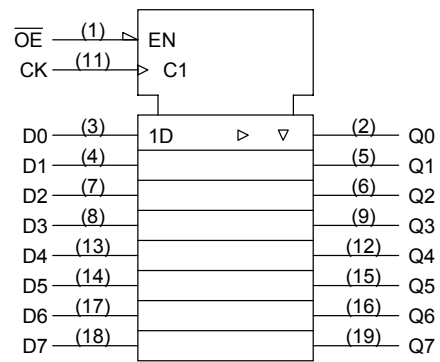
Weight

| | |
|----------------------|-----------------|
| SOP20-P-300-1.27A | : 0.22 g (typ.) |
| SOP20-P-300-1.27 | : 0.22 g (typ.) |
| SOL20-P-300-1.27 | : 0.46 g (typ.) |
| TSSOP20-P-0044-0.65A | : 0.08 g (typ.) |

Pin Assignment



IEC Logic Symbol



Truth Table

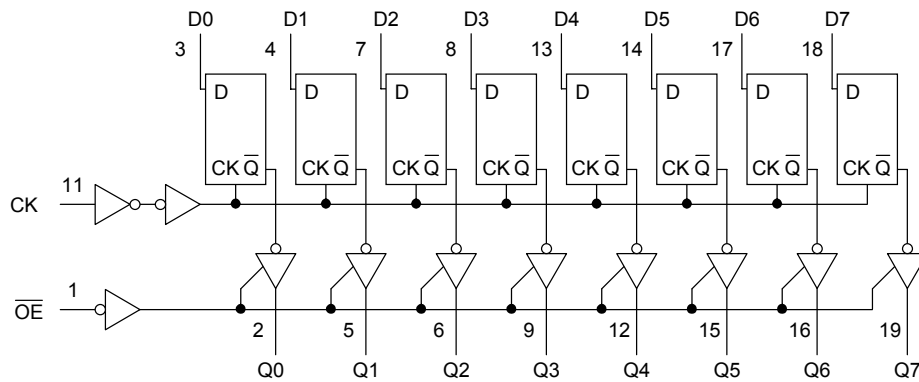
| Inputs | | | Output |
|-----------------|----|---|--------|
| \overline{OE} | CK | D | |
| H | X | X | Z |
| L | | X | Q_n |
| L | | L | L |
| L | | H | H |

X: Don't care

Z: High impedance

Q_n : No change

System Diagram



Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|-----------|------------------------|------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V |
| DC input voltage | V_{IN} | -0.5 to 7.0 | V |
| DC output voltage | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| Input diode current | I_{IK} | -20 | mA |
| Output diode current | I_{OK} | ± 20 | mA |
| DC output current | I_{OUT} | ± 25 | mA |
| DC V_{CC} /ground current | I_{CC} | ± 75 | mA |
| Power dissipation | P_D | 180 | mW |
| Storage temperature | T_{stg} | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (Note)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|---|------|
| Supply voltage | V_{CC} | 2.0 to 5.5 | V |
| Input voltage | V_{IN} | 0 to 5.5 | V |
| Output voltage | V_{OUT} | 0 to V_{CC} | V |
| Operating temperature | T_{opr} | -40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V) | ns/V |

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics
DC Characteristics

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | | | Ta = -40 to 85°C | | Unit |
|----------------------------------|-----------------|---|--|---------------------|-------------------------------|--------|-------------------------------|-------------------------------|-------------------------------|------|
| | | | | V _{CC} (V) | Min | Typ. | Max | Min | Max | |
| High-level input voltage | V _{IH} | — | | 2.0 3.0 to 5.5 | 1.50 V _{CC} × 0.7 | — — | — — | 1.50 V _{CC} × 0.7 | — — | V |
| Low-level input voltage | V _{IL} | — | | 2.0 3.0 to 5.5 | — — | — — | 0.50 V _{CC} × 0.3 | — — | 0.50 V _{CC} × 0.3 | V |
| High-level output voltage | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | | 4.5 | 3.94 | — | — | 3.80 | — | |
| Low-level output voltage | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | | 4.5 | — | — | 0.36 | — | 0.44 | |
| 3-state output off-state current | I _{OZ} | V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | | 5.5 | — | — | ±0.25 | — | ±2.50 | μA |
| Input leakage current | I _{IN} | V _{IN} = 5.5 V or GND | | 0 to 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | I _{CC} | V _{IN} = V _{CC} or GND | | 5.5 | — | — | 4.0 | — | 40.0 | μA |

Timing Requirements (input: t_r = t_f = 3 ns)

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | Ta = -40 to 85°C | Unit |
|-----------------------------|--------------------|----------------|-----------|-----------|------|------------------------|------|
| | | | | VCC (V) | Typ. | Limit | |
| Minimum pulse width (CK) | t _w (H) | — | 3.3 ± 0.3 | — | 5.0 | 5.5 | ns |
| | t _w (L) | | 5.0 ± 0.5 | — | 5.0 | 5.0 | |
| Minimum set-up time | t _s | — | 3.3 ± 0.3 | — | 4.5 | 4.5 | ns |
| | | | 5.0 ± 0.5 | — | 3.0 | 3.0 | |
| Minimum hold time | t _h | — | 3.3 ± 0.3 | — | 2.0 | 2.0 | ns |
| | | | 5.0 ± 0.5 | — | 2.0 | 2.0 | |

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | | | Ta = 25°C | | | Ta = -40 to 85°C | | Unit |
|----------------------------------|--|-----------------------|---------------------|---------------------|-----------|------|------|---------------------|------|------|
| | | | V _{CC} (V) | C _L (pF) | Min | Typ. | Max | Min | Max | |
| Propagation delay time (CK-Q) | t _{pLH} t _{pHL} | — | 3.3 ± 0.3 | 15 | — | 8.1 | 12.7 | 1.0 | 15.0 | ns |
| | | | | 50 | — | 10.6 | 16.2 | 1.0 | 18.5 | |
| | | | 5.0 ± 0.5 | 15 | — | 5.4 | 8.1 | 1.0 | 9.5 | |
| | | | | 50 | — | 6.9 | 10.1 | 1.0 | 11.5 | |
| 3-state output enable time | t _{pZL} t _{pZH} | R _L = 1 kΩ | 3.3 ± 0.3 | 15 | — | 7.1 | 11.0 | 1.0 | 13.0 | ns |
| | | | | 50 | — | 9.6 | 14.5 | 1.0 | 16.5 | |
| | | | 5.0 ± 0.5 | 15 | — | 5.1 | 7.6 | 1.0 | 9.0 | |
| | | | | 50 | — | 6.6 | 9.6 | 1.0 | 11.0 | |
| 3-state output disable time | t _{pLZ} t _{pHZ} | R _L = 1 kΩ | 3.3 ± 0.3 | 50 | — | 10.2 | 14.0 | 1.0 | 16.0 | ns |
| | | | 5.0 ± 0.5 | 50 | — | 6.1 | 8.8 | 1.0 | 10.0 | |
| Maximum clock frequency | f _{max} | — | 3.3 ± 0.3 | 15 | 80 | 130 | — | 70 | — | MHz |
| | | | | 50 | 55 | 85 | — | 50 | — | |
| | | | 5.0 ± 0.5 | 15 | 130 | 185 | — | 110 | — | |
| | | | | 50 | 85 | 120 | — | 75 | — | |
| Output to output skew | t _{osLH} t _{osHL} | (Note 1) | 3.3 ± 0.3 | 50 | — | — | 1.5 | — | 1.5 | ns |
| | | | 5.0 ± 0.5 | 50 | — | — | 1.0 | — | 1.0 | |
| Input capacitance | C _{IN} | — | | | — | 4 | 10 | — | 10 | pF |
| Output capacitance | C _{OUT} | — | | | — | 6 | — | — | — | pF |
| Power dissipation capacitance | C _{PD} | (Note 2) | | | — | 32 | — | — | — | pF |

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:

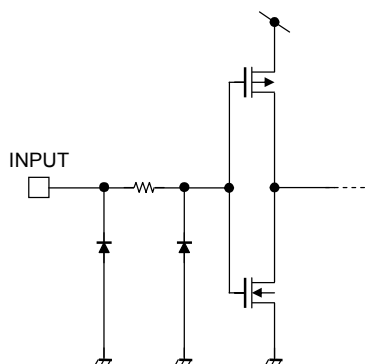
$$C_{PD(\text{total})} = 20 + 12 \cdot n$$

Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$) (Note)

| Characteristics | Symbol | Test Condition | $V_{CC} \text{ (V)}$ | $T_a = 25^\circ\text{C}$ | | Unit |
|--|-----------|-----------------------|----------------------|--------------------------|----------------|------|
| | | | | Typ. | Max | |
| Quiet output maximum dynamic V_{OL} | V_{OLP} | $C_L = 50 \text{ pF}$ | 5.0 | 0.5 (0.6) | 0.8 (0.9) | V |
| Quiet output minimum dynamic V_{OL} | V_{OLV} | $C_L = 50 \text{ pF}$ | 5.0 | -0.5 (-0.6) | -0.8 (-0.9) | V |
| Minimum high level dynamic input voltage | V_{IHD} | $C_L = 50 \text{ pF}$ | 5.0 | — | 3.5 | V |
| Maximum low level dynamic input voltage | V_{ILD} | $C_L = 50 \text{ pF}$ | 5.0 | — | 1.5 | V |

Note: The value in () only applies to JEDEC SOP (FW) devices.

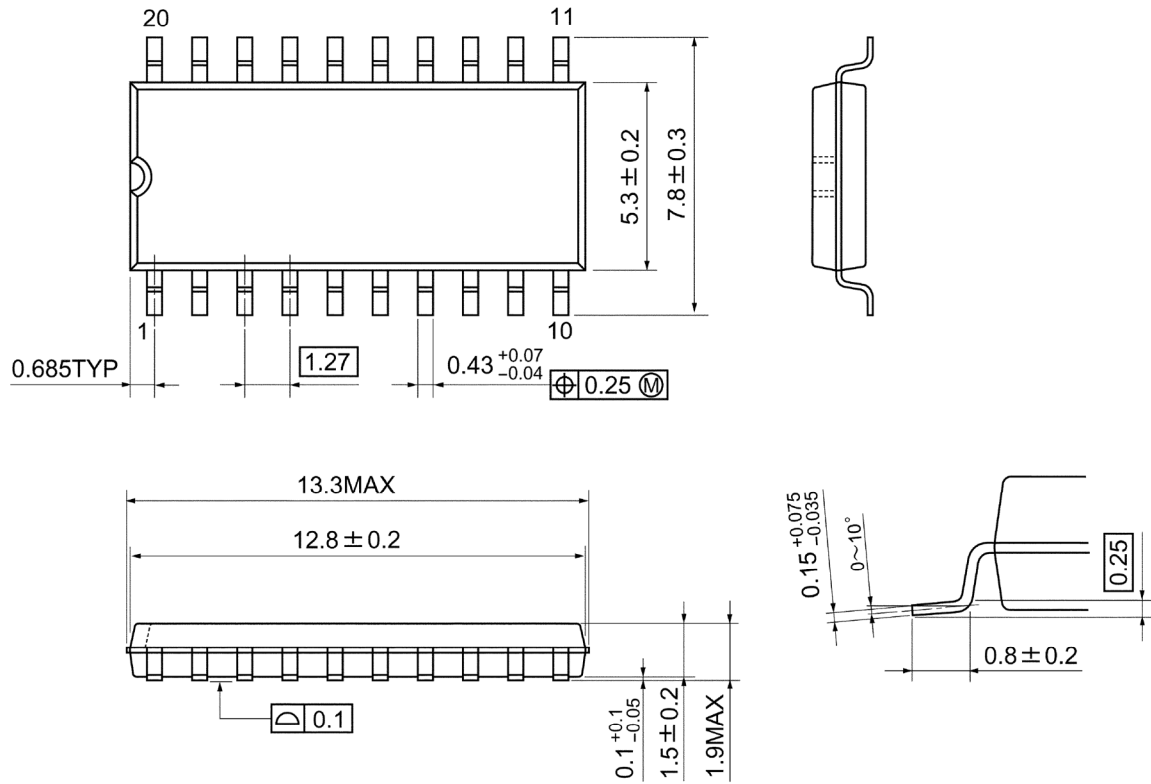
Input Equivalent Circuit



Package Dimensions

SOP20-P-300-1.27A

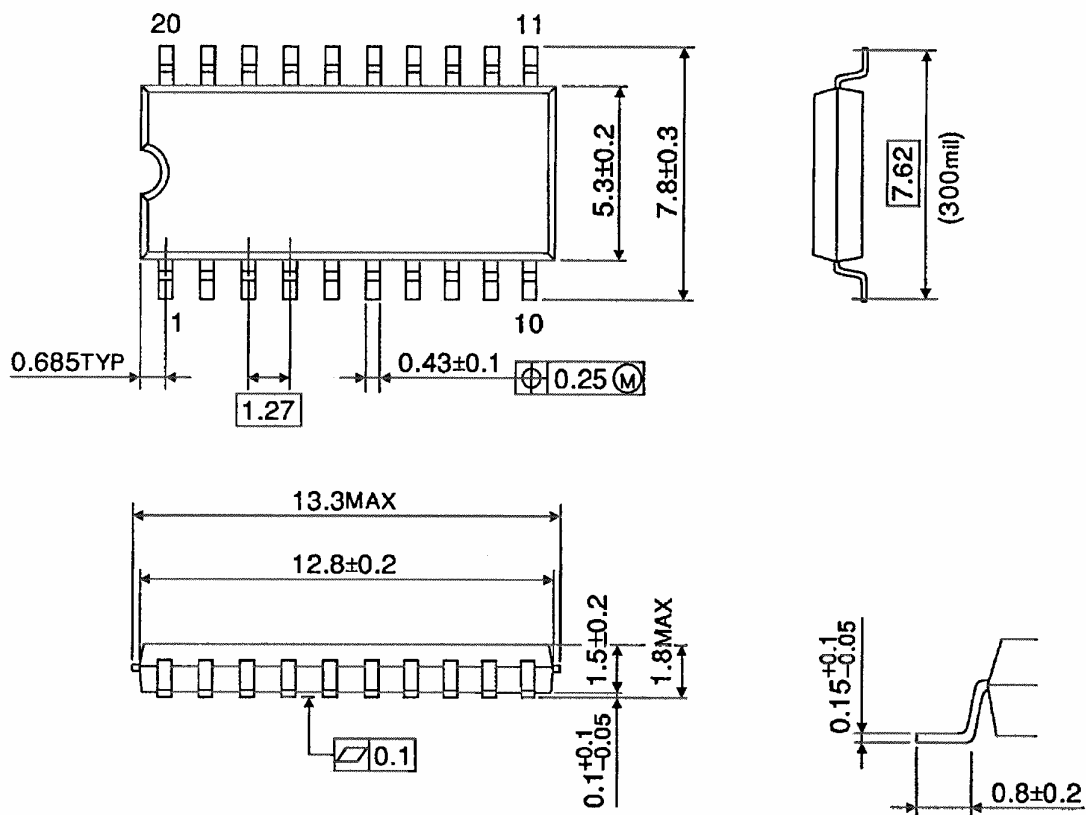
Unit: mm



Weight: 0.22 g (typ.)

SOP20-P-300-1.27

Unit : mm

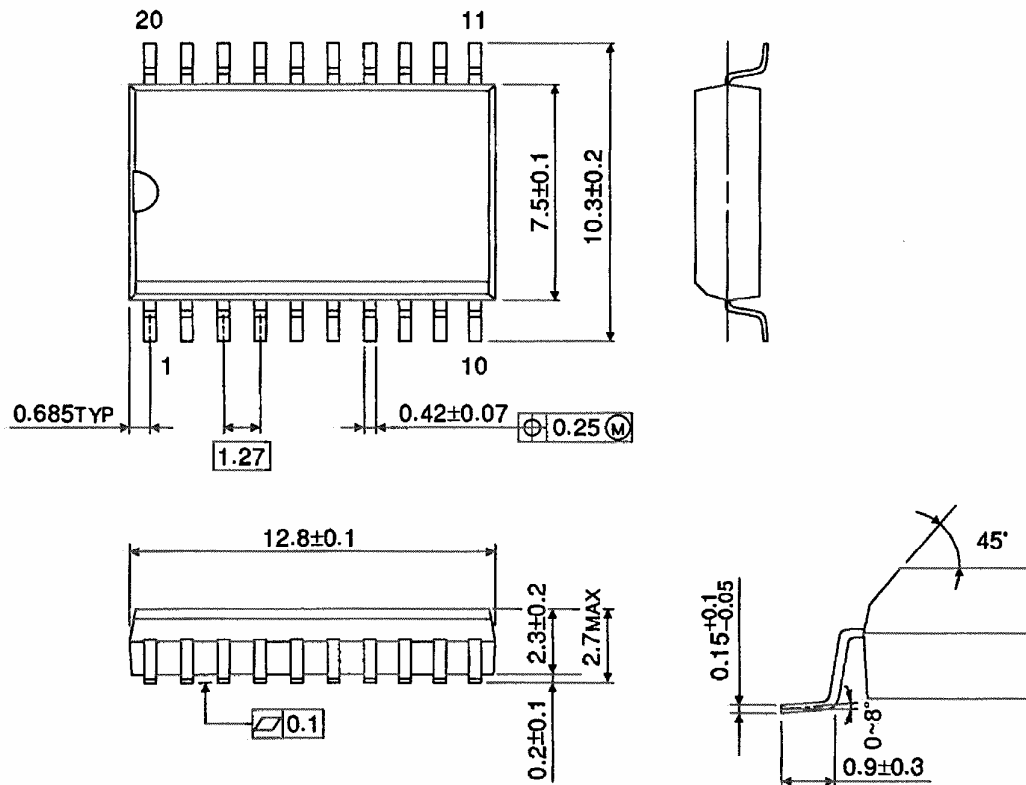


Weight: 0.22 g (typ.)

Package Dimensions (Note)

SOL20-P-300-1.27

Unit : mm



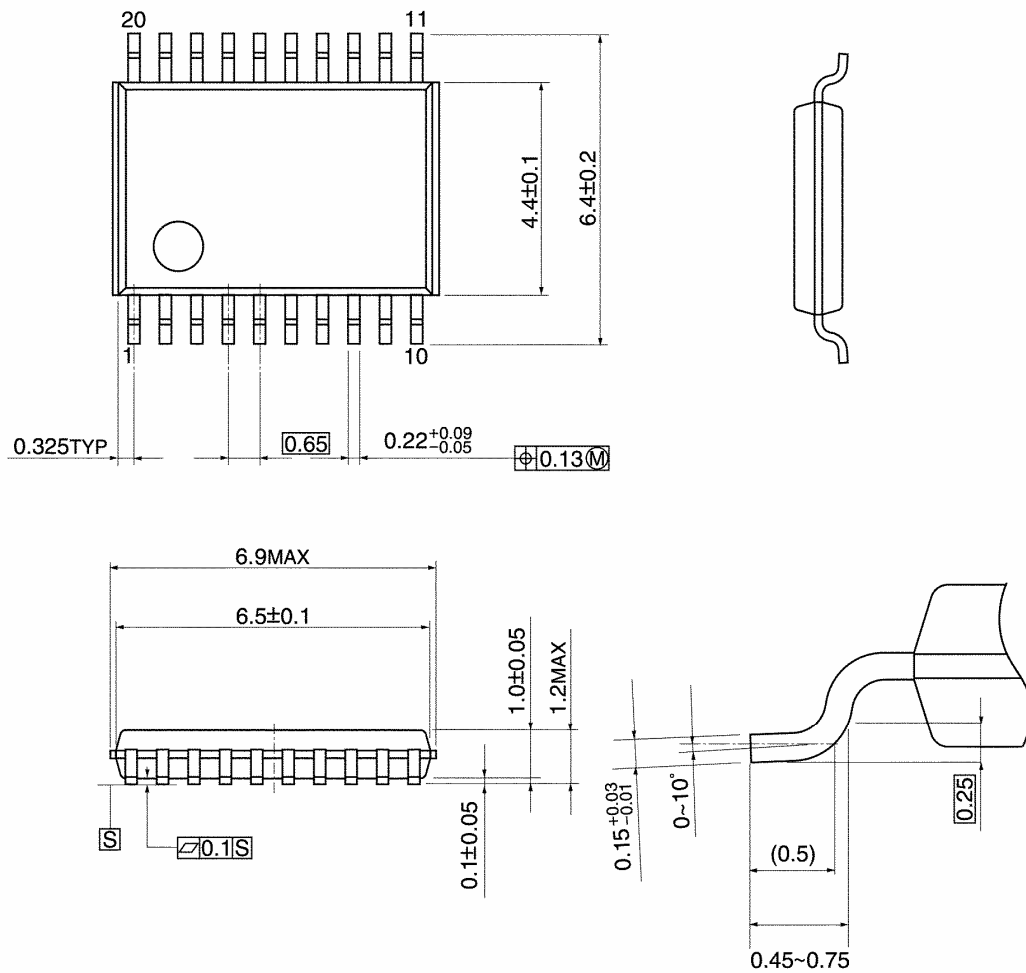
Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

Note: Lead (Pb)-Free Packages

SOP20-P-300-1.27A TSSOP20-P-0044-0.65A

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