CMOS Digital Integrated Circuits Silicon Monolithic

TC74VCX163245

1. Functional Description

- 16-Bit Dual Supply Bus Transceiver

2. General

The TC74VCX163245 is a dual supply, advanced high-speed CMOS 16-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Designed for use as an interface between a 1.8 V or 2.5 V bus and a 2.5 V or 3.6 V bus in mixed 1.8 V or 2.5 V/2.5 V or 3.6 V supply systems.

The B-port interfaces with the 1.8 V or 2.5 V bus, the A-port with the 2.5 V or 3.6 V bus.

The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features (Note)

(1) Wide operating temperature range: T_{opr} = -40 to 125 °C (Note 1)

(2) Operating voltage: 1.8 V-2.5 V / 1.8 V-3.6 V / 2.5 V-3.6 V bidirectional interface

(3) High-speed operation: t_{pd} = 7.0 ns (max) (V_{CCB} = 1.8±0.15 V, V_{CCA} = 2.5±0.2 V)
t_{pd} = 7.1 ns (max) (V_{CCB} = 1.8±0.15 V, V_{CCA} = 3.3±0.3 V)
t_{pd} = 4.6 ns (max) (V_{CCB} = 2.5±0.2 V, V_{CCA} = 3.3±0.3 V)

(4) Output current: I_{OH}/I_{OL} = ±24 mA (min) (V_{CC} = 3.0 V)
I_{OH}/I_{OL} = ±18 mA (min) (V_{CC} = 2.3 V)
I_{OH}/I_{OL} = ±6 mA (min) (V_{CC} = 1.65 V)

(5) Latch-up performance: -300 mA

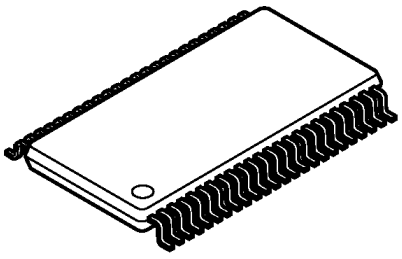
(6) ESD performance: Human Body Model ≥ ±2000 V

(7) 3.6 V tolerant function and power-down protection provided on all inputs and outputs.

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input levels fixed by means of pull-up or pull-down resistors.

Note 1: Operating Range spec of T_{opr} = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

4. Packaging

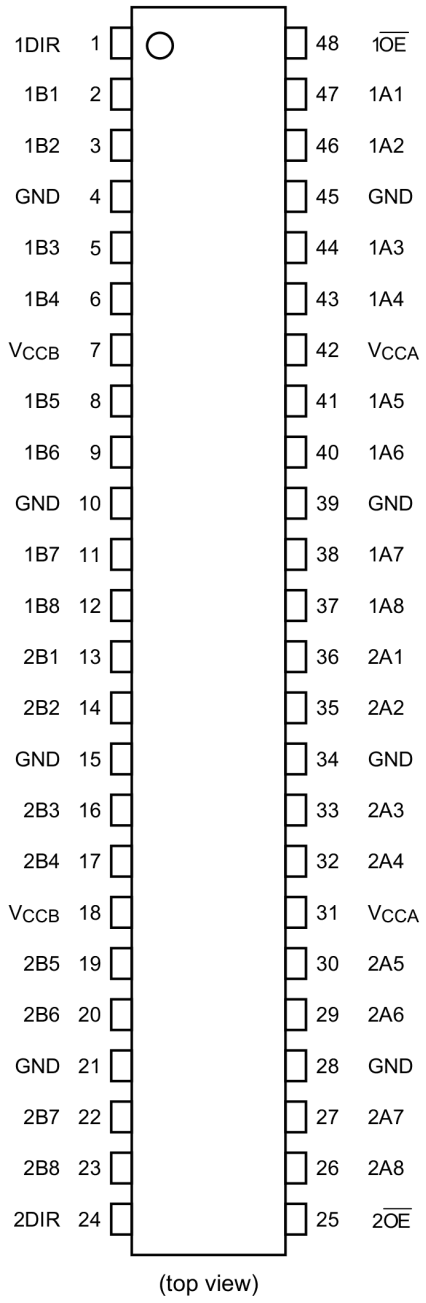


TSSOP48

Start of commercial production
2020-04

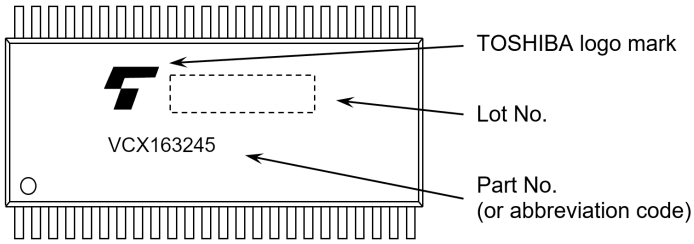
2020-09-15
Rev.1.0

5. Pin Assignment

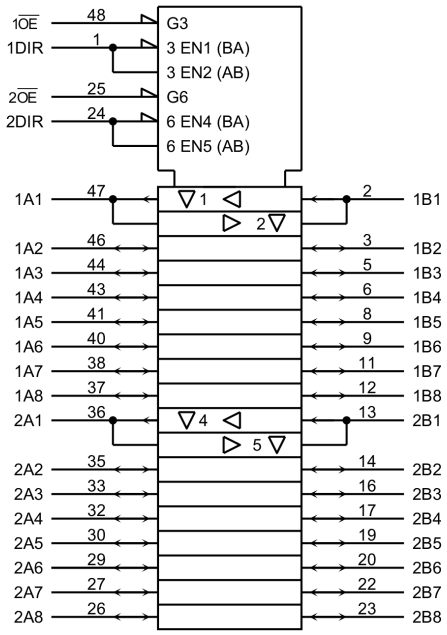


(top view)

6. Marking



7. IEC Logic Symbol

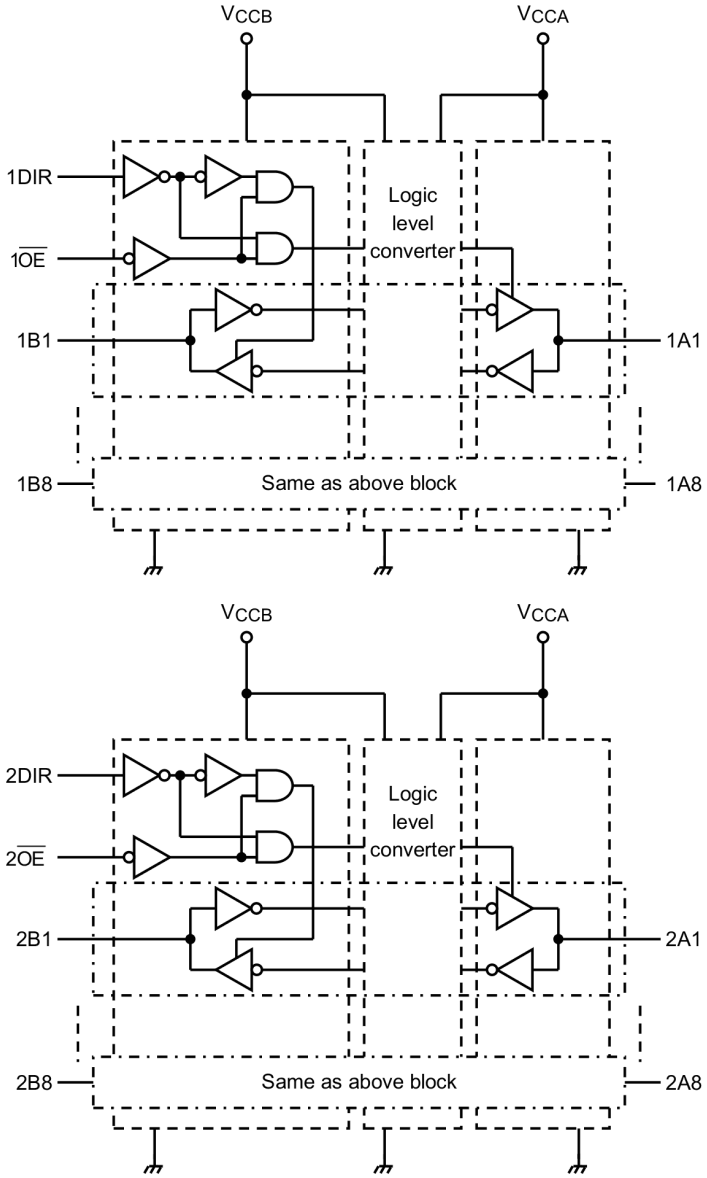


8. Truth Table

Inputs 1$\overline{OE}$ 2$\overline{OE}$	Inputs 1DIR 2DIR	Outputs	Function Bus 1A1-1A8 Bus 2A1-2A8	Function Bus 1B1-1B8 Bus 2B1-2B8
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	Z	Z

X: Don't care
Z: High impedance

9. System Diagram



10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCB}	(Note 1)	-0.5 to 4.6	V
	V_{CCA}		-0.5 to 4.6	
Input voltage (DIR/$\overline{OE}$)	V_{IN}		-0.5 to 4.6	V
Bus I/O voltage	$V_{I/OB}$	(Note 2)	-0.5 to 4.6	V
		(Note 3)	-0.5 to V_{CCB} + 0.5	
	$V_{I/OA}$	(Note 2)	-0.5 to 4.6	
		(Note 3)	-0.5 to V_{CCA} + 0.5	
Input diode current	I_{IK}		-50	mA
I/O diode current	$I_{I/OK}$	(Note 4)	±50	mA
Output current	I_{OUTB}		±50	mA
	I_{OUTA}		±50	
Power dissipation	P_D	(Note 5)	400	mW
V_{CC}/ground current per supply pin	I_{CCB}		±100	mA
	I_{CCA}		±100	
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Don't supply a voltage to V_{CCA} terminal when V_{CCB} is in the off-state.

Note 2: Output in OFF state.

Note 3: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Note 5: 400 mW in the range of Ta = -40 to 85 °C. From Ta = 85 to 125 °C a derating factor of -6.25 mW/°C shall be applied until 150 mW.

11. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCB}	(Note 1)	1.65 to 2.7	V
	V_{CCA}		2.3 to 3.6	
Input voltage (DIR/$\overline{OE}$)	V_{IN}		0 to 3.6	V
Bus I/O voltage	$V_{I/OB}$	(Note 2)	0 to 3.6	V
		(Note 3)	0 to V_{CCB}	
	$V_{I/OA}$	(Note 2)	0 to 3.6	
		(Note 3)	0 to V_{CCA}	
Output current	I_{OUTB}	(Note 4)	±18	mA
		(Note 5)	±6	
	I_{OUTA}	(Note 6)	±24	
		(Note 7)	±18	
Operating temperature	T_{opr}	(Note 8)	-40 to 125	°C
Input rise and fall times	dt/dv	(Note 9)	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 1: Don't use in $V_{CCB} > V_{CCA}$

Note 2: Output in OFF state.

Note 3: High (H) or Low (L) state.

Note 4: V_{CCB} = 2.3 to 2.7 V

Note 5: V_{CCB} = 1.65 to 1.95 V

Note 6: V_{CCA} = 3.0 to 3.6 V

Note 7: V_{CCA} = 2.3 to 2.7 V

Note 8: Operating Range spec of T_{opr} = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

Note 9: V_{INB} = 0.7 to 1.6 V , V_{CCB} = 2.5 V
V_{INA} = 0.8 to 2.0 V , V_{CCA} = 3.0 V

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Min	Max	Unit
High-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		1.65 to 1.95	2.3 to 3.6	V_{CCB} × 0.65	—	V
				2.3 to 2.7	3.0 to 3.6	1.6	—	
	V_{IHA}	An		1.65 to 1.95	2.3 to 2.7	1.6	—	V
				1.65 to 2.7	3.0 to 3.6	2.0	—	
Low-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		1.65 to 1.95	2.3 to 3.6	—	V_{CCB} × 0.35	V
				2.3 to 2.7	3.0 to 3.6	—	0.7	
	V_{ILA}	An		1.65 to 1.95	2.3 to 2.7	—	0.7	V
				1.65 to 2.7	3.0 to 3.6	—	0.8	
High-level output voltage	V_{OHB}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100 μA	1.65 to 1.95	2.3 to 3.6	V_{CCB} - 0.2	—	V
				2.3 to 2.7	3.0 to 3.6	V_{CCB} - 0.2	—	
			I_{OH} = -6 mA	1.65	2.3 to 3.6	1.25	—	
			I_{OH} = -18 mA	2.3	3.0 to 3.6	1.7	—	
	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100 μA	1.65 to 1.95	2.3 to 3.6	V_{CCA} - 0.2	—	
				2.3 to 2.7	3.0 to 3.6	V_{CCA} - 0.2	—	
			I_{OH} = -18 mA	1.65 to 1.95	2.3	1.7	—	
			I_{OH} = -24 mA	1.65 to 2.7	3.0	2.2	—	
Low-level output voltage	V_{OLB}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.65 to 1.95	2.3 to 3.6	—	0.2	V
				2.3 to 2.7	3.0 to 3.6	—	0.2	
			I_{OL} = 6 mA	1.65	2.3 to 3.6	—	0.3	
			I_{OL} = 18 mA	2.3	3.0 to 3.6	—	0.6	
	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.65 to 1.95	2.3 to 3.6	—	0.2	
				2.3 to 2.7	3.0 to 3.6	—	0.2	
			I_{OL} = 18 mA	1.65 to 1.95	2.3	—	0.6	
			I_{OL} = 24 mA	1.65 to 2.7	3.0	—	0.55	
Input leakage current	I_{IN}	V_{IN} = 0 to 3.6 V		1.65 to 1.95	2.3 to 3.6	—	±5.0	μA
				2.3 to 2.7	3.0 to 3.6	—	±5.0	
3-state output OFF-state leakage current	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 1.95	2.3 to 3.6	—	±10.0	μA
				2.3 to 2.7	3.0 to 3.6	—	±10.0	
	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 1.95	2.3 to 3.6	—	±10.0	μA
				2.3 to 2.7	3.0 to 3.6	—	±10.0	
Power-OFF leakage current	I_{OFF}	V_{IN}/V_{OUT} = 0 to 3.6 V		0	0	—	10.0	μA
Quiescent supply current	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 1.95	2.3 to 3.6	—	20.0	μA
				2.3 to 2.7	3.0 to 3.6	—	20.0	
		$V_{CCB} \leq (V_{IN}/V_{OUT}) \leq 3.6$ V		1.65 to 1.95	2.3 to 3.6	—	±20.0	
				2.3 to 2.7	3.0 to 3.6	—	±20.0	
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 1.95	2.3 to 3.6	—	20.0	
				2.3 to 2.7	3.0 to 3.6	—	20.0	
		$V_{CCA} \leq (V_{IN}/V_{OUT}) \leq 3.6$ V		1.65 to 1.95	2.3 to 3.6	—	±20.0	
				2.3 to 2.7	3.0 to 3.6	—	±20.0	
	I_{CCTB}	V_{IHB} = V_{CCB} - 0.6 V (per input)		1.65 to 1.95	2.3 to 3.6	—	750	μA
				2.3 to 2.7	3.0 to 3.6	—	750	
	I_{CCTA}	V_{IHA} = V_{CCA} - 0.6 V (per input)		1.65 to 1.95	2.3 to 3.6	—	750	
				2.3 to 2.7	3.0 to 3.6	—	750	

12.2. DC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Min	Max	Unit
High-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		1.65 to 1.95	2.3 to 3.6	V_{CCB} × 0.65	—	V
				2.3 to 2.7	3.0 to 3.6	1.6	—	
	V_{IHA}	An		1.65 to 1.95	2.3 to 2.7	1.6	—	V
				1.65 to 2.7	3.0 to 3.6	2.0	—	
Low-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		1.65 to 1.95	2.3 to 3.6	—	V_{CCB} × 0.35	V
				2.3 to 2.7	3.0 to 3.6	—	0.7	
	V_{ILA}	An		1.65 to 1.95	2.3 to 2.7	—	0.7	V
				1.65 to 2.7	3.0 to 3.6	—	0.8	
High-level output voltage	V_{OHB}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100 μA	1.65 to 1.95	2.3 to 3.6	V_{CCB} - 0.2	—	V
				2.3 to 2.7	3.0 to 3.6	V_{CCB} - 0.2	—	
			I_{OH} = -6 mA	1.65	2.3 to 3.6	1.25	—	
			I_{OH} = -18 mA	2.3	3.0 to 3.6	1.6	—	
	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100 μA	1.65 to 1.95	2.3 to 3.6	V_{CCA} - 0.2	—	
				2.3 to 2.7	3.0 to 3.6	V_{CCA} - 0.2	—	
			I_{OH} = -18 mA	1.65 to 1.95	2.3	1.6	—	
			I_{OH} = -24 mA	1.65 to 2.7	3.0	2.2	—	
Low-level output voltage	V_{OLB}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.65 to 1.95	2.3 to 3.6	—	0.2	V
				2.3 to 2.7	3.0 to 3.6	—	0.2	
			I_{OL} = 6 mA	1.65	2.3 to 3.6	—	0.3	
			I_{OL} = 18 mA	2.3	3.0 to 3.6	—	0.8	
	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.65 to 1.95	2.3 to 3.6	—	0.2	
				2.3 to 2.7	3.0 to 3.6	—	0.2	
			I_{OL} = 18 mA	1.65 to 1.95	2.3	—	0.8	
			I_{OL} = 24 mA	1.65 to 2.7	3.0	—	0.55	
Input leakage current	I_{IN}	V_{IN} = 0 to 3.6 V		1.65 to 1.95	2.3 to 3.6	—	±20.0	μA
				2.3 to 2.7	3.0 to 3.6	—	±20.0	
3-state output OFF-state leakage current	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 1.95	2.3 to 3.6	—	±40.0	μA
				2.3 to 2.7	3.0 to 3.6	—	±40.0	
	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		1.65 to 1.95	2.3 to 3.6	—	±40.0	μA
				2.3 to 2.7	3.0 to 3.6	—	±40.0	
Power-OFF leakage current	I_{OFF}	V_{IN}/V_{OUT} = 0 to 3.6 V		0	0	—	40.0	μA
Quiescent supply current	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 1.95	2.3 to 3.6	—	80.0	μA
				2.3 to 2.7	3.0 to 3.6	—	80.0	
		$V_{CCB} \leq (V_{IN}/V_{OUT}) \leq 3.6$ V		1.65 to 1.95	2.3 to 3.6	—	±80.0	
				2.3 to 2.7	3.0 to 3.6	—	±80.0	
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		1.65 to 1.95	2.3 to 3.6	—	80.0	
				2.3 to 2.7	3.0 to 3.6	—	80.0	
		$V_{CCA} \leq (V_{IN}/V_{OUT}) \leq 3.6$ V		1.65 to 1.95	2.3 to 3.6	—	±80.0	
				2.3 to 2.7	3.0 to 3.6	—	±80.0	
	I_{CCTB}	V_{IHB} = V_{CCB} - 0.6 V (per input)		1.65 to 1.95	2.3 to 3.6	—	1.5	mA
				2.3 to 2.7	3.0 to 3.6	—	1.5	
	I_{CCTA}	V_{IHA} = V_{CCA} - 0.6 V (per input)		1.65 to 1.95	2.3 to 3.6	—	1.5	
				2.3 to 2.7	3.0 to 3.6	—	1.5	

Note: Operating Range spec of T_{opr} = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

12.3. AC Characteristics (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Note	Test Condition	V_{CCB} (V)	V_{CCA} (V)	Min	Max	Unit
Propagation delay time (Bn→An)	t_{PLH},t_{PHL}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.1, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	5.8	ns
				1.8 ± 0.15	3.3 ± 0.3	0.6	5.5	
				2.5 ± 0.2	3.3 ± 0.3	0.6	4.4	
Propagation delay time (An→Bn)	t_{PLH},t_{PHL}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.1, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	1.5	7.0	ns
				1.8 ± 0.15	3.3 ± 0.3	1.5	7.1	
				2.5 ± 0.2	3.3 ± 0.3	0.8	4.6	
3-state output enable time ($\overline{OE}$→An)	t_{PZL},t_{PZH}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	6.9	ns
				1.8 ± 0.15	3.3 ± 0.3	0.6	6.9	
				2.5 ± 0.2	3.3 ± 0.3	0.6	4.8	
3-state output enable time ($\overline{OE}$→Bn)	t_{PZL},t_{PZH}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	1.5	11.0	ns
				1.8 ± 0.15	3.3 ± 0.3	1.5	10.3	
				2.5 ± 0.2	3.3 ± 0.3	0.8	6.2	
3-state output disable time ($\overline{OE}$→An)	t_{PLZ},t_{PHZ}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	6.4	ns
				1.8 ± 0.15	3.3 ± 0.3	0.6	7.1	
				2.5 ± 0.2	3.3 ± 0.3	0.6	4.9	
3-state output disable time ($\overline{OE}$→Bn)	t_{PLZ},t_{PHZ}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	7.0	ns
				1.8 ± 0.15	3.3 ± 0.3	0.8	7.1	
				2.5 ± 0.2	3.3 ± 0.3	0.8	4.9	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	1.8 ± 0.15	2.5 ± 0.2	—	0.5	ns
				1.8 ± 0.15	3.3 ± 0.3	—	0.5	
				2.5 ± 0.2	3.3 ± 0.3	—	0.5	

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m-t_{PLH}n|$, t_{osHL} = $|t_{PHL}m-t_{PHL}n|$)

12.4. AC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Note	Test Condition	V_{CCB} (V)	V_{CCA} (V)	Min	Max	Unit
Propagation delay time (Bn→An)	t_{PLH},t_{PHL}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.1, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	7.3	ns
				1.8 ± 0.15	3.3 ± 0.3	0.6	6.9	
				2.5 ± 0.2	3.3 ± 0.3	0.6	5.5	
Propagation delay time (An→Bn)	t_{PLH},t_{PHL}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.1, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	1.5	8.8	ns
				1.8 ± 0.15	3.3 ± 0.3	1.5	8.9	
				2.5 ± 0.2	3.3 ± 0.3	0.8	5.8	
3-state output enable time ($\overline{OE}$→An)	t_{PZL},t_{PZH}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	8.7	ns
				1.8 ± 0.15	3.3 ± 0.3	0.6	8.7	
				2.5 ± 0.2	3.3 ± 0.3	0.6	6.0	
3-state output enable time ($\overline{OE}$→Bn)	t_{PZL},t_{PZH}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	1.5	13.8	ns
				1.8 ± 0.15	3.3 ± 0.3	1.5	12.9	
				2.5 ± 0.2	3.3 ± 0.3	0.8	7.8	
3-state output disable time ($\overline{OE}$→An)	t_{PLZ},t_{PHZ}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	8.0	ns
				1.8 ± 0.15	3.3 ± 0.3	0.6	8.9	
				2.5 ± 0.2	3.3 ± 0.3	0.6	6.2	
3-state output disable time ($\overline{OE}$→Bn)	t_{PLZ},t_{PHZ}		See 12.7 AC Test Circuit, Table 12.7.1, Fig. 12.8.2, Table 12.8.1	1.8 ± 0.15	2.5 ± 0.2	0.8	8.8	ns
				1.8 ± 0.15	3.3 ± 0.3	0.8	8.9	
				2.5 ± 0.2	3.3 ± 0.3	0.8	6.2	
Output skew	t_{osLH},t_{osHL}	(Note 1)	—	1.8 ± 0.15	2.5 ± 0.2	—	1.0	ns
				1.8 ± 0.15	3.3 ± 0.3	—	1.0	
				2.5 ± 0.2	3.3 ± 0.3	—	1.0	

Note: Operating Range spec of T_{opr} = -40 °C to 125 °C is applicable only for the products which manufactured after April 2020.

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

12.5. Dynamic Switching Characteristics (Note) (Unless otherwise specified, T_a = 25°C, Input: $t_r = t_f$ = 2.0 ns, C_L = 30 pF)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	V_{CCA} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL} (B→A)	V_{OLP}	$V_{IH} = V_{CC}$, V_{IL} = 0 V	1.8	2.5	0.25	V
			1.8	3.3	0.25	
			2.5	3.3	0.6	
Quiet output maximum dynamic V_{OL} (A→B)			1.8	2.5	0.6	V
			1.8	3.3	0.8	
			2.5	3.3	0.8	
Quiet output minimum dynamic V_{OL} (B→A)	V_{OLV}	$V_{IH} = V_{CC}$, V_{IL} = 0 V	1.8	2.5	-0.25	V
			1.8	3.3	-0.25	
			2.5	3.3	-0.6	
Quiet output minimum dynamic V_{OL} (A→B)			1.8	2.5	-0.6	V
			1.8	3.3	-0.8	
			2.5	3.3	-0.8	
Quiet output minimum dynamic V_{OH} (B→A)	V_{OHV}	$V_{IH} = V_{CC}$, V_{IL} = 0 V	1.8	2.5	1.3	V
			1.8	3.3	1.3	
			2.5	3.3	1.7	
Quiet output minimum dynamic V_{OH} (A→B)			1.8	2.5	1.7	V
			1.8	3.3	2.0	
			2.5	3.3	2.0	

Note: Parameter guaranteed by design.

12.6. Capacitive Characteristics (Unless otherwise specified, T_a = 25°C)

Characteristics	Symbol	Note	Test Condition	V_{CCB} (V)	V_{CCA} (V)	Typ.	Unit
Input capacitance	C_{IN}		DIR, $\overline{OE}$	2.5	3.3	7	pF
Bus I/O capacitance	$C_{I/O}$		An, Bn	2.5	3.3	8	pF
Power dissipation capacitance	C_{PDA}	(Note 1)	A→B (DIR = H)	2.5	3.3	2	pF
			B→A (DIR = L)	2.5	3.3	23	
	C_{PDB}		A→B (DIR = H)	2.5	3.3	26	
			B→A (DIR = L)	2.5	3.3	2	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per bit)

12.7. AC Test Circuit

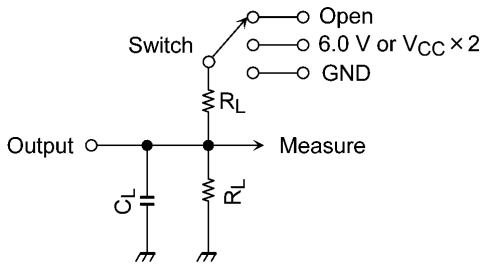


Table 12.7.1 Parameter for AC Test Circuit

Parameter	Switch	Test Condition
t_{PLH}, t_{PHL}	OPEN	—
t_{PLZ}, t_{PZL}	6.0 V	V_{CC} = 3.3 ± 0.3 V
	V_{CC} × 2	V_{CC} = 2.5 ± 0.2 V
		V_{CC} = 1.8 ± 0.15 V
t_{PHZ}, t_{PZH}	GND	—

12.8. AC Waveform

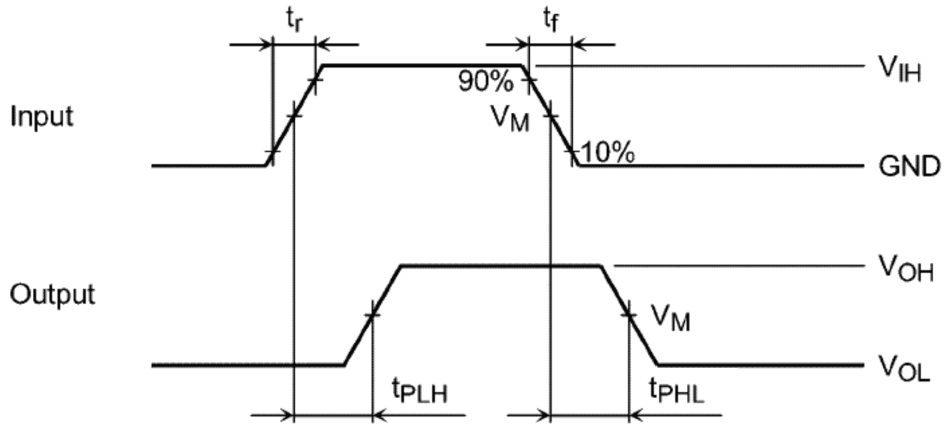


Fig. 12.8.1 t_{PLH}, t_{PHL}

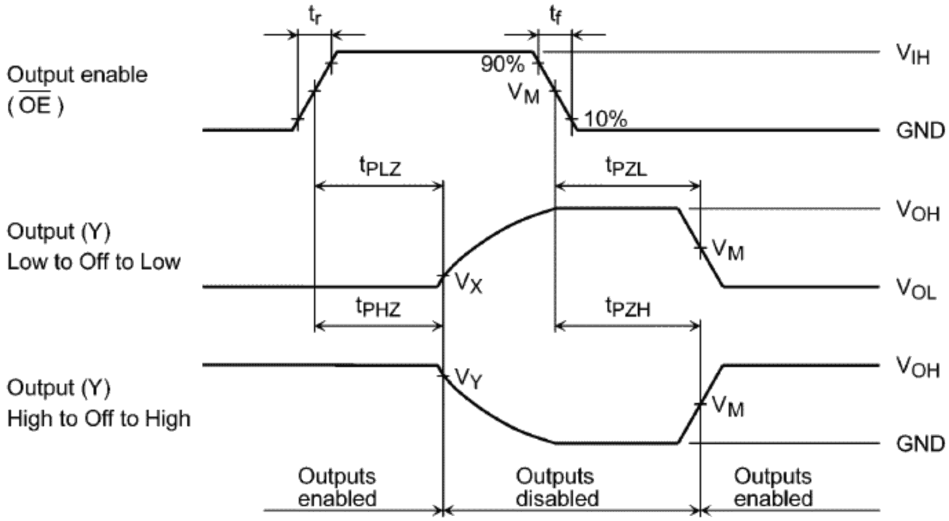


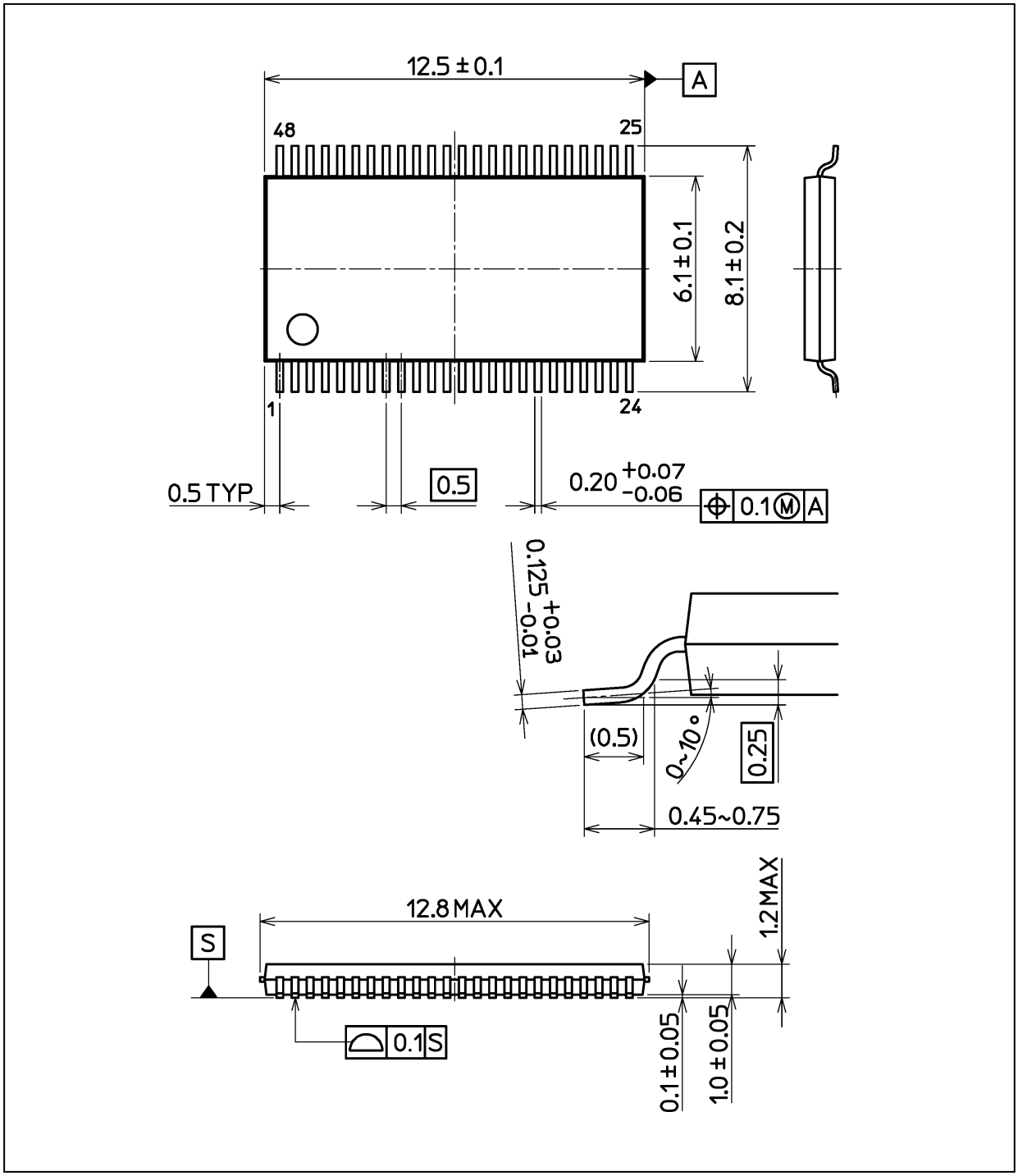
Fig. 12.8.2 t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

Table 12.8.1 AC Waveform Symbols

	Symbol	V_{CC} = 3.3 ± 0.3 V	V_{CC} = 2.5 ± 0.2 V	V_{CC} = 1.8 ± 0.15 V
Input	V_{IH}	2.7 V	V_{CC}	V_{CC}
	V_M	1.5 V	V_{CC}/2	V_{CC}/2
	t_r, t_f	2.0 ns	2.0 ns	2.0 ns
Output	V_M	1.5 V	V_{CC}/2	V_{CC}/2
	V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
	V_Y	V_{OH} - 0.3 V	V_{OH} - 0.15 V	V_{OH} - 0.15 V
Load	C_L	30 pF	30 pF	30 pF
	R_L	500 Ω	500 Ω	500 Ω

Package Dimensions

Unit: mm



Weight: 0.25 g (typ.)

Package Name(s)
Nickname: TSSOP48

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