

TC74HC280P 9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

The TC74HC280 is a high speed CMOS 9-BIT PARITY GENERATOR fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It is composed of nine data inputs (A thru I) and odd/even parity outputs (Σ ODD and Σ EVEN).

The nine input data control the output conditions.

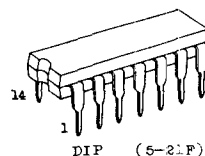
When the number of high level inputs is odd, Σ ODD output is kept high and Σ EVEN output low. On the contrary, when the number is even, Σ EVEN output is kept high and Σ ODD low. This IC facilitates operation of either odd or even parity application.

The word-length capability is easily expanded by cascading.

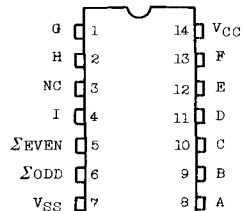
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $t_{pd}=33ns$ (Typ.) at $V_{CC}=5V$
- Low Power Dissipation..... $I_{CC}=4\mu A$ (Max.) at $T_a=25^\circ C$
- High Noise Immunity..... $V_{NIH}=V_{NIL}=28\% V_{CC}$ (Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}|=I_{OL}=4mA$ (Min.)
- Balanced Propagation Delays... $t_{PLH}=t_{PHL}$
- Wide Operating Voltage Range... $V_{CC}(opr)=2V \sim 6V$
- Pin and Function Compatible with 74LS280



PIN ASSIGNMENT



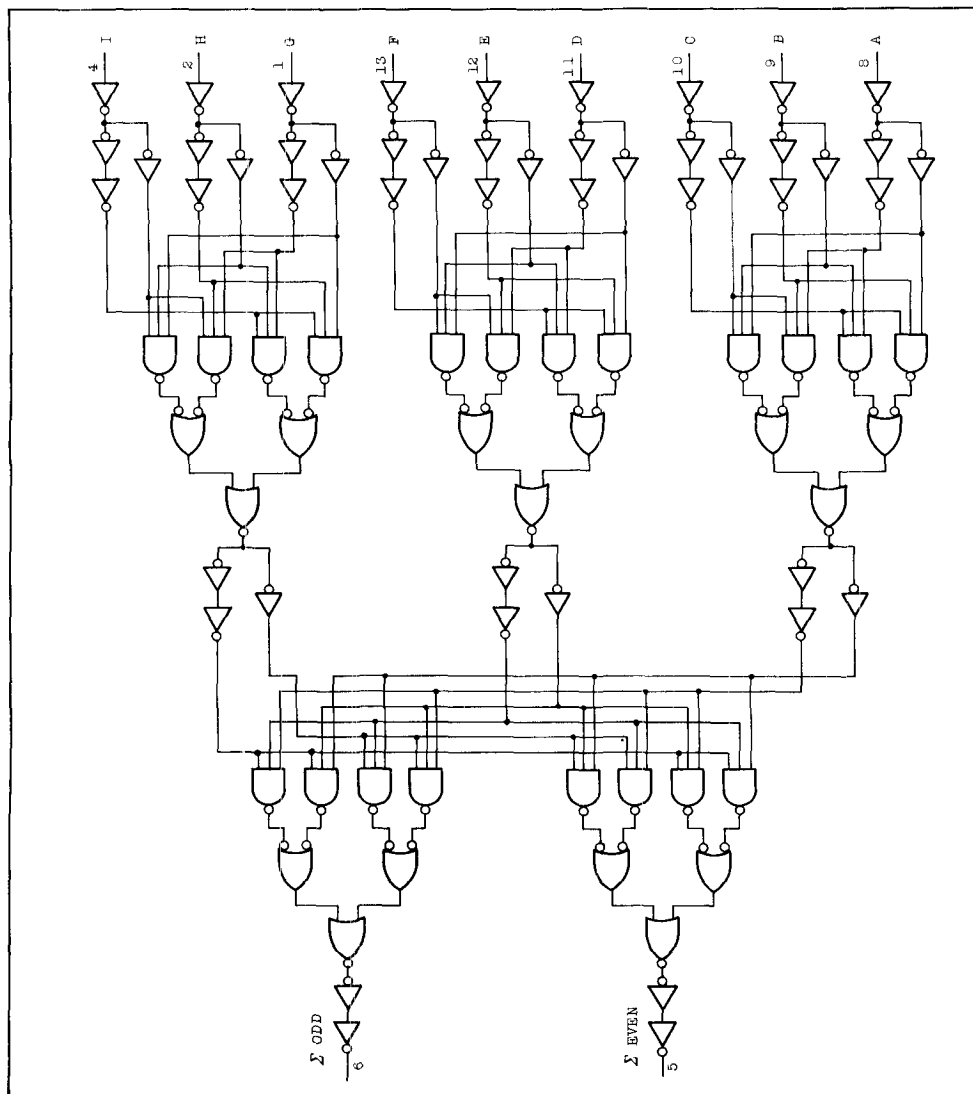
(Top View)

NC : No Connection

TRUTH TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

LOGIC DIAGRAM



TC74HC280P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 ($V_{CC}=2.0V$)	ns
		0 ~ 500 ($V_{CC}=4.5V$)	
		0 ~ 400 ($V_{CC}=6.0V$)	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$T_a=25^{\circ}C$				$T_a=-40\sim85^{\circ}C$		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	V
				4.5	4.4	4.5	-	4.4	
				6.0	5.9	6.0	-	5.9	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	
				6.0	5.68	5.80	-	5.63	
				6.0	-	-	-	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	V
				4.5	-	0.0	0.1	-	
				6.0	-	0.0	0.1	-	
			$I_{OL}=4mA$	4.5	-	0.17	0.32	-	
				6.0	-	0.18	0.32	-	
				6.0	-	-	-	-	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	± 0.1	-	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6\text{ns}$)

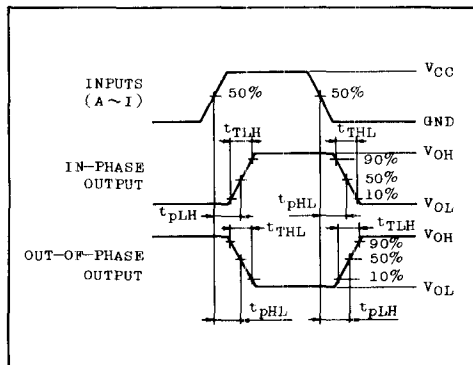
PARAMETER	SYMBOL	TEST CONDITION	$T_a=25^\circ\text{C}$				$T_a=-40\sim85^\circ\text{C}$		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	90	ns
			4.5	-	8	15	-	18	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{PLH} t_{PHL}		2.0	-	150	295	-	355	ns
			4.5	-	39	59	-	71	
			6.0	-	34	51	-	62	
Input Capacitance	C_{IN}		-	-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$		-	-	110	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

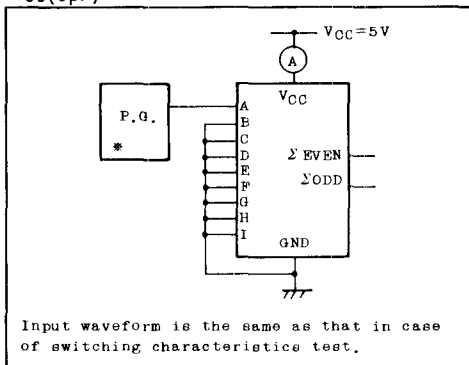
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

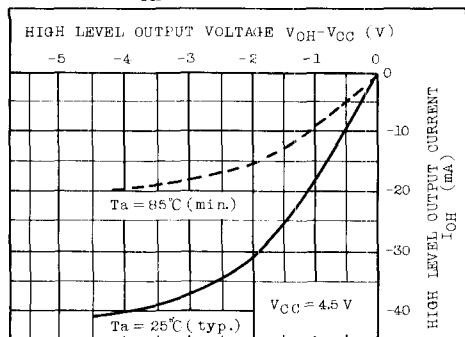


$I_{CC(opr)}$ TEST CIRCUIT

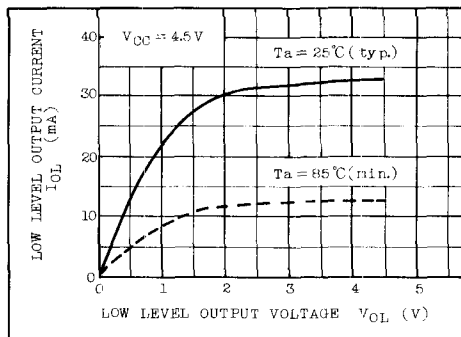


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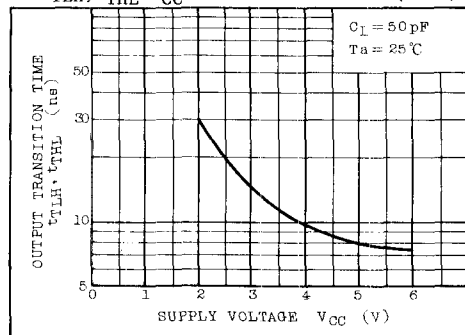
I_{OH} CHARACTERISTICS



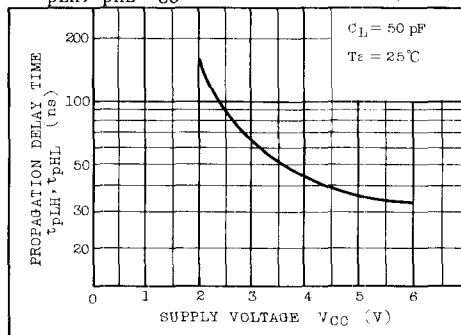
I_{OL} CHARACTERISTICS



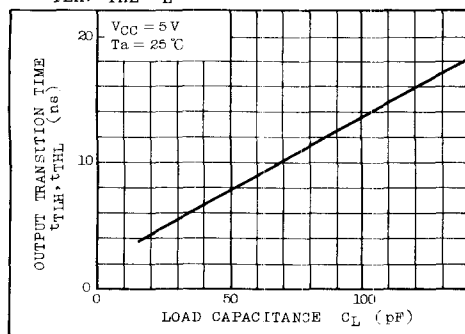
$t_{TLH}, t_{THL}-V_{CC}$ CHARACTERISTICS (TYP.)



$t_{PLH}, t_{PHL}-V_{CC}$ CHARACTERISTICS (TYP.)



$t_{TLH}, t_{THL}-C_L$ CHARACTERISTICS (TYP.)



$t_{PLH}, t_{PHL}-C_L$ CHARACTERISTICS (TYP.)

