

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

**8 GBIT (1G × 8 BIT) CMOS NAND E<sup>2</sup>PROM (Multi-Level-Cell)****DESCRIPTION**

The TC58NVG3D2 is a single 3.3 V 8 Gbit (8,984,199,168 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E<sup>2</sup>PROM) organized as (8192 + 376) bytes × 128 pages × 1028 blocks.

The device has two 8568-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 8568-byte increments. The Erase operation is implemented in a single block unit (1 Mbytes + 47 Kbytes: 8568 bytes × 128 pages).

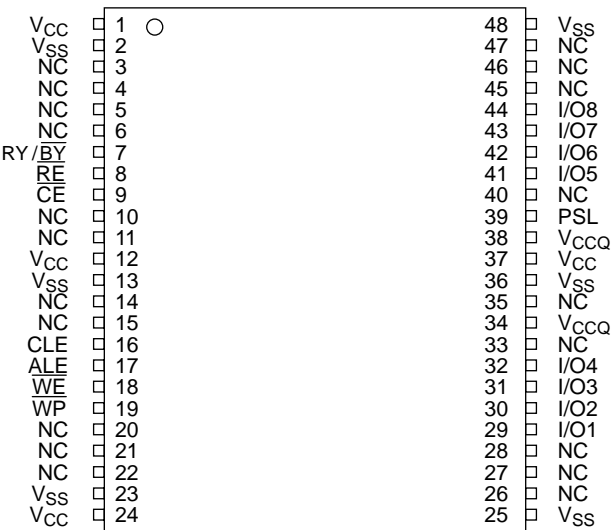
The TC58NVG3D2 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

**FEATURES**

- Organization

	TC58NVG3D2E
Memory cell array	8568 × 128.5K × 8
Register	8568 × 8
Page size	8568 bytes
Block size	(1M + 47 K) bytes
- Modes
  - Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy,
- Mode control
  - Serial input/output
  - Command control
- Number of valid blocks
  - Min 984 blocks
  - Max 1028 blocks
- Power supply
  - V<sub>CC</sub> = 2.7 V to 3.6 V
  - V<sub>CCQ</sub> = 2.7 V to 3.6 V
- Access time
  - Cell array to register    200 μs max
  - Serial Read Cycle        25 ns min
- Program/Erase time
  - Auto Page Program       1400 μs/page typ.
  - Auto Block Erase        3 ms/block typ.
- Operating current
  - Read (30 ns cycle)       30 mA max.
  - Program (avg.)           30 mA max.
  - Erase (avg.)            30 mA max.
  - Standby                  100 μA max
- Package
  - TSOP I 48-P-1220-0.50C    (Weight: 0.53 g typ.)
- FOR RELIABILITY GUIDANCE, PLEASE REFER TO THE APPLICATION NOTES AND COMMENTS (17).  
24 bit ECC for each 1024 bytes is required.

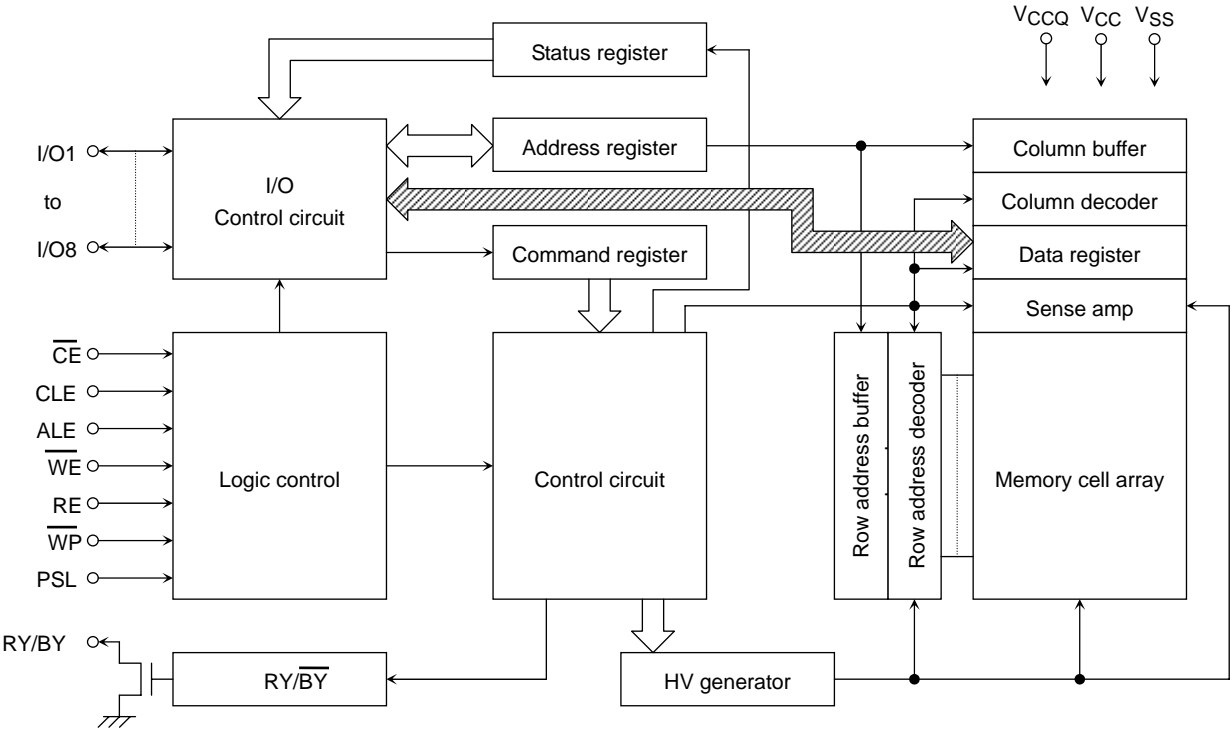
**PIN ASSIGNMENT (TOP VIEW)**



**PIN NAMES**

I/O1 to I/O8	I/O port
$\overline{\text{CE}}$	Chip enable
$\overline{\text{WE}}$	Write enable
$\overline{\text{RE}}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
PSL	Power on select
$\overline{\text{WP}}$	Write protect
RY/ $\overline{\text{BY}}$	Ready/Busy
V <sub>CC</sub>	Power supply
V <sub>CCQ</sub>	I/O port Power supply
V <sub>SS</sub>	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
$V_{CC}/V_{CCQ}$	Power Supply Voltage	-0.6 to 4.6	V
$V_{IN}$	Input Voltage	-0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	-0.6 V to $V_{CC} + 0.3$ V ( $\leq 4.6$ V)	V
$P_D$	Power Dissipation	0.3	W
$T_{SOLDER}$	Soldering Temperature (10 s)	260	°C
$T_{STG}$	Storage Temperature	-55 to 150	°C
$T_{OPR}$	Operating Temperature	0 to 70	°C

CAPACITANCE \*( $T_a = 25^\circ\text{C}$ ,  $f = 1$  MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
$C_{IN}$	Input	$V_{IN} = 0$ V	—	10	pF
$C_{OUT}$	Output	$V_{OUT} = 0$ V	—	10	pF

\* This parameter is periodically sampled and is not tested for every device.

**VALID BLOCKS**

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N <sub>VB</sub>	Number of Valid Blocks	984	—	1028	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.

The first block (Block 0) is guaranteed to be a valid block at the time of shipment.

The specification for the minimum number of valid blocks is applicable over the device lifetime.

\* The number of valid blocks includes extended blocks.

**RECOMMENDED DC OPERATING CONDITIONS**

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V <sub>CC</sub> / V <sub>CCQ</sub>	Power Supply Voltage		2.7 V	—	3.6 V	V
V <sub>IH</sub>	High Level input Voltage	2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	0.8 × V <sub>CC</sub>	—	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Low Level Input Voltage	2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	−0.3*	—	0.2 × V <sub>CC</sub>	V

\* −2 V (pulse width lower than 20 ns)

**DC CHARACTERISTICS (Ta = 0 to 70 °C, V<sub>CC</sub> = 2.7 V to 3.6 V)**

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	—	—	±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 V to V <sub>CCQ</sub>	—	—	±10	μA
I <sub>CCO0</sub> *	Power On Reset Current	PSL = GND or NU	—	—	30	mA
		PSL = V <sub>CC</sub> , FFh command input after Power On	—	—	30	
I <sub>CCO1</sub>	Serial Read Current	$\overline{CE}$ = V <sub>IL</sub> , I <sub>OUT</sub> = 0 mA, t <sub>cycle</sub> = 30 ns	—	—	30	mA
I <sub>CCO2</sub>	Programming Current	—	—	—	30	mA
I <sub>CCO3</sub>	Erasing Current	—	—	—	30	mA
I <sub>CCS</sub>	Standby Current	$\overline{CE}$ = V <sub>CC</sub> − 0.2 V, $\overline{WP}$ = 0 V/V <sub>CC</sub> , PSL = 0 V/V <sub>CC</sub> /NU	—	—	100	μA
V <sub>OH</sub>	High Level Output Voltage	I <sub>OH</sub> = −0.4 mA (2.7 V ≤ V <sub>CCQ</sub> ≤ 3.6 V)	2.4	—	—	V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>OL</sub> = 2.1 mA (2.7 V ≤ V <sub>CCQ</sub> ≤ 3.6 V)	—	—	0.4	V
I <sub>OL</sub> (R <sub>Y</sub> /B <sub>Y</sub> )	Output current of R <sub>Y</sub> /B <sub>Y</sub> pin	V <sub>OL</sub> = 0.4 V (2.7 V ≤ V <sub>CCQ</sub> ≤ 3.6 V)	—	8	—	mA

\* Refer to application note (2) for detail

**AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

(Ta = 0 to 70 , Vcc = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
tCLS	CLE Setup Time	0	—	ns
tCLS2	CLE Setup Time	30	—	ns
tCLH	CLE Hold Time	5	—	ns
tCS	$\overline{CE}$ Setup Time	8	—	ns
tCS2	$\overline{CE}$ Setup Time	20	—	ns
tCH	$\overline{CE}$ Hold Time	5	—	ns
tWP	Write Pulse Width	12	—	ns
tALS	ALE Setup Time	0	—	ns
tALH	ALE Hold Time	5	—	ns
tDS	Data Setup Time	10	—	ns
tDH	Data Hold Time	5	—	ns
tWC	Write Cycle Time	25	—	ns
tWH	$\overline{WE}$ High Hold Time	10	—	ns
tWHW *	$\overline{WE}$ High Hold Time from final address to first data	80	—	ns
tWW	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
tRR	Ready to $\overline{RE}$ Falling Edge	20	—	ns
tRW	Ready to $\overline{WE}$ Falling Edge	20	—	ns
tRP	Read Pulse Width	12	—	ns
tRC	Read Cycle Time	25	—	ns
tREA	$\overline{RE}$ Access Time	—	20	ns
tCR	$\overline{CE}$ Low to $\overline{RE}$ Low	10	—	ns
tCLR	CLE Low to $\overline{RE}$ Low	10	—	ns
tAR	ALE Low to $\overline{RE}$ Low	10	—	ns
tRHOH	Data Output Hold Time from $\overline{RE}$ High	25	—	ns
tRLOH	Data Output Hold Time from $\overline{RE}$ Low	5	—	ns
tRHZ	$\overline{RE}$ High to Output High Impedance	—	60	ns
tCHZ	$\overline{CE}$ High to Output High Impedance	—	30	ns
tCLHZ	CLE High to Output High Impedance	—	30	ns
tREH	$\overline{RE}$ High Hold Time	10	—	ns
tIR	Output-High-impedance-to- $\overline{RE}$ Falling Edge	0	—	ns
tRHW	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
tWHC	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
tWHR	$\overline{WE}$ High to $\overline{RE}$ Low	180	—	ns
tR	Memory Cell Array to Starting Address	—	200	μs
tDCBSYR1	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	200	μs
tDCBSYR2	Data Cache Busy in Page Copy (following 3Ah)	—	205	μs
tWB	$\overline{WE}$ High to Busy	—	100	ns
tRST	Device Reset Time (Ready/Read/Program/Erase)	—	10/10/30/500	μs

\*  $t_{WHW}$  is the time from the  $\overline{WE}$  rising edge of final address cycle to the  $\overline{WE}$  falling edge of first data cycle.

## AC TEST CONDITIONS

PARAMETER	CONDITION
	$2.7\text{ V} \leq V_{CCQ} \leq 3.6\text{ V}$
Input level	0 V to $V_{CCQ}$
Input pulse rise and fall time	3ns
Input comparison level	$V_{CCQ}/2$
Output data comparison level	$V_{CCQ}/2$
Output load	$C_L$ (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the  $RY/\overline{BY}$  pin.  
(Refer to Application Note (9) toward the end of this document.)

## PROGRAMMING AND ERASING CHARACTERISTICS ( $T_a = 0$ to $70^\circ\text{C}$ , $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ )

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
$t_{\text{PROG}}$	Average Programming Time	—	1400	3000	$\mu\text{s}$	
$t_{\text{DCBSYW2}}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	3000	$\mu\text{s}$	(2)
N	Number of Partial Program Cycles in the Same Page	—	—	—		(1)
$t_{\text{BERASE}}$	Block Erasing Time	—	3	10	ms	

(1) Refer to Application Note (12) toward the end of this document.

(2)  $t_{\text{DCBSYW2}}$  depends on the timing between internal programming time and data in time.

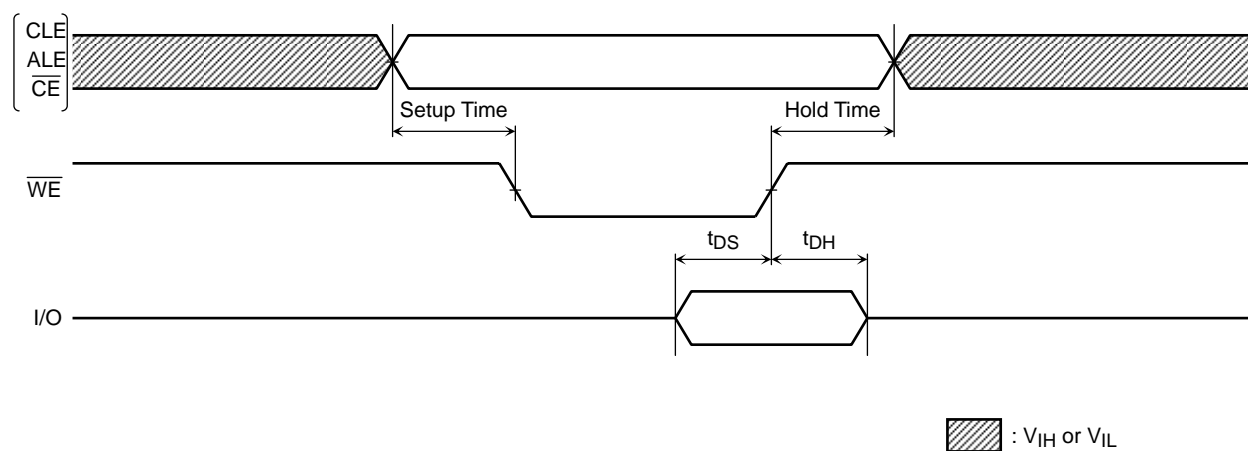
## Data Output

When  $t_{\text{REH}}$  is long, output buffers are disabled by  $/\text{RE}=\text{High}$ , and the hold time of data output depend on  $t_{\text{RHOH}}$  (30 ns MIN). On this condition, waveforms look like normal serial read mode.

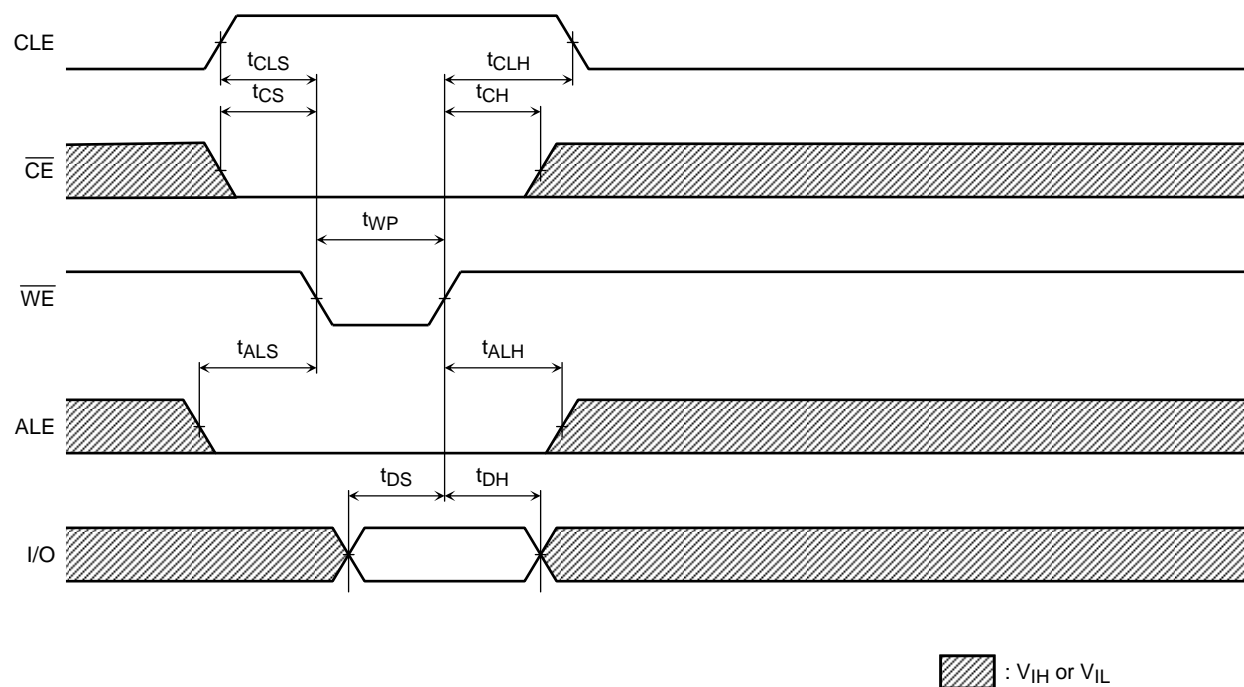
When  $t_{\text{REH}}$  is short, output buffers are not disabled by  $/\text{RE}=\text{High}$ , and the hold time of data output depend on  $t_{\text{RLOH}}$  (5ns MIN). On this condition, output buffers are disabled by the rising edge of  $\text{CLE}$ ,  $\text{ALE}$ ,  $/\text{CE}$  or falling edge of  $/\text{WE}$ , and waveforms look like Extended Data Output Mode.

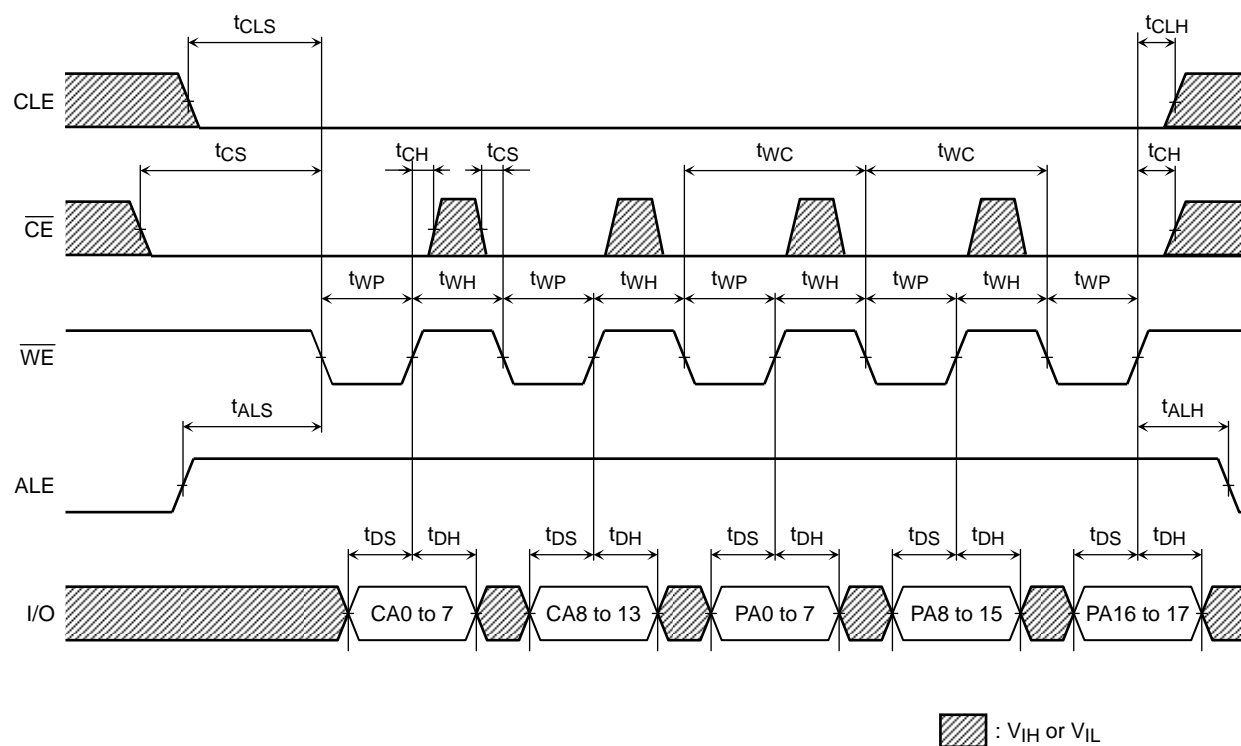
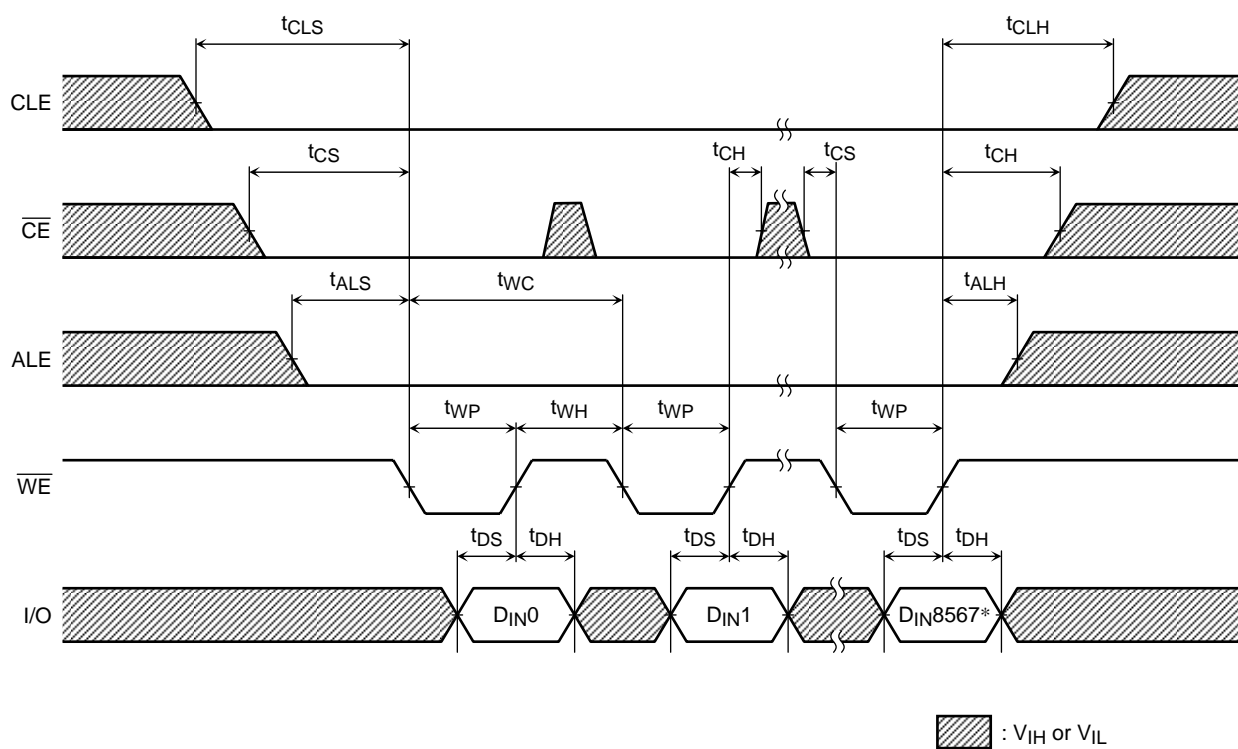
## TIMING DIAGRAMS

Latch Timing Diagram for Command/Address/Data



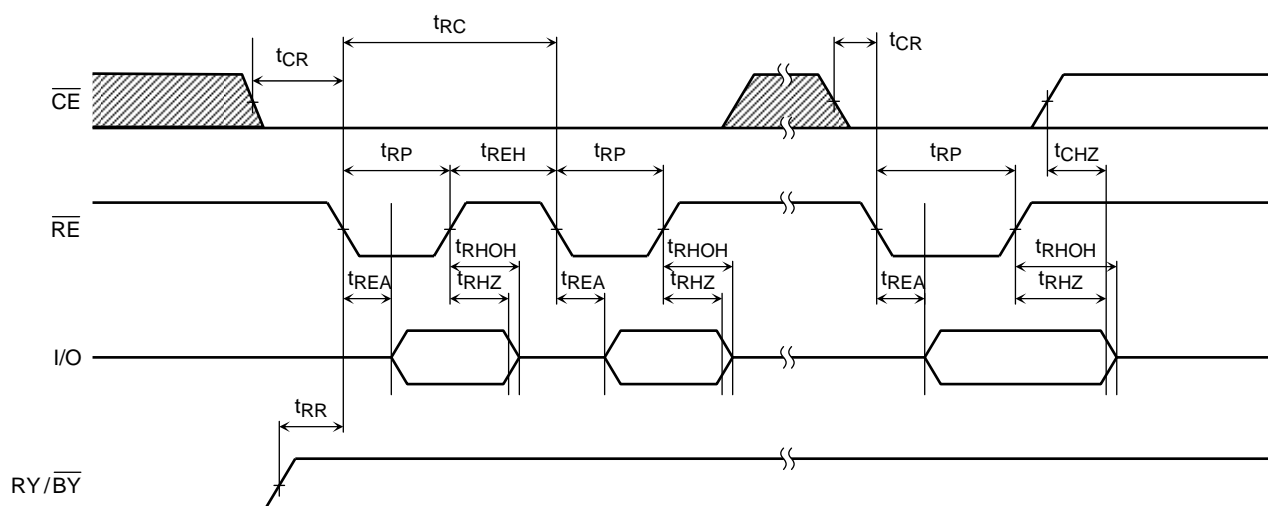
Command Input Cycle Timing Diagram



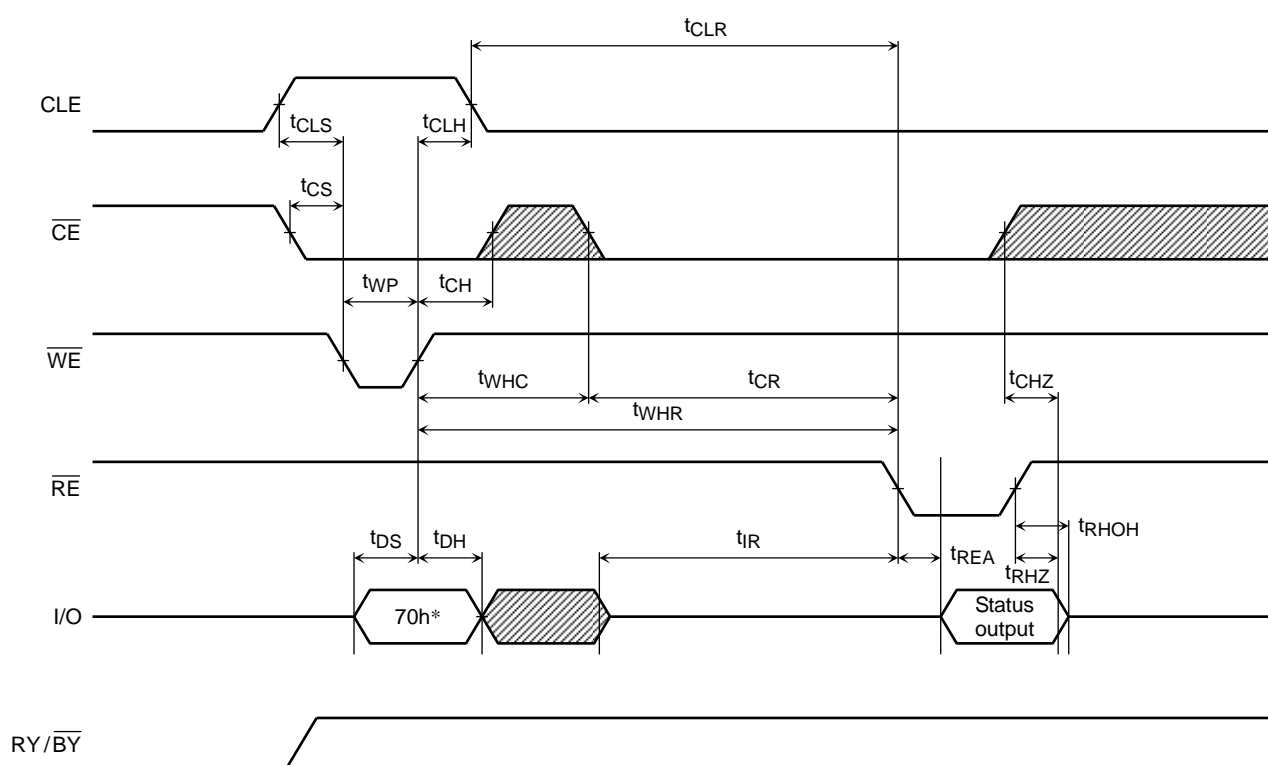
Address Input Cycle Timing DiagramData Input Cycle Timing Diagram



### Serial Read Cycle Timing Diagram

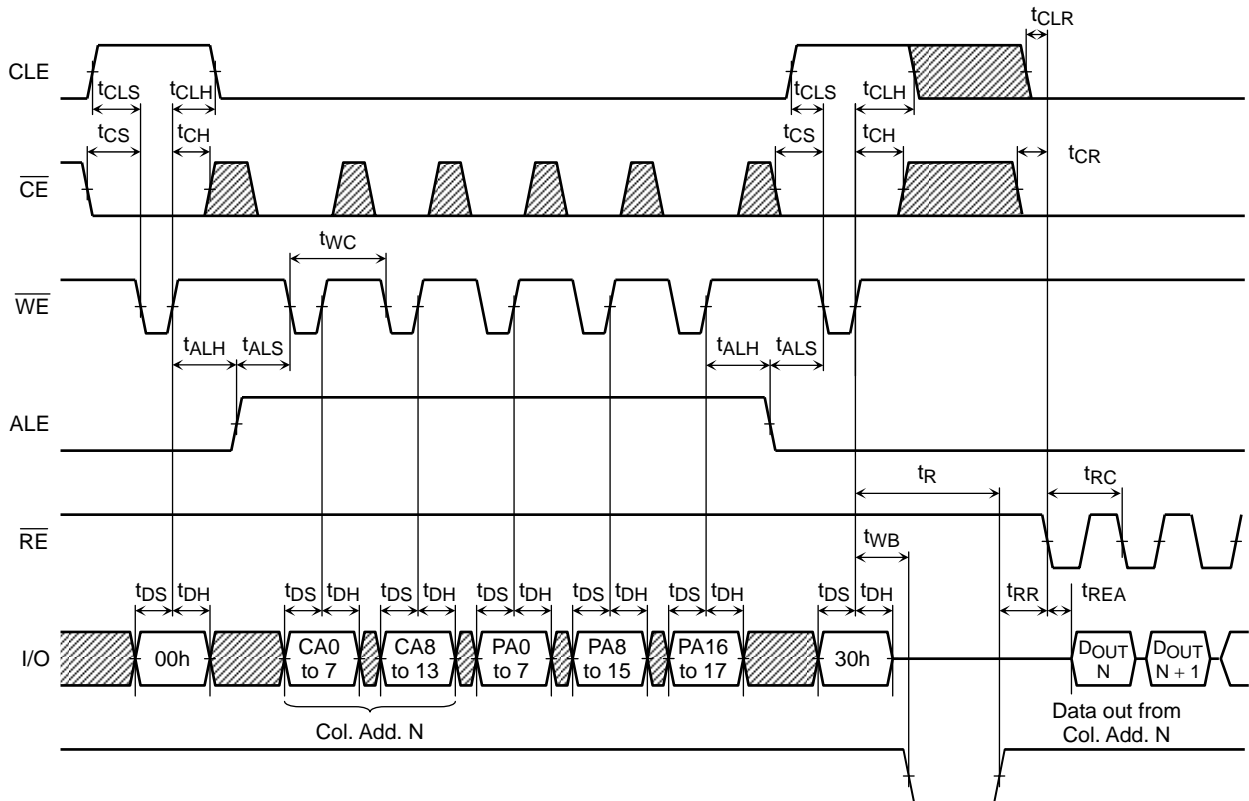
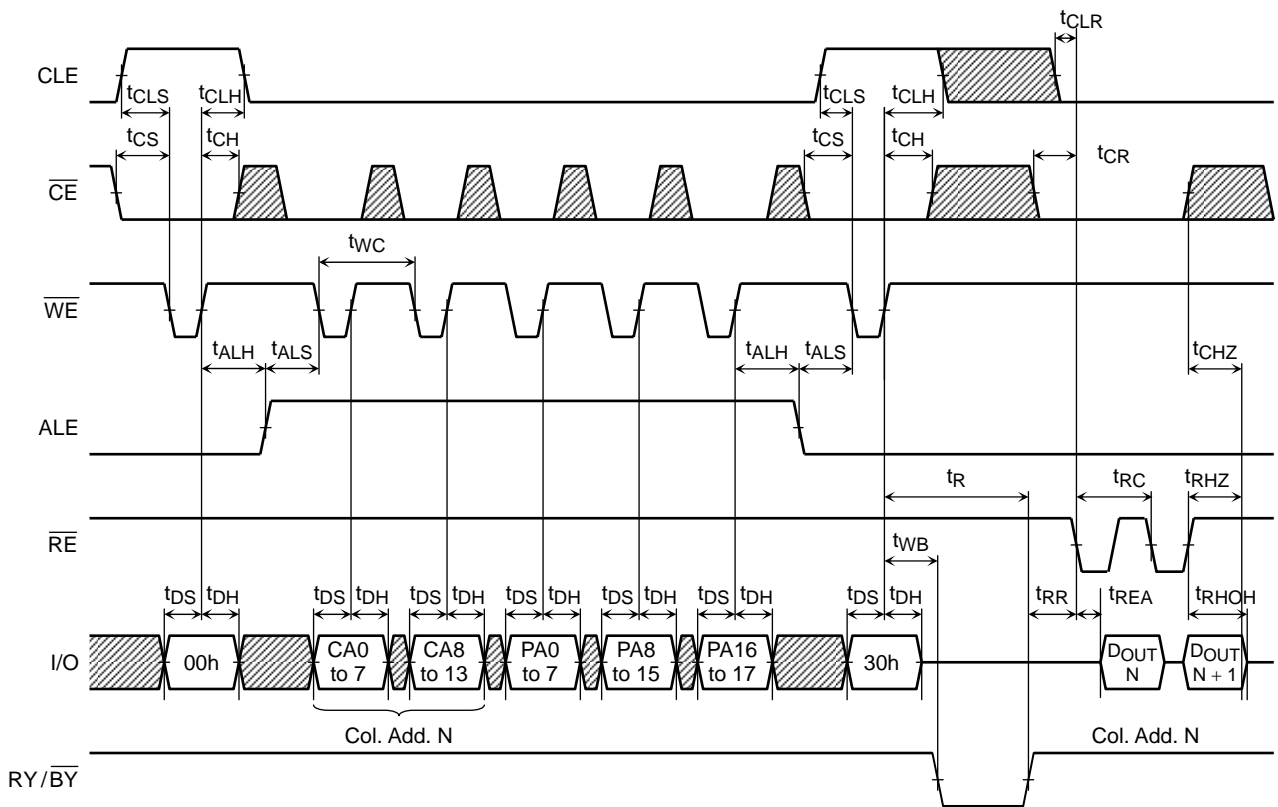


### Status Read Cycle Timing Diagram

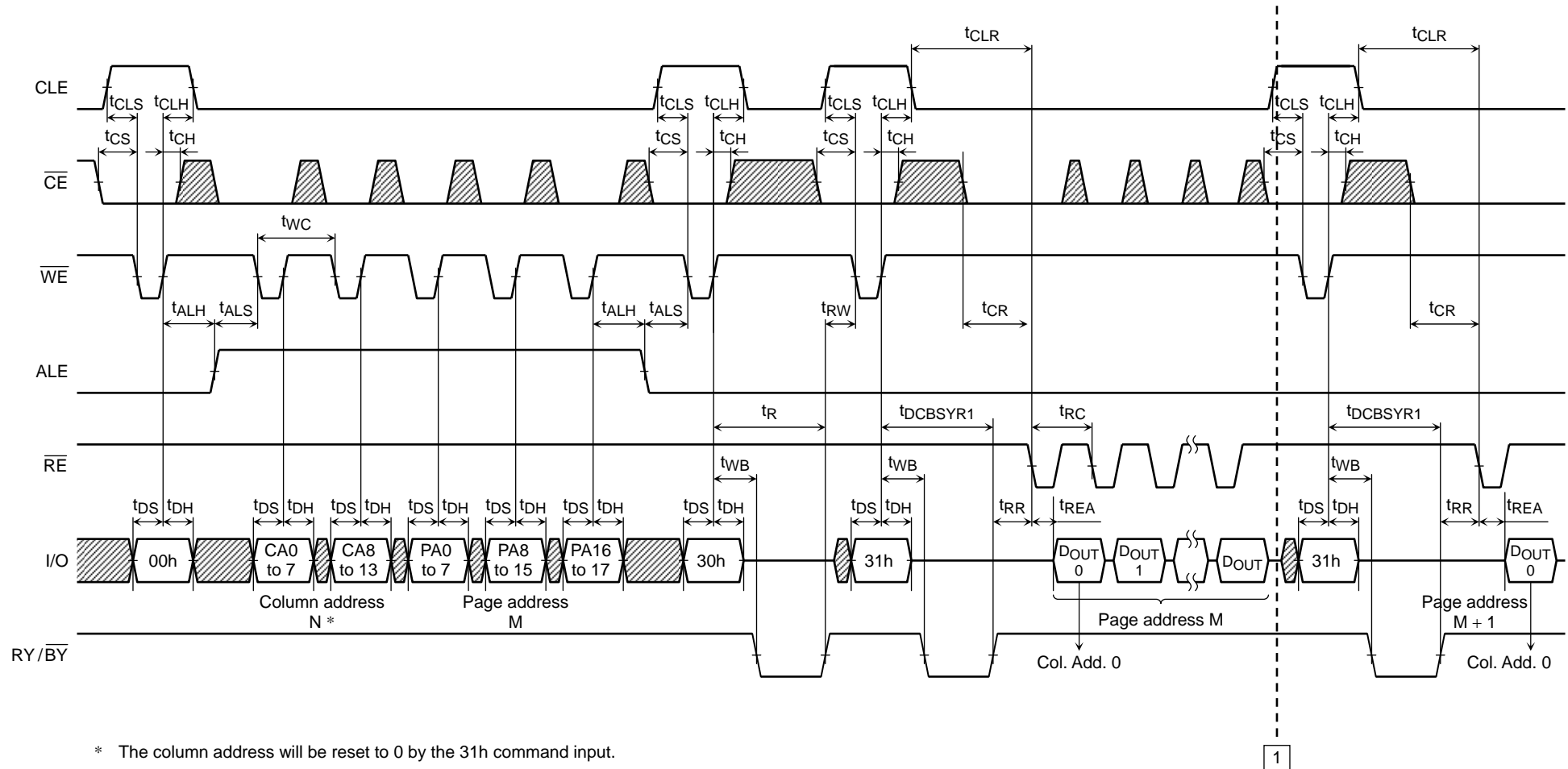


\*: 70h represents the hexadecimal number

 :  $V_{IH}$  or  $V_{IL}$

Read Cycle Timing DiagramRead Cycle Timing Diagram: When Interrupted by  $\overline{CE}$ 

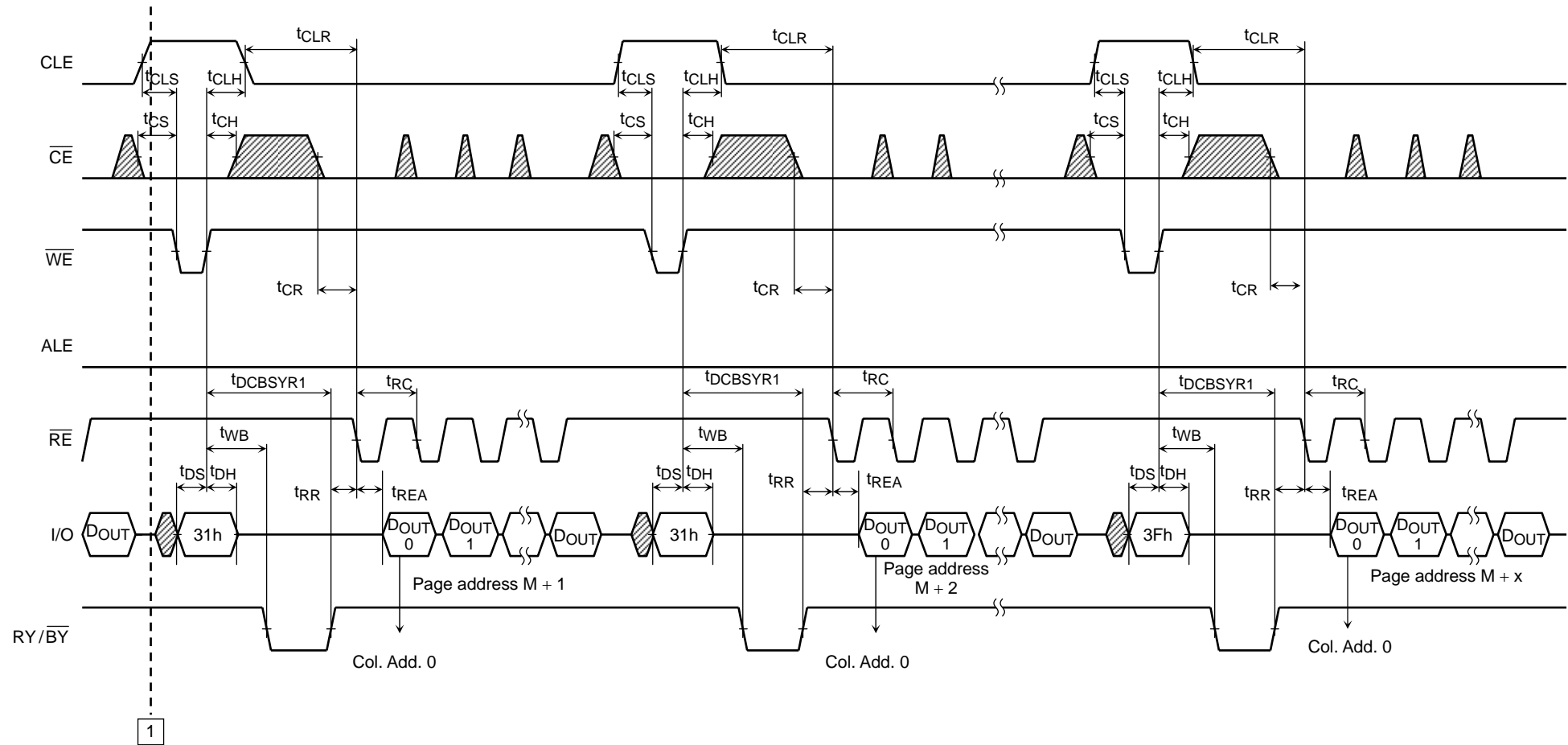
Read Cycle with Data Cache Timing Diagram (1/2)



\* The column address will be reset to 0 by the 31h command input.

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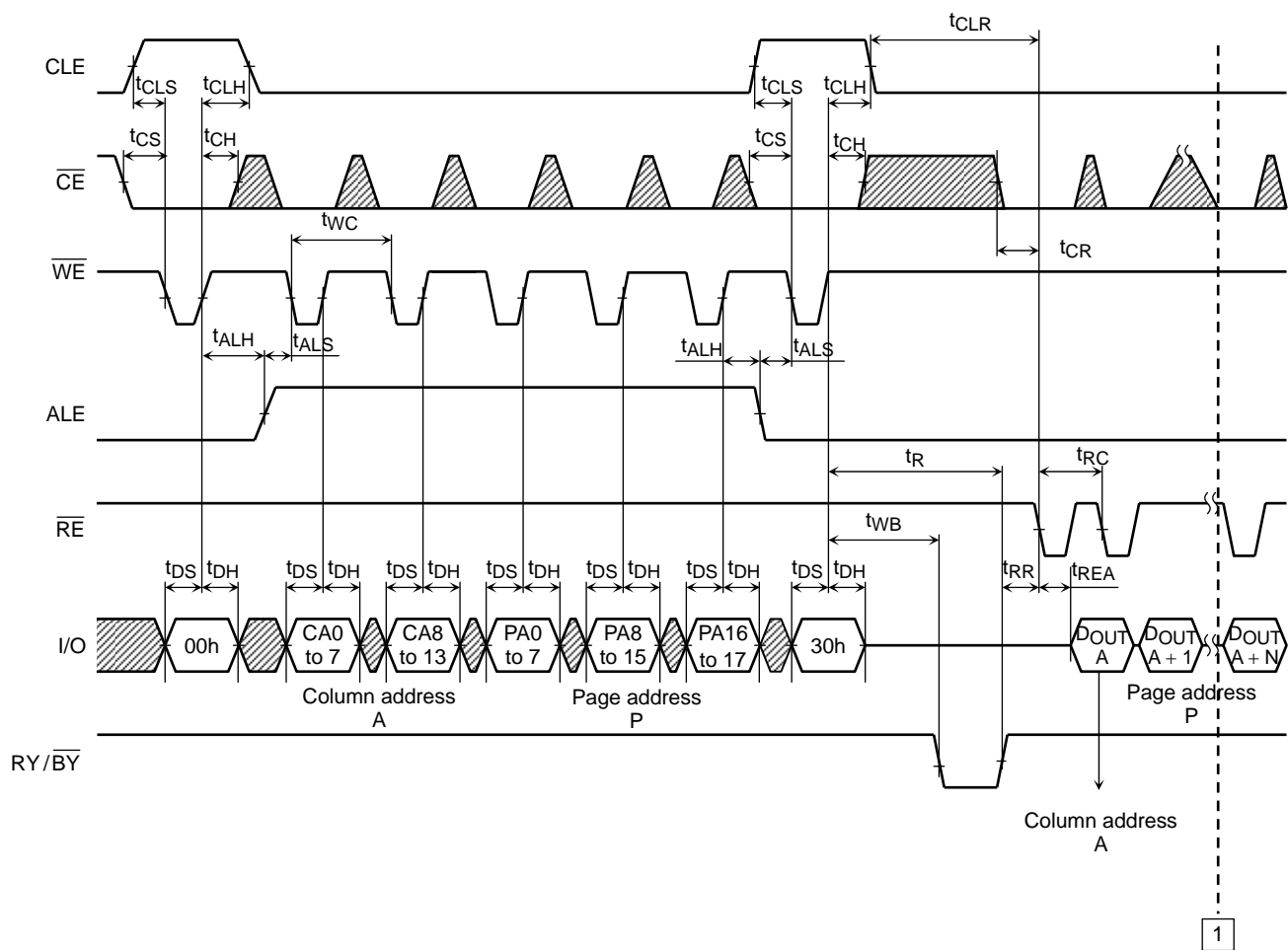
Read Cycle with Data Cache Timing Diagram (2/2)



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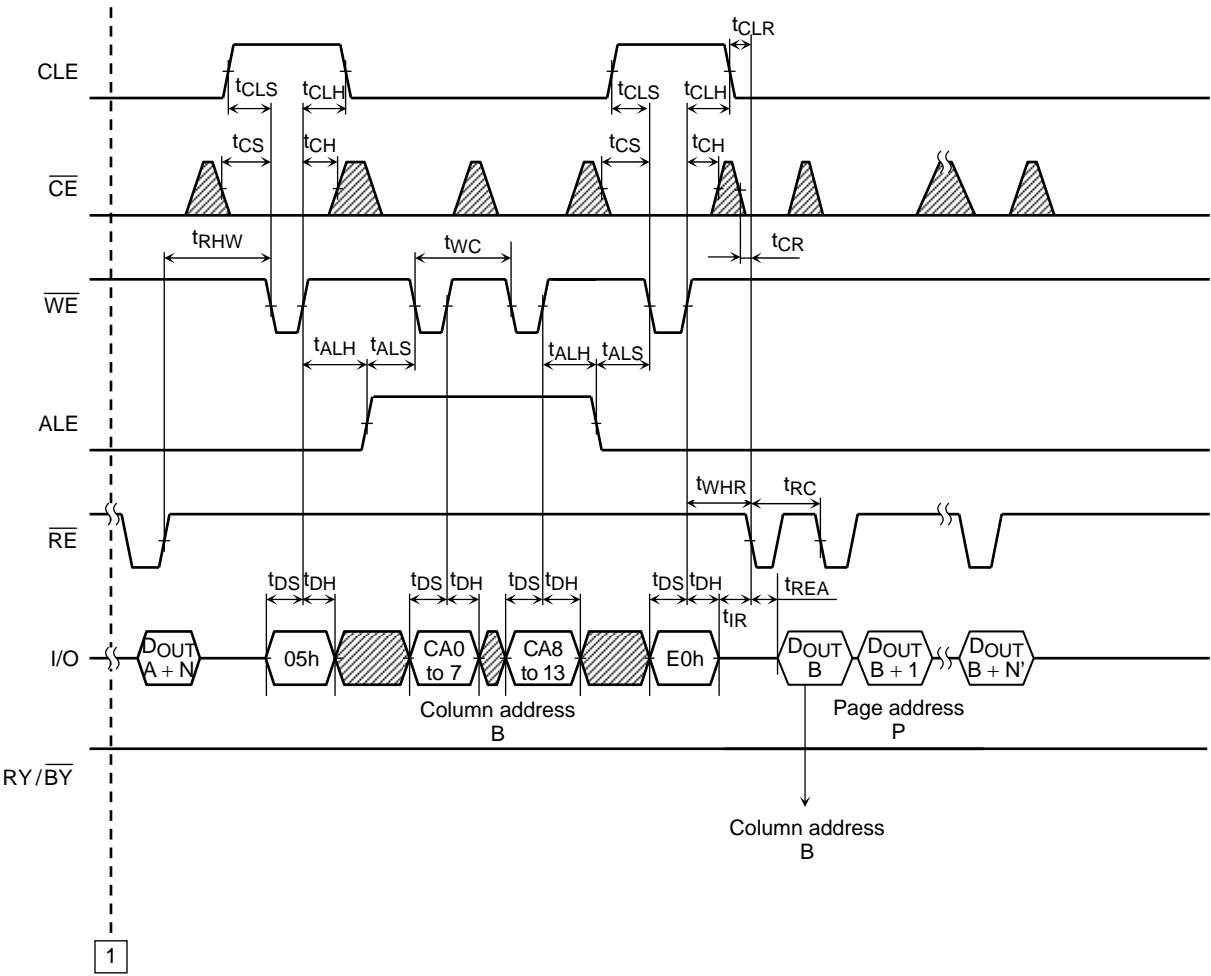
(Note) Make sure to terminate the operation with 3Fh command.

## Column Address Change in Read Cycle Timing Diagram (1/2)

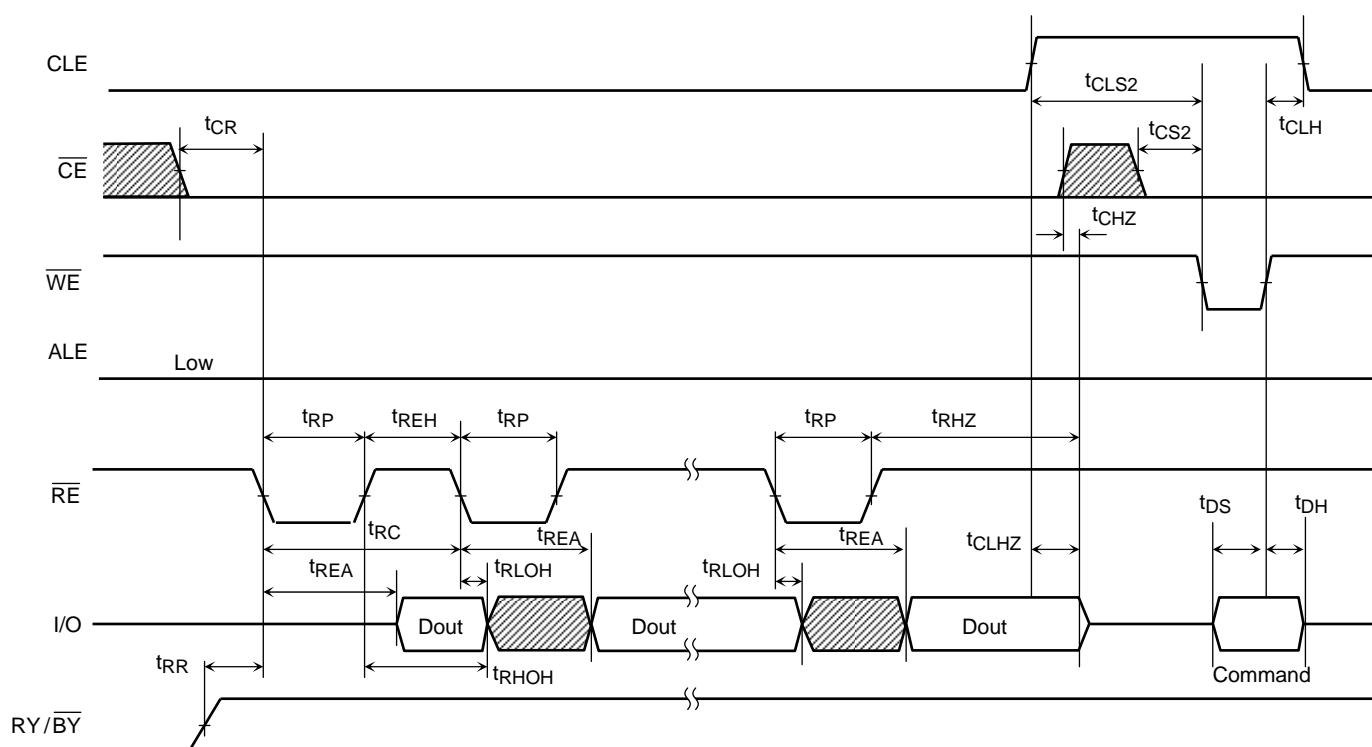


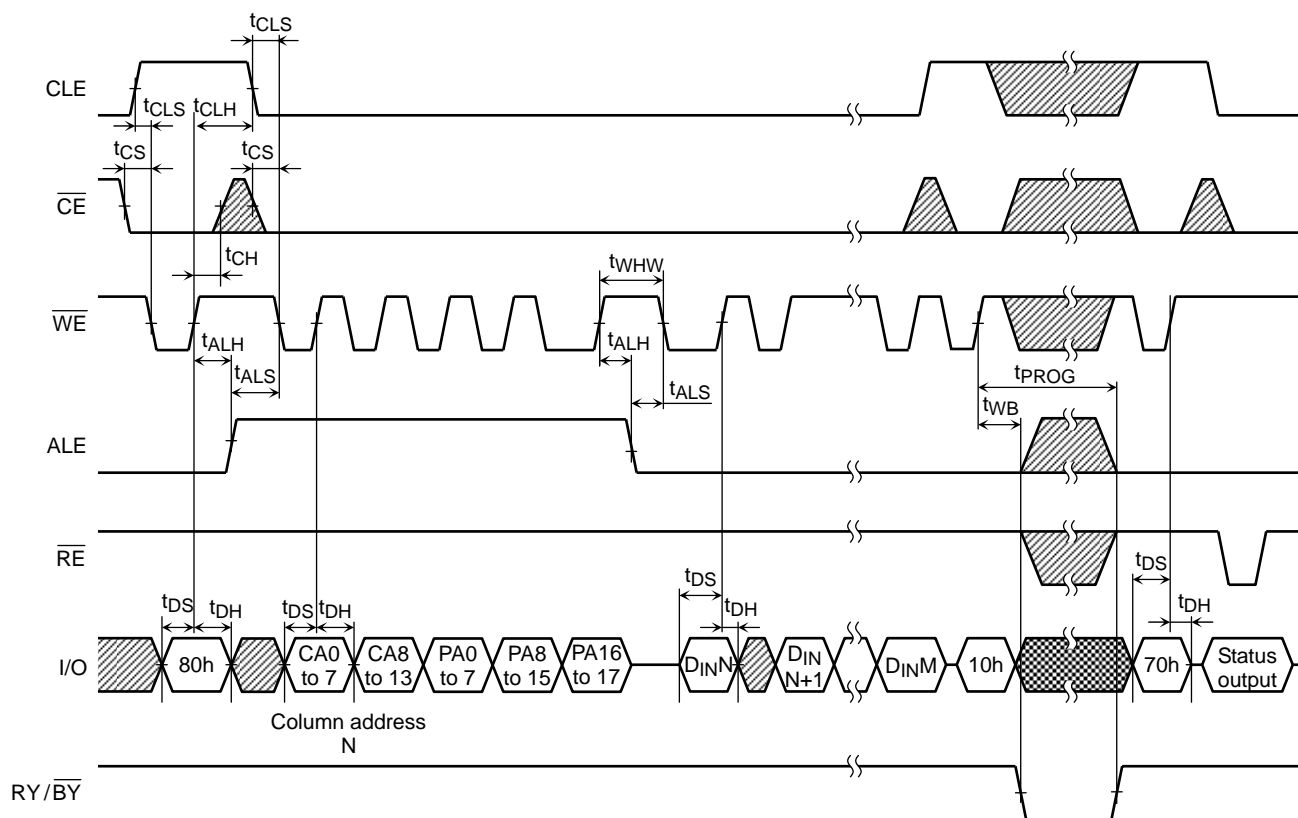
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Column Address Change in Read Cycle Timing Diagram (2/2)




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Data Output Timing Diagram

Auto-Program Operation Timing Diagram

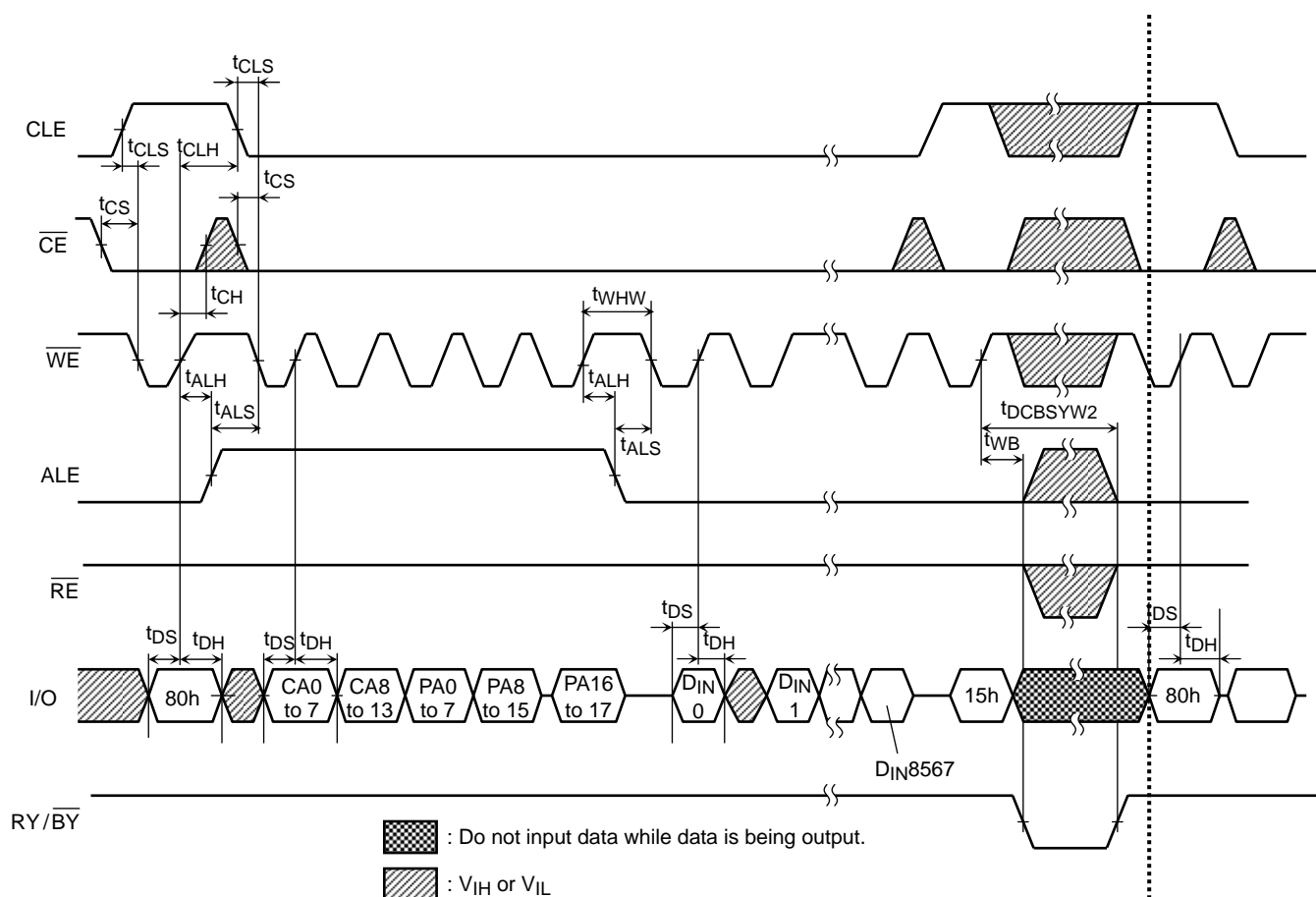
 : Do not input data while data is being output.

 :  $V_{IH}$  or  $V_{IL}$

\*) M: up to 8567



## Auto-Program Operation with Data Cache Timing Diagram (1/3)

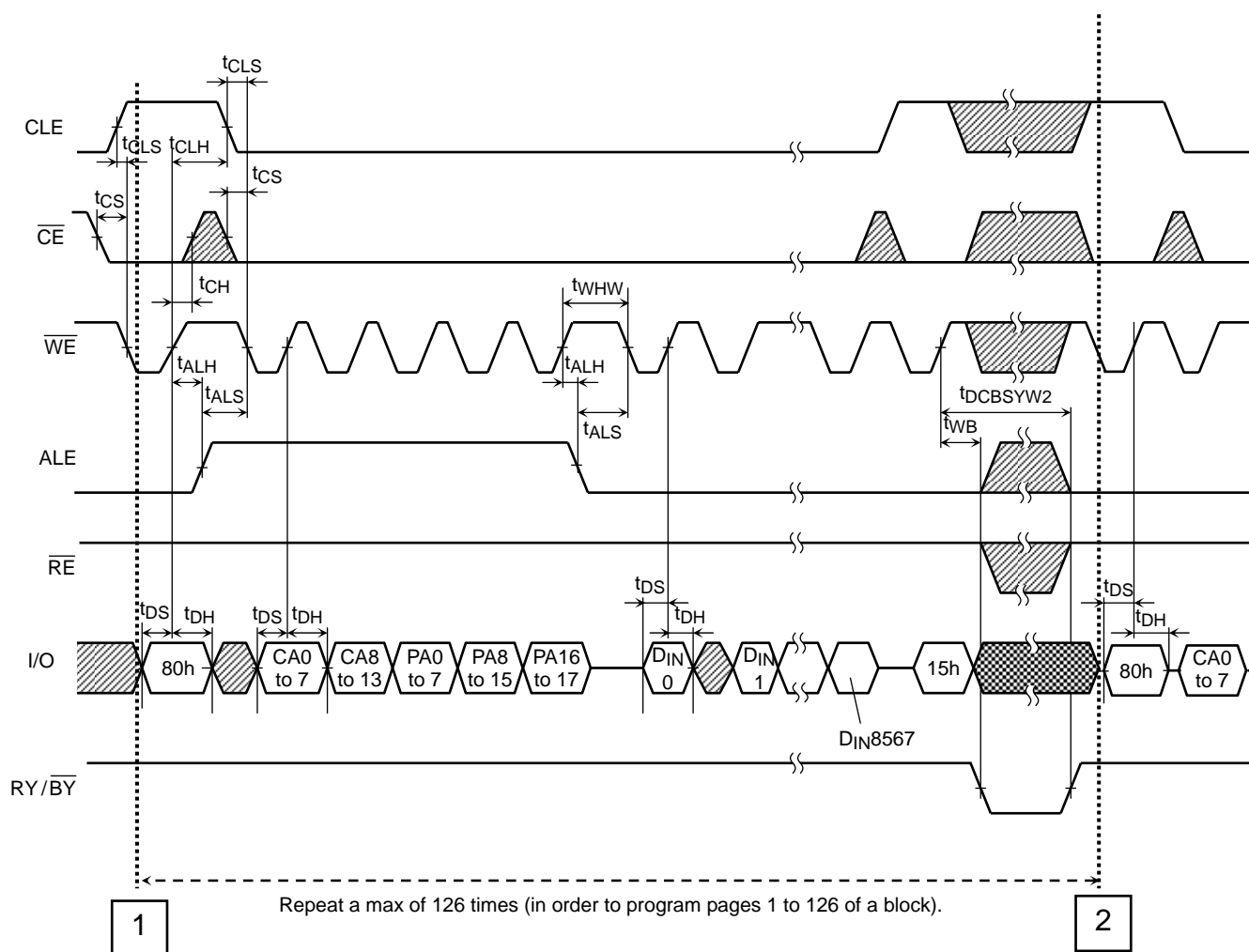


CA0 to CA12 is 0 in this diagram.


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## Auto-Program Operation with Data Cache Timing Diagram (2/3)

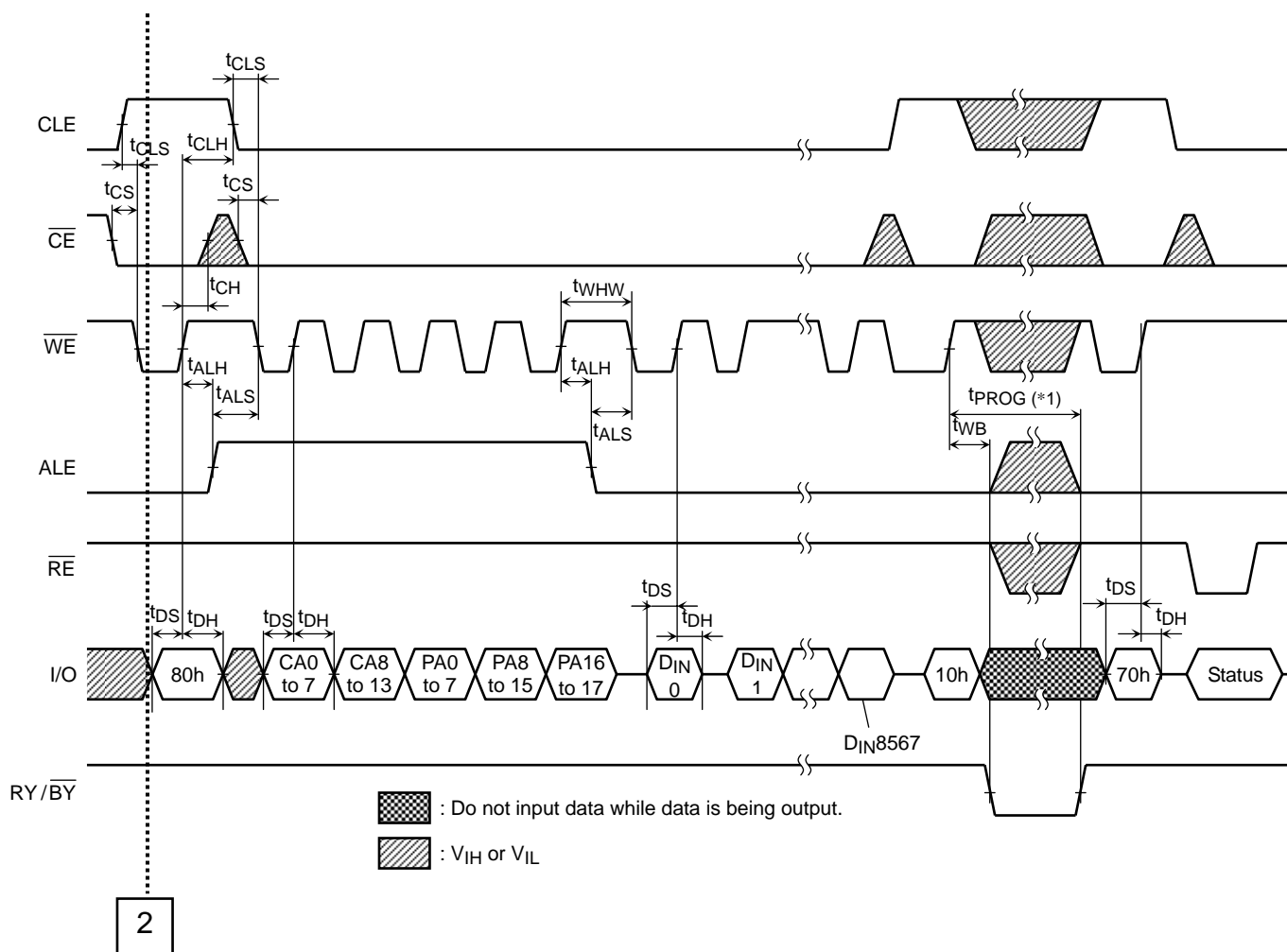


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 : Do not input data while data is being output.

 :  $V_{IH}$  or  $V_{IL}$

## Auto-Program Operation with Data Cache Timing Diagram (3/3)



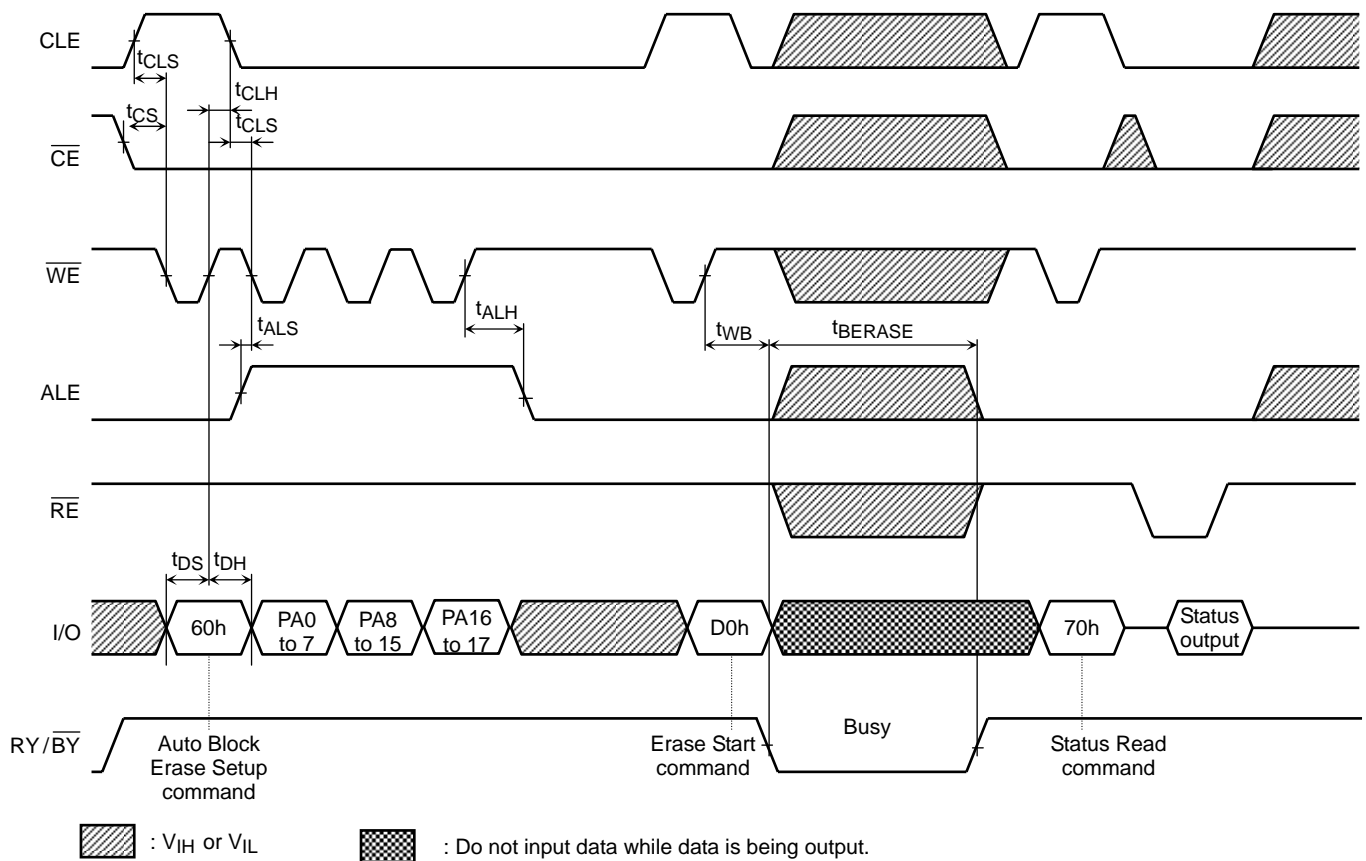
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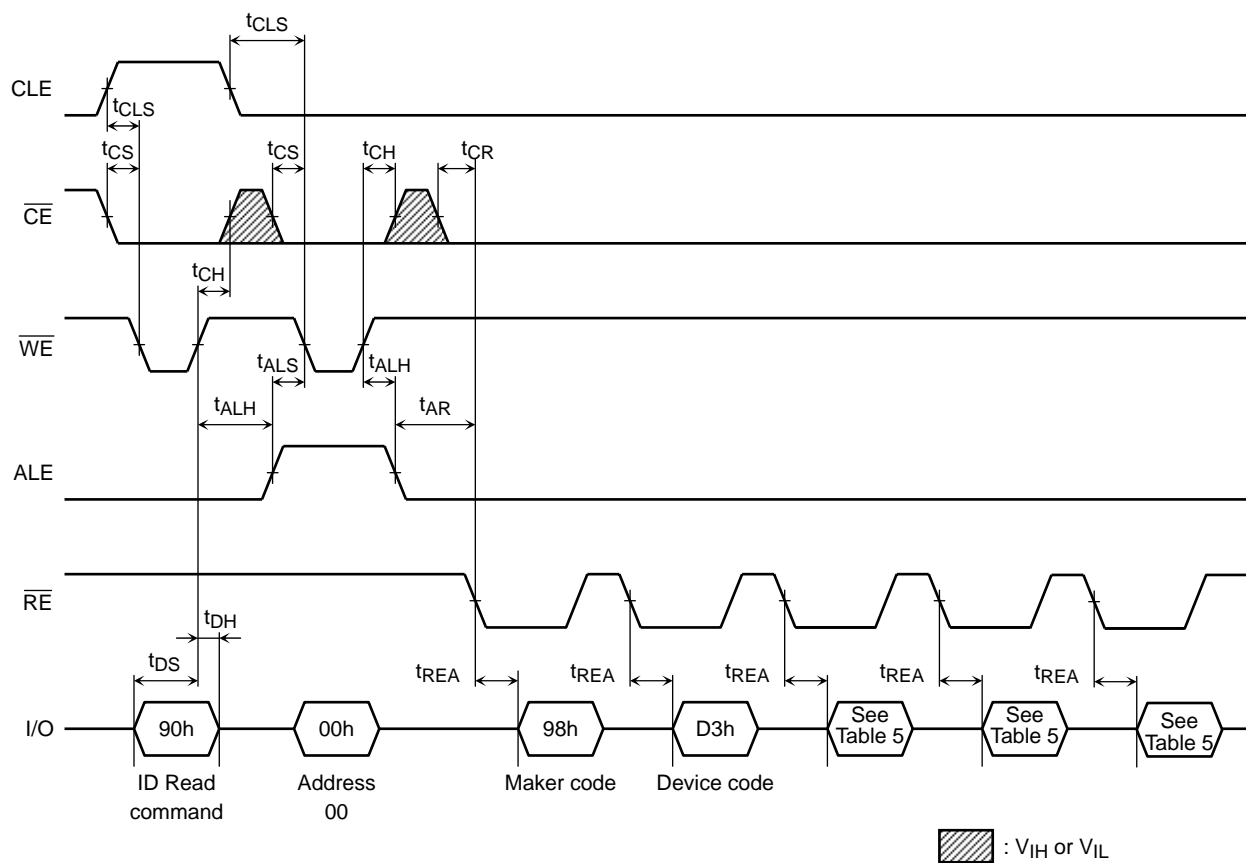
(\*1)  $t_{PROG}$ : Since the last page programming by 10h command is initiated after the previous cache program, the  $t_{PROG}$  during cache programming is given by the following equation.

$$t_{PROG} = t_{PROG} \text{ of the last page} + t_{PROG} \text{ of the previous page} - A$$

$A = (\text{command input cycle} + \text{address input cycle} + \text{data input cycle time of the last page})$

If "A" exceeds the  $t_{PROG}$  of previous page,  $t_{PROG}$  of the last page is  $t_{PROG} \text{ max.}$

Auto Block Erase Timing Diagram

ID Read Operation Timing Diagram

## PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

### Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the  $\overline{WE}$  signal while CLE is High.

### Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of  $\overline{WE}$  while ALE is High.

### Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when  $\overline{CE}$  goes High during the device is in Ready state. The  $\overline{CE}$  signal is ignored when device is in Busy state ( $RY/\overline{BY} = L$ ), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the  $\overline{CE}$  input goes High.

### Write Enable: $\overline{WE}$

The  $\overline{WE}$  signal is used to control the acquisition of data from the I/O port.

### Read Enable: $\overline{RE}$

The  $\overline{RE}$  signal controls serial data output. Data is available  $t_{REA}$  after the falling edge of  $\overline{RE}$ .

The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

### I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

### Write Protect: $\overline{WP}$

The  $\overline{WP}$  signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when  $\overline{WP}$  is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

### Ready/Busy: $RY/\overline{BY}$

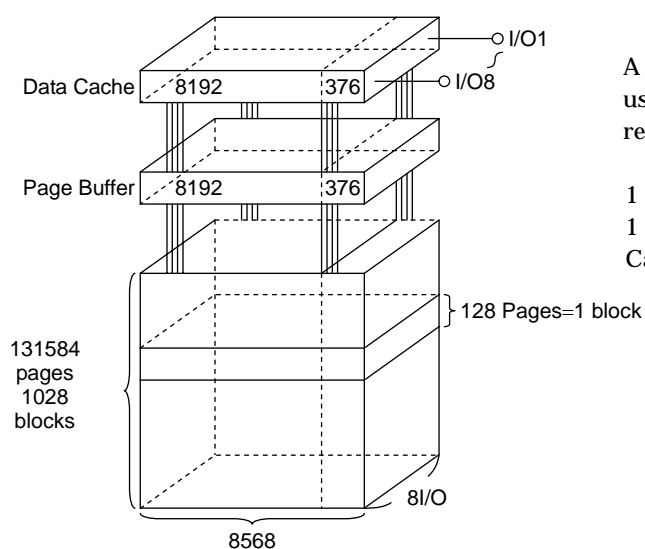
The  $RY/\overline{BY}$  output signal is used to indicate the operating condition of the device. The  $RY/\overline{BY}$  signal is in Busy state ( $RY/\overline{BY} = L$ ) during the Program, Erase and Read operations and will return to Ready state ( $RY/\overline{BY} = H$ ) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to  $V_{ccq}$  with an appropriate resistor.

### Power on Select: PSL

The PSL signal is used to select whether the device initialization should take place during the device power on or during the first Reset. Please refer to the application note (2) for details.

## Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 8568 bytes in which 8192 bytes are used for main memory storage and 376 bytes are for redundancy or for other uses.

1 page = 8568 bytes

1 block = 8568 bytes × 128 pages = (1M + 47K) bytes

Capacity = 8568 bytes × 128 pages × 1028 blocks

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth cycle	L	L	L	L	L	L	PA17	PA16

CA0 to CA13: Column address

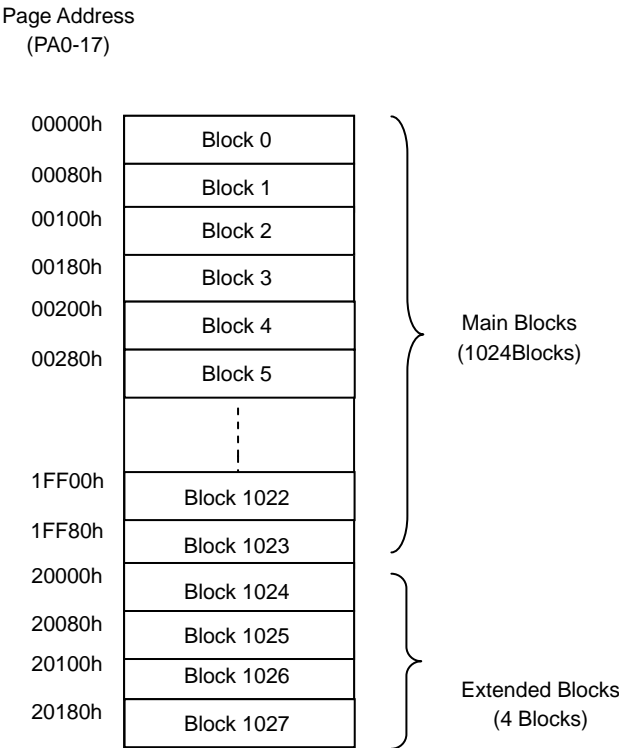
PA0 to PA17: Page address

PA7 to PA17: Block address

PA0 to PA6: NAND address in block

Extended Blocks Arrangement

The device has 4 extended blocks to increase valid blocks. Extended blocks can be accessed by the following addressing.









Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE,  $\overline{\text{CE}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{RE}}$  and  $\overline{\text{WP}}$  signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	$\overline{\text{WP}}$ *1	PSL *3
Command Input	H	L	L		H	*	0V/ V <sub>CC</sub> / NU
Data Input	L	L	L		H	H	0V/ V <sub>CC</sub> / NU
Address input	L	H	L		H	*	0V/ V <sub>CC</sub> / NU
Serial Data Output	L	L	L	H		*	0V/ V <sub>CC</sub> / NU
During Program (Busy)	*	*	*	*	*	H	0V/ V <sub>CC</sub> / NU
During Erase (Busy)	*	*	*	*	*	H	0V/ V <sub>CC</sub> / NU
During Read (Busy)	*	*	H	*	*	*	0V/ V <sub>CC</sub> / NU
	*	*	L	H (*2)	H (*2)	*	0V/ V <sub>CC</sub> / NU
Program, Erase Inhibit	*	*	*	*	*	L	0V/ V <sub>CC</sub> / NU
Standby	*	*	H	*	*	0 V/V <sub>CC</sub>	0V/ V <sub>CC</sub> / NU

H: V<sub>IH</sub>, L: V<sub>IL</sub>, \*: V<sub>IH</sub> or V<sub>IL</sub>

\*1: Refer to Application Note (10) toward the end of this document regarding the  $\overline{\text{WP}}$  signal when Program or Erase Inhibit

\*2: If  $\overline{\text{CE}}$  is low during read busy,  $\overline{\text{WE}}$  and  $\overline{\text{RE}}$  must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

\*3: PSL must be tied to either 0V or V<sub>cc</sub>, or left unconnected (NU).

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Read with Data Cache	31	—	
Read Start for Last Page in Read Cycle with Data Cache	3F	—	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Program with Data Cache	80	15	
Read for Page Copy (2)	00	3A	
Auto Program with Data Cache during Page Copy (2)	8C	15	
Auto Program for last page during Page Copy (2)	8C	10	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	○
Reset	FF	—	○

HEX data bit assignment

(Example)

Serial Data Input: 80h

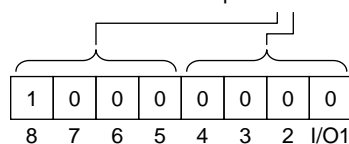
Table 4 shows the operation states for Read mode, when t<sub>REH</sub> is long.

Table 4. Read mode operation states

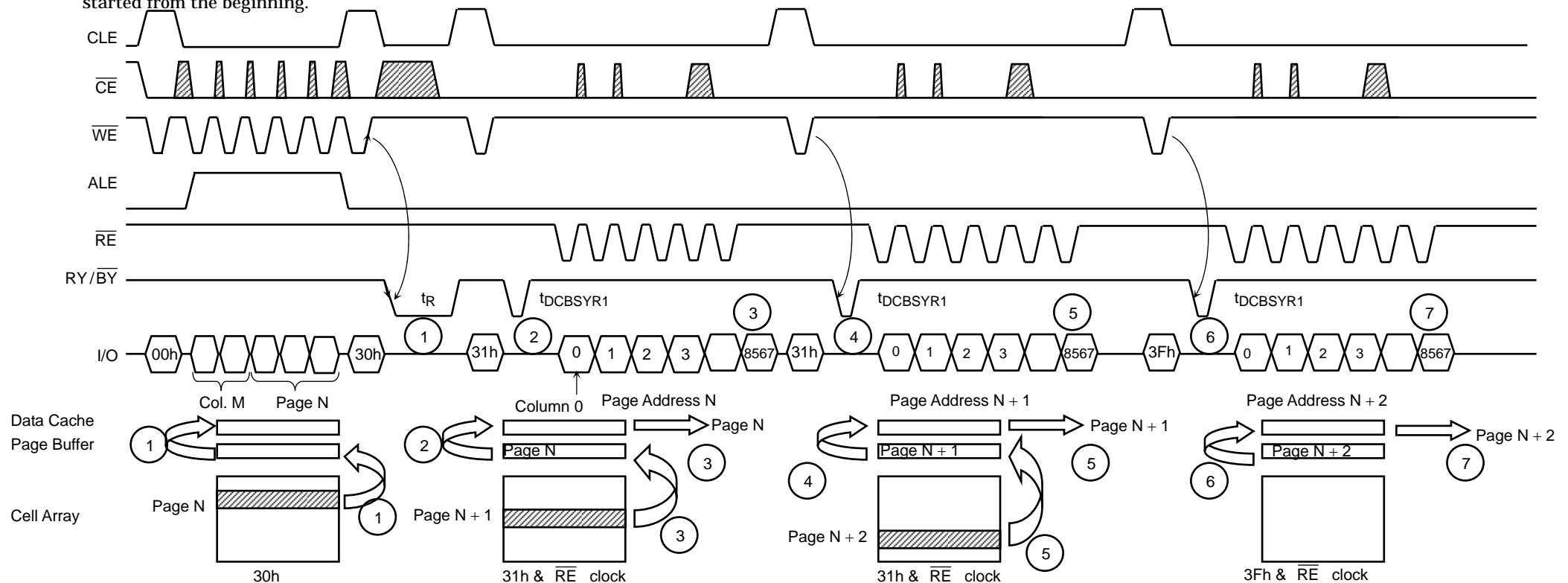
	CLE	ALE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V<sub>IH</sub>, L: V<sub>IL</sub>



## Read Operation with Read Cache

The device has a Read operation with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.

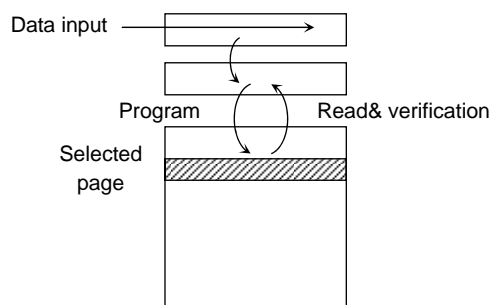
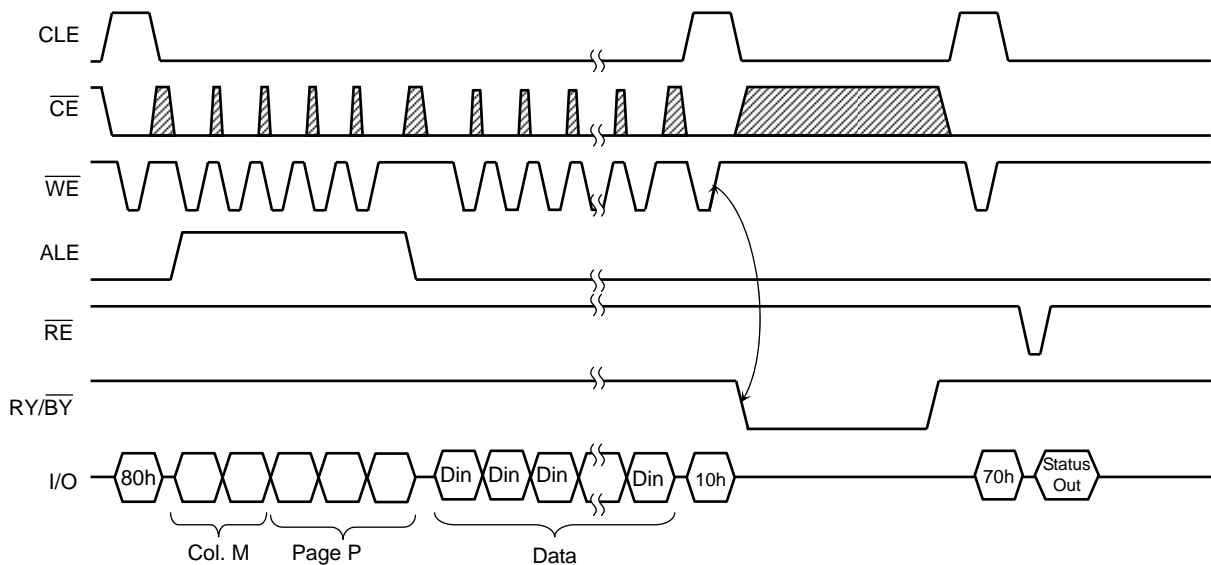


If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the  $t_R$  (Data transfer from memory cell to data register) will be reduced.

- 1 Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for  $t_R$  max.
- 2 After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes  $t_{DCBSYR1}$  max and the completion of this time period can be detected by Ready/Busy signal.
- 3 Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data cache can be read out by /RE clock simultaneously.
- 4 The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for  $t_{DCBSYR1}$  max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
- 5 Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data cache can be read out by /RE clock simultaneously
- 6 The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for  $t_{DCBSYR1}$  max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.
- 7 Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

### Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

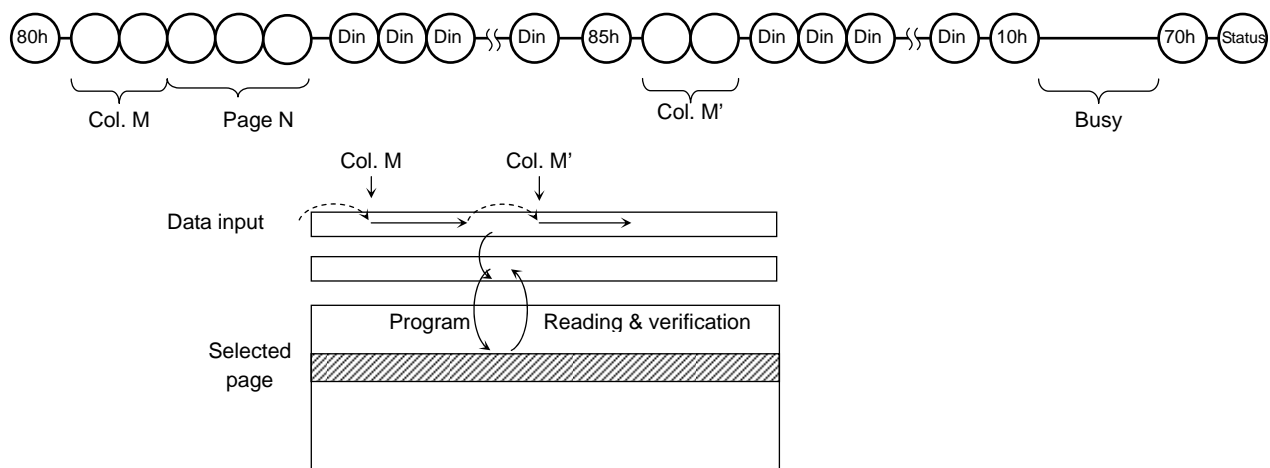


The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of WE following input of the "10h" command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

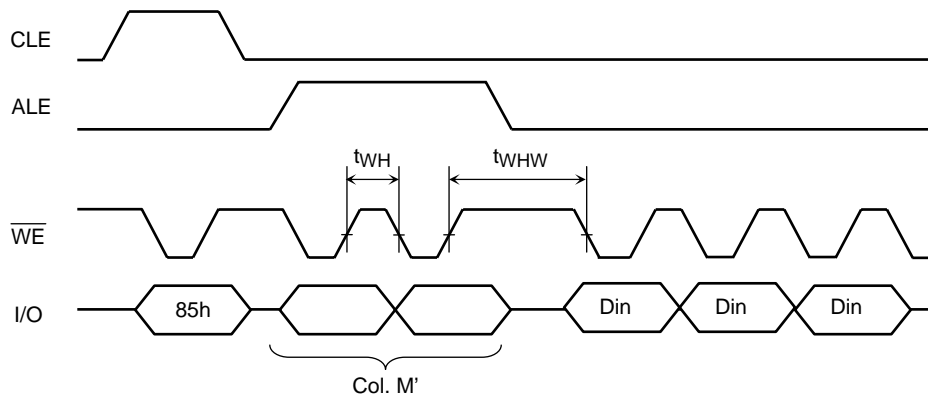
### Random Column Address Change in Auto Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.

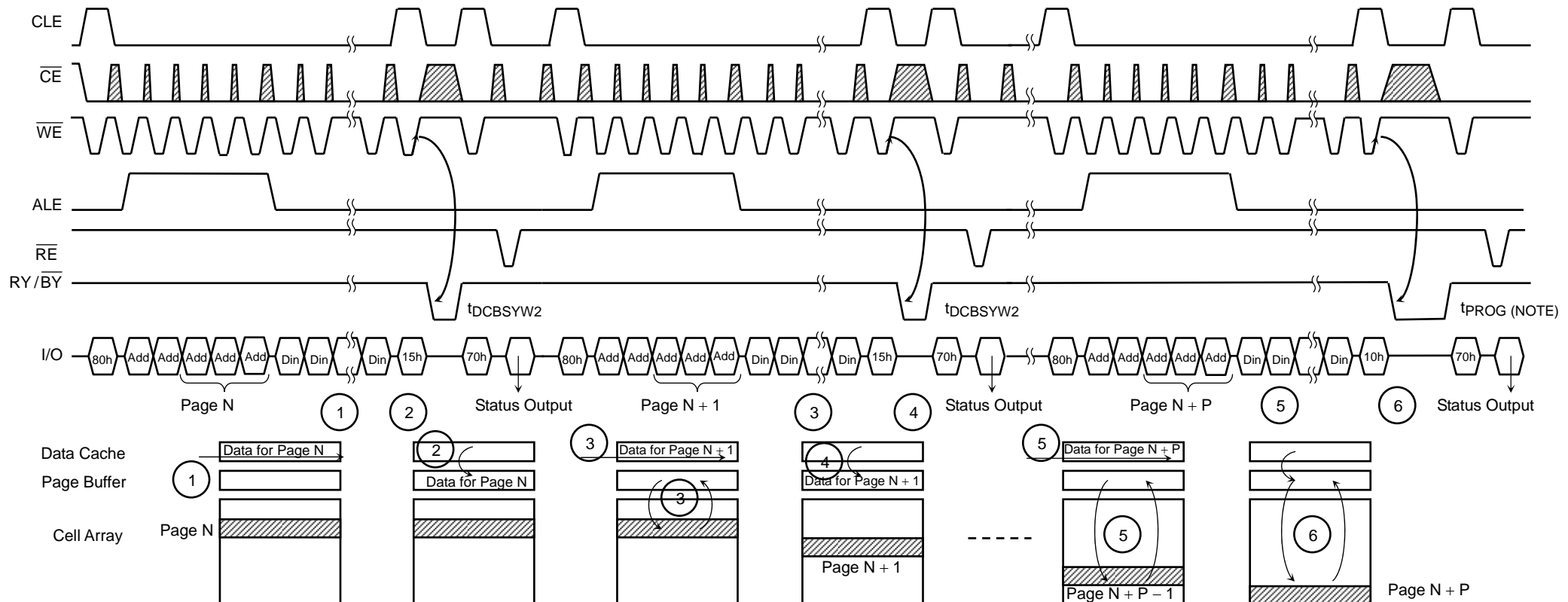


$t_{WHW}$  is the time from the the  $\overline{WE}$  rising edge of final address cycle to the  $\overline{WE}$  falling edge of first data cycle.  
 $\overline{WE}$  High Hold Time for the final address input after 85h command is also needed more time ( $t_{WHW}$ ) than  $t_{WH}$ .



## Auto Page Program Operation with Data Cache

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes this sequenced has to be started from the beginning.



Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache

- 1 Data for Page N is input to Data Cache.
- 2 Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy outputs Busy State ( $t_{DCBSYW2}$ ).
- 3 Data is programmed to the selected page while the data for page N + 1 is input to the Data Cache.
- 4 By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of page N is completed. The device output busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of page N and serial data input for Page N + 1 ( $t_{DCBSYW2}$ ).
- 5 Data for Page N + P is input to the Data Cache while the data of the Page N + P - 1 is being programmed.
- 6 The programming with Data Cache is terminated by the 10h command. When the device becomes Ready, it shows that the internal programming of the Page N + P is completed.

NOTE: Since the last page programming by the 10h command is initiated after the previous cache program, the  $t_{PROG}$  during cache programming is given by the following;

$$t_{PROG} = t_{PROG} \text{ for the last page} + t_{PROG} \text{ of the previous page} - (\text{command input cycle} + \text{address input cycle} + \text{data input cycle time of the last page})$$

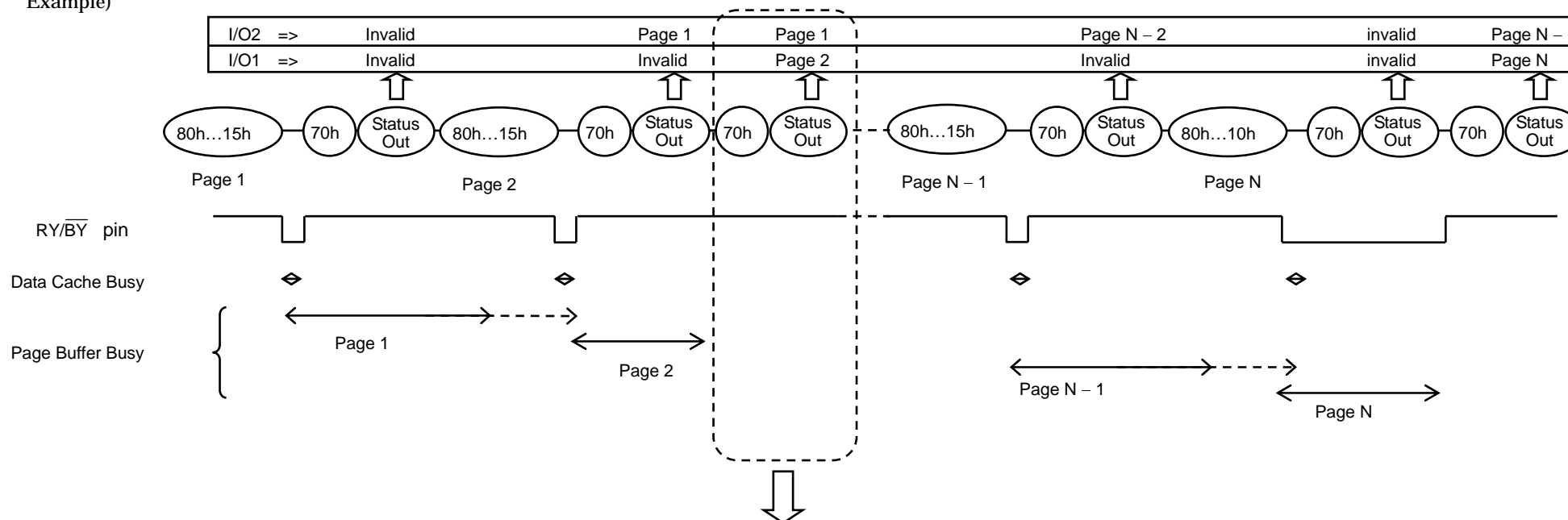
Pass/fail status for each page programmed by the Auto Page Programming with Data Cache operation can be detected by the Status Read operation.

- I/O1 : Pass/fail of the current page program operation.
- I/O2 : Pass/fail of the previous page program operation.

The Pass/Fail status on I/O1 and I/O2 are valid under the following conditions.

- Status on I/O1: Page Buffer Ready/Busy is Ready State.  
The Page Buffer Ready/Busy is output on I/O6 by Status Read operation or  $\overline{RY}/\overline{BY}$  pin after the 10h command
- Status on I/O2: Data Cache Read/Busy is Ready State.  
The Data Cache Ready/Busy is output on I/O7 by Status Read operation or  $\overline{RY}/\overline{BY}$  pin after the 15h command.

Example)



If the Page Buffer Busy returns to Ready before the next 80h command input, and if Status Read is done during this Ready period, the Status Read provides pass/fail for Page 2 on I/O1 and pass/fail result for Page1 on I/O2



Operating restriction during the Program with Data Cache operation

(Restriction)

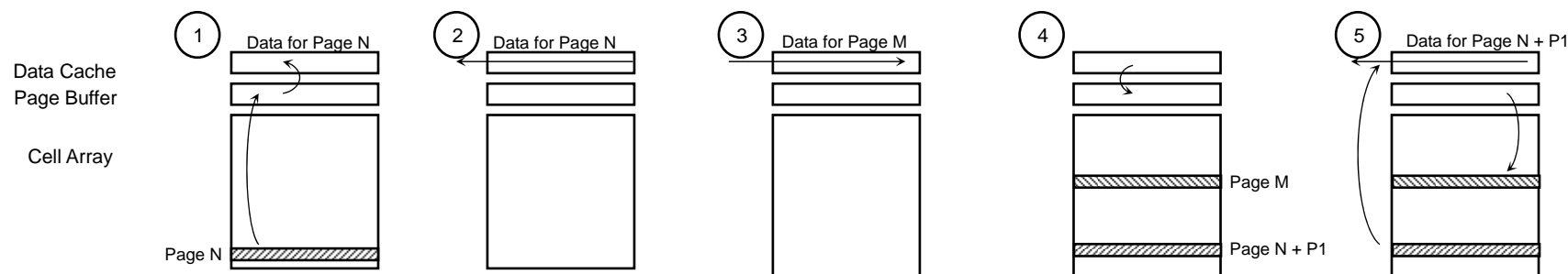
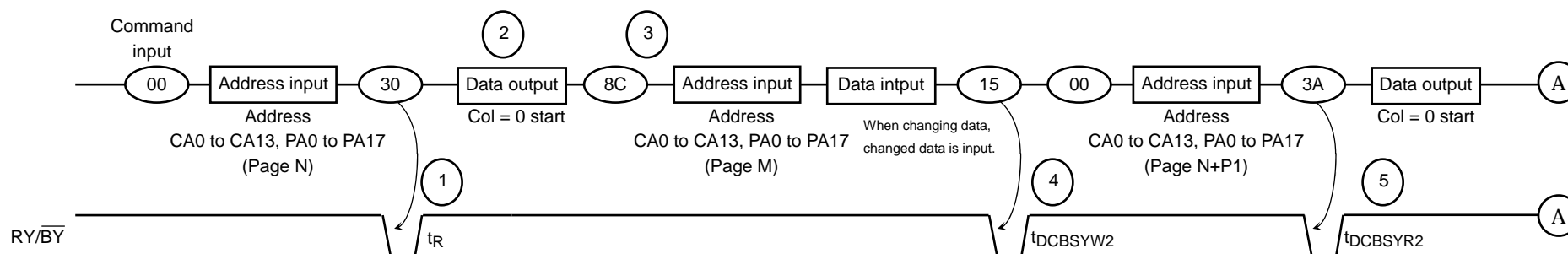
The operation has to be terminated with "10h" command.

Once the operation is started, no commands other than the commands shown in the timing diagram is allowed to be input except for Status Read command and reset command. If FF reset command is input before write operation to page B is complete, it may cause damage to data not only to the programmed page, but also to the adjacent page A. Regarding page A and B, please see below table.

Page A	Page B	Page A	Page B
0	2	⋮	⋮
1	4	⋮	⋮
3	6	⋮	⋮
5	8	97	100
7	10	99	102
9	12	101	104
11	14	103	106
13	16	105	108
15	18	107	110
17	20	109	112
19	22	111	114
21	24	113	116
23	26	115	118
25	28	117	120
27	30	119	122
⋮	⋮	121	124
⋮	⋮	123	126
⋮	⋮	125	127

## Page Copy (2)

By using Page Copy (2), data in a page can be copied to another page after the data has been read out. When the block address changes (increments) this sequenced has to be started from the beginning.

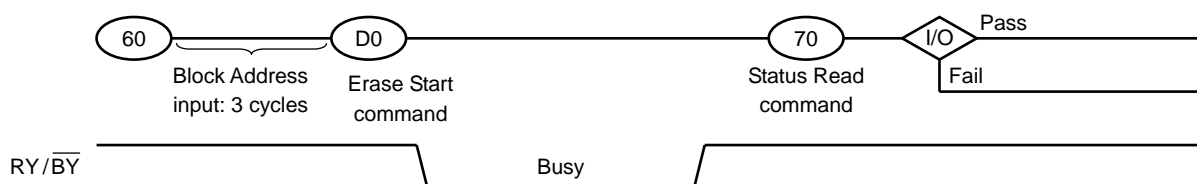


Page Copy (2) operation is as following.

- 1 Data for Page N is transferred to the Data Cache.
- 2 Data for Page N is read out.
- 3 Copy Page address M is input and if the data needs to be changed, changed data is input.
- 4 Data Cache for Page M is transferred to the Page Buffer.
- 5 After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.

### Auto Block Erase

The Auto Block Erase operation starts on the rising edge of  $\overline{WE}$  after the Erase Start command "D0h" which follows the Erase Setup command "60h". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



Make sure to terminate the operation with D0h command. If the operation needs to be terminated before D0h command input, input the FFh reset command to terminate the operation.

ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

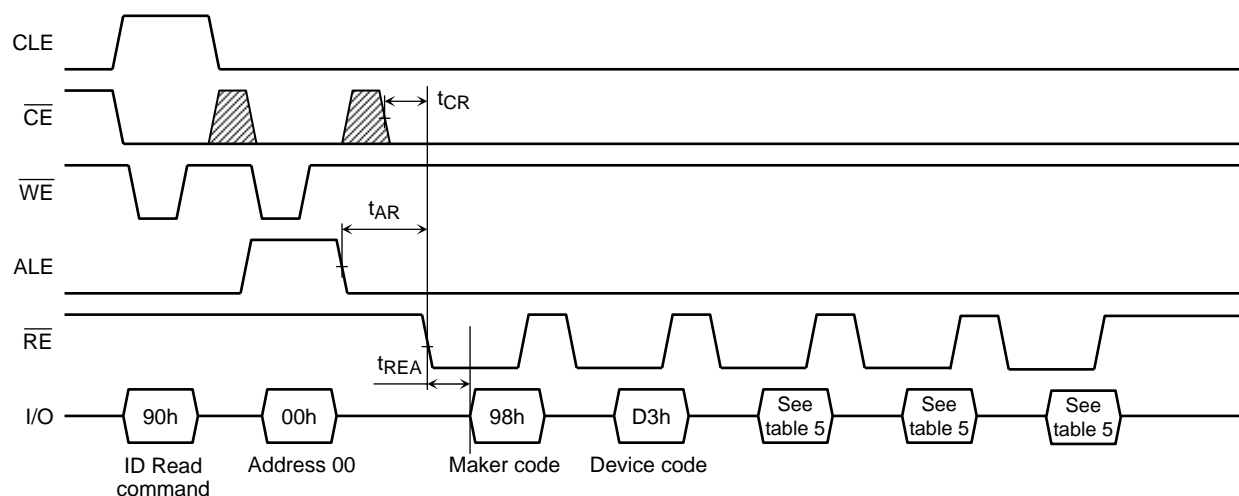


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	0	1	0	0	1	1	D3h
3rd Data	Chip Number, Cell Type	—	—	—	—	—	—	—	—	See table
4th Data	Page Size, Block Size	—	—	—	—	—	—	—	—	See table
5th Data	Plane Number	—	—	—	—	—	—	—	—	See table

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 level cell					0	0		
	4 level cell					0	1		
	8 level cell					1	0		
	16 level cell					1	1		

4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	2 KB							0	0
	4 KB							0	1
	8 KB							1	0
	Reserved							1	1
Block Size (without redundant area)	128 KB	0		0	0				
	256 KB	0		0	1				
	512 KB	0		1	0				
	1 MB	0		1	1				
	Reserved	1		0 or 1	0 or 1				

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using  $\overline{RE}$  after a "70h" command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program Block Erase	Cache Program	Read Cache Read
I/O1	Chip Status1 Pass: 0      Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O2	Chip Status 2 Pass: 0      Fail: 1	Invalid	Pass/Fail	Invalid
I/O3	Not Used	0	0	0
I/O4	Not Used	0	0	0
I/O5	Not Used	0	0	0
I/O6	Page Buffer Ready/Busy Ready: 1      Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Data Cache Ready/Busy Ready: 1      Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O8	Write Protect Not Protected :1    Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O1 and I/O2 is only valid during a Program/Erase operation when the device is in the Ready state.

**Chip Status 1:**

During a Auto Page Program or Auto Block Erase operation this bit indicates the pass/fail result.

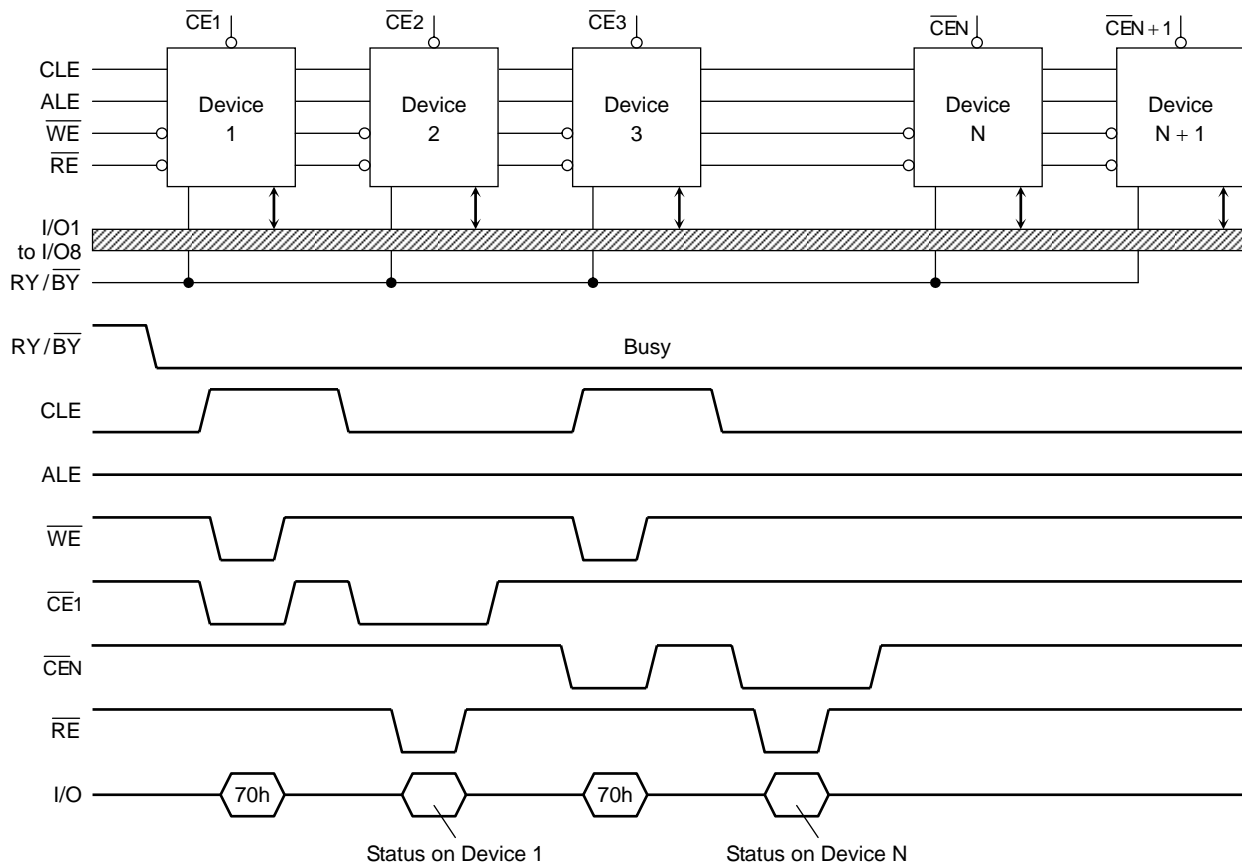
During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is only valid when I/O6 shows the Ready state.

**Chip Status 2:**

This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O7 shows the Ready State.

The status output on the I/O6 is the same as that of I/O7 if the command input just before the 70h is not 15h or 31h.

An application example with multiple devices is shown in the figure below.



System Design Note: If the  $\overline{RY}/\overline{BY}$  pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

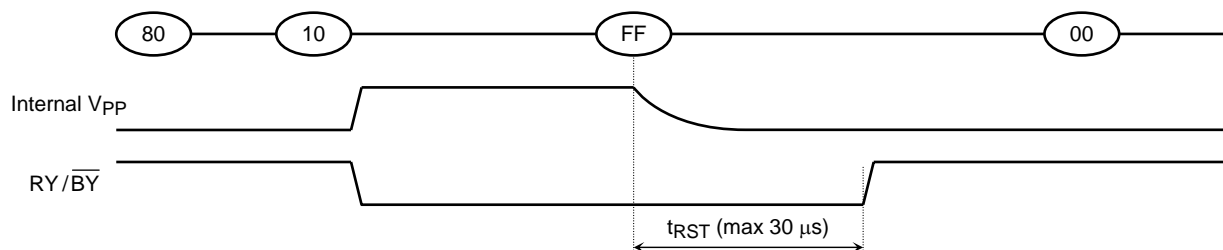
## Reset

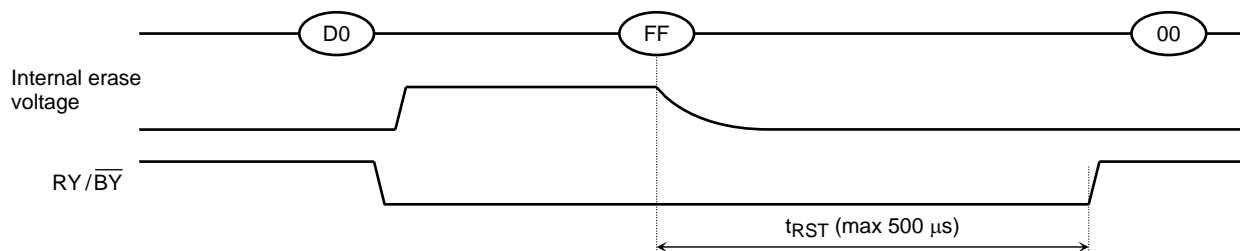
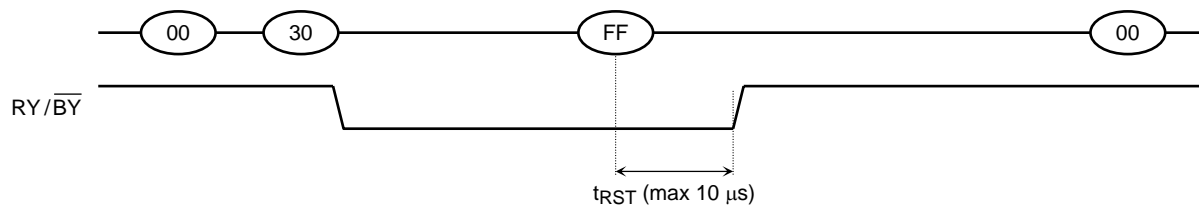
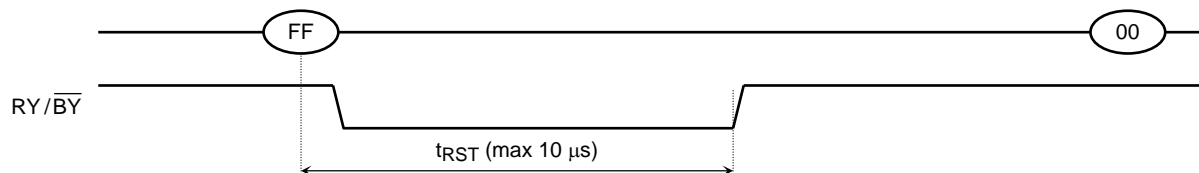
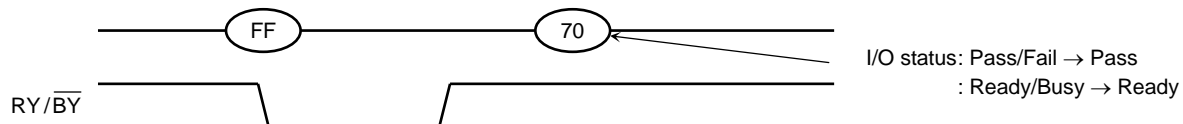
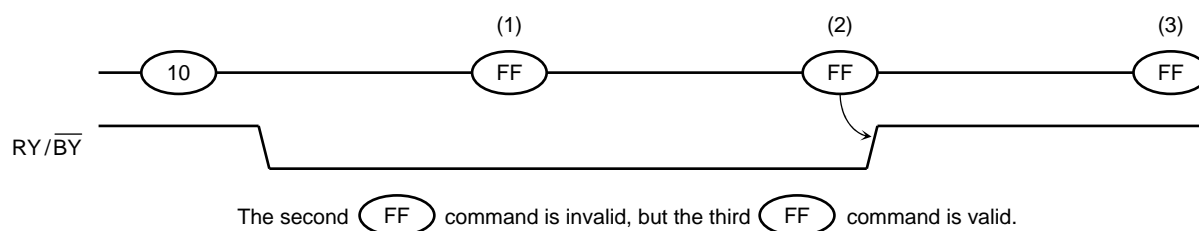
The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input.

The response to a "FFh" Reset command input during the various device operations is as follows:

### When a Reset (FFh) command is input during programming



When a Reset (FFh) command is input during erasingWhen a Reset (FFh) command is input during Read operationWhen a Reset (FFh) command is input during ReadyWhen a Status Read command (70h) is input after a ResetWhen two or more Reset commands are input in succession



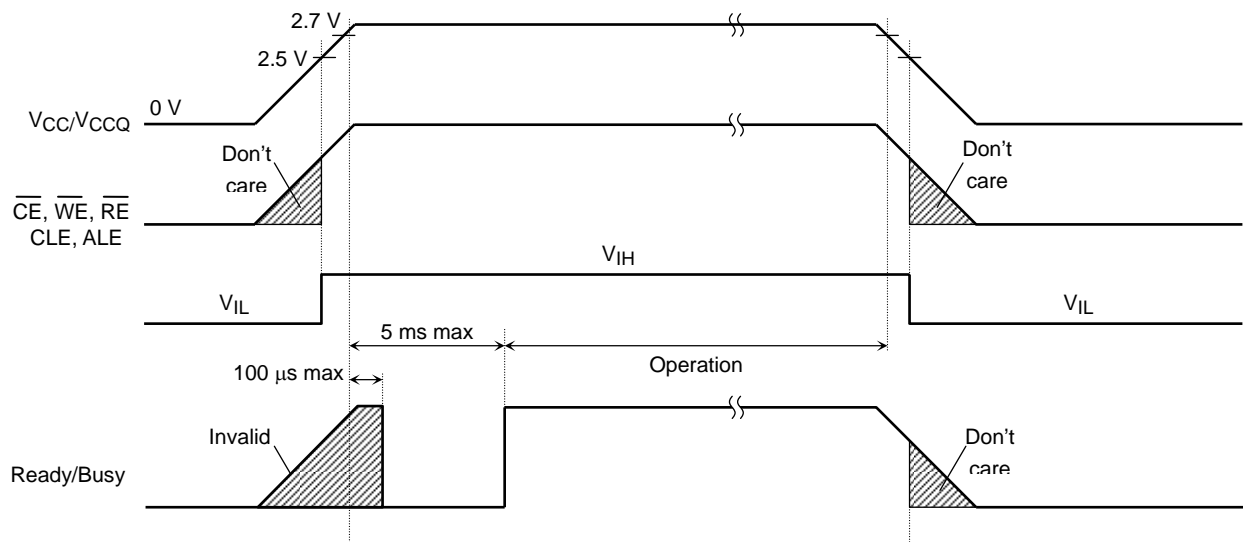
## APPLICATION NOTES AND COMMENTS

### (1) Power-on/off sequence:

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

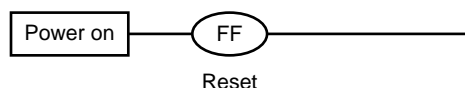
The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

The  $\overline{WP}$  signal is useful for protecting against data corruption at power-on/off.



### (2) Power-on Reset

The device goes into automatic self initialization during power on if PSL is tied either to GND or NU. During the initialization process, the device consumes a maximum current of 30 mA ( $I_{CC00}$ ). If PSL is tied to VCC, the device will not complete its self initialization during power on and will not consume  $I_{CC00}$ , and completes the initialization process with the first Reset command input after power on. During the first FFh reset Busy period, the device consumes a maximum current of 30 mA ( $I_{CC00}$ ). In either case (PSL = GND/NU or VCC), the following sequence is necessary because some input signals may not be stable at power-on.



### (3) Prohibition of unspecified commands

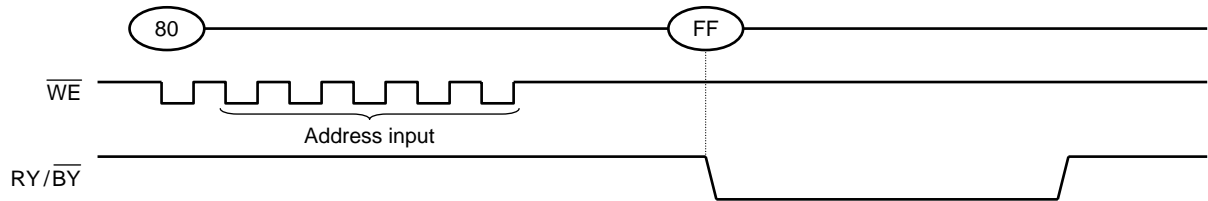
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

### (4) Restriction of commands while in the Busy state

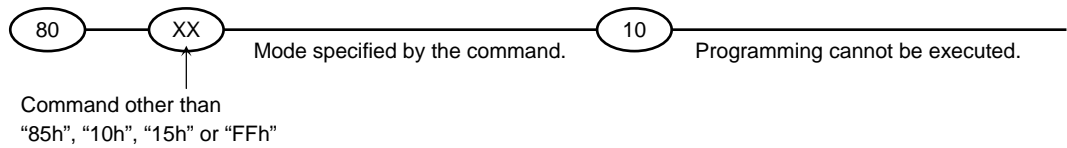
During the Busy state, do not input any command except 70h(71h) and FFh.

(5) Acceptable commands after Serial Input command "80h"

Once the Serial Input command "80h" has been input, do not input any command other than the Column Address Change in Serial Data Input command "85h", Auto Program command "10h", Auto Program with Data Cache Command "15h", or the Reset command "FFh".



If a command other than "85h", "10h", "15h" or "FFh" is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

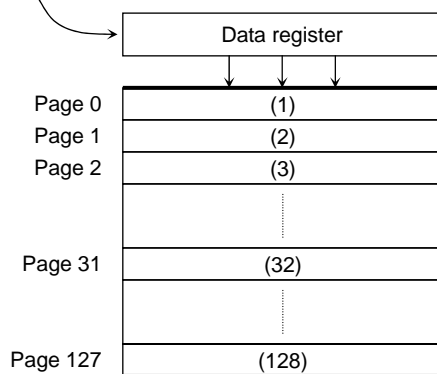


(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

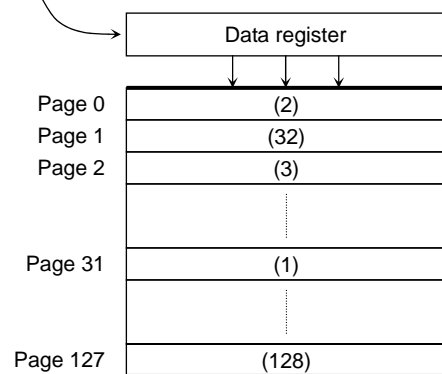
From the LSB page to MSB page

DATA IN: Data (1) → Data (128)

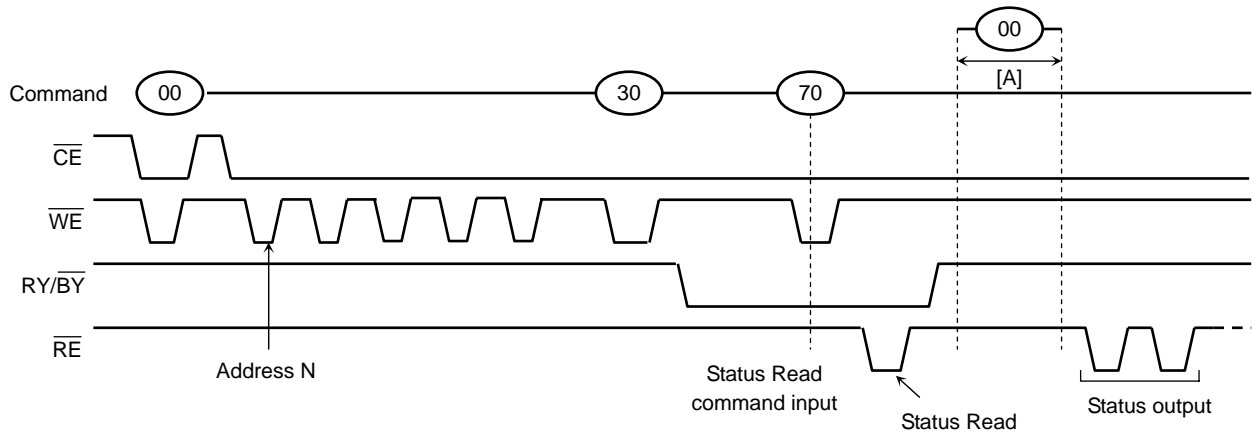


Ex.) Random page program (Prohibition)

DATA IN: Data (1) → Data (128)

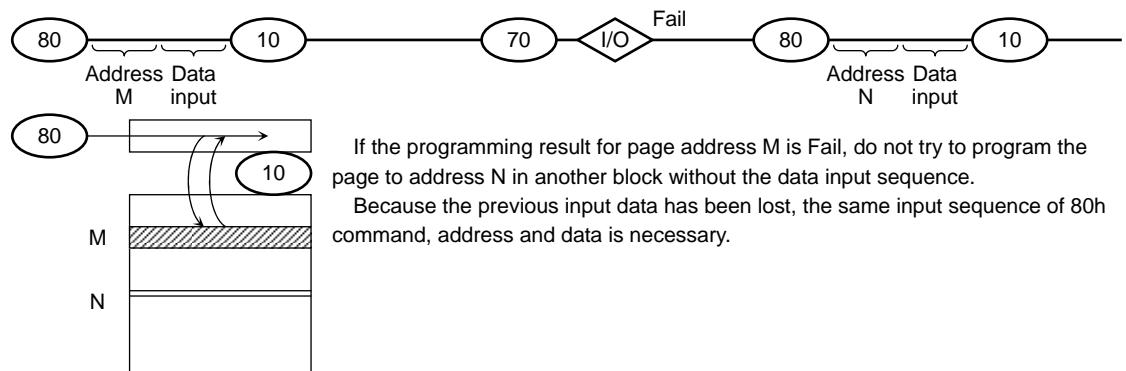


## (7) Status Read during a Read operation



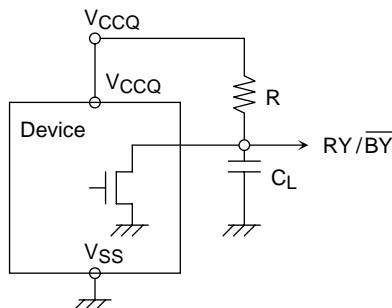
The device status can be read out by inputting the Status Read command “70h” in Read mode. Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode unless the Read command “00h” is input during [A]. If the Read command “00h” is input during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

## (8) Auto programming failure

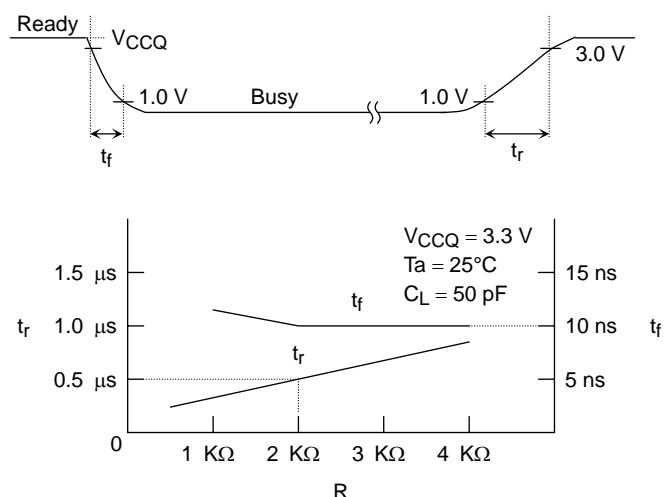


## (9) RY/BY : termination for the Ready/Busy pin (RY/BY)

A pull-up resistor needs to be used for termination because the RY/BY buffer consists of an open drain circuit.

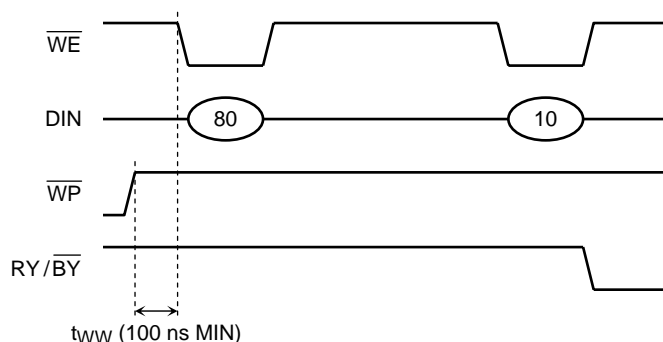
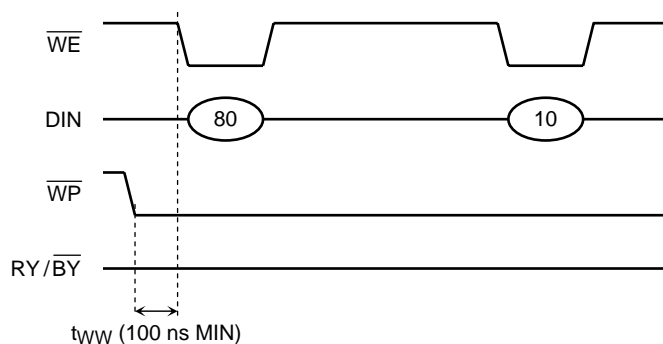
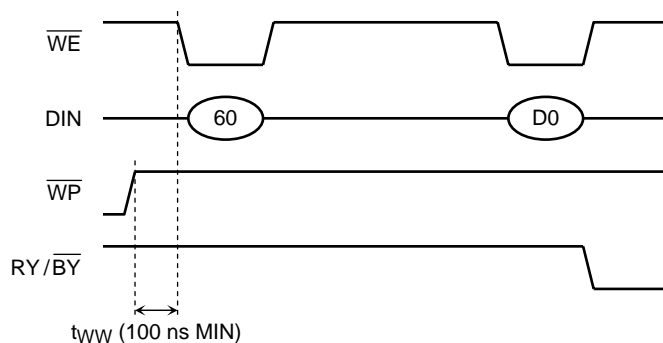
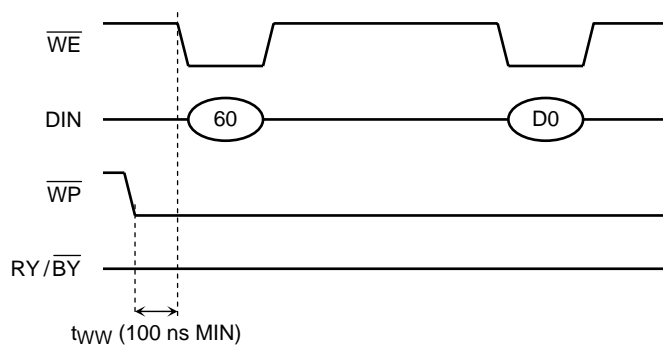


This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.



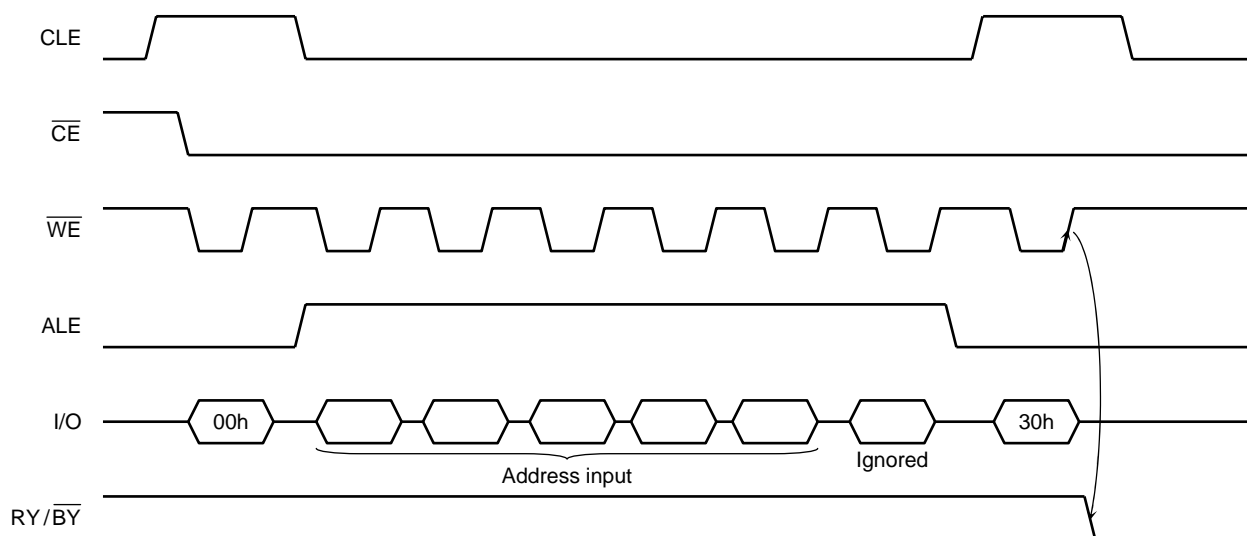
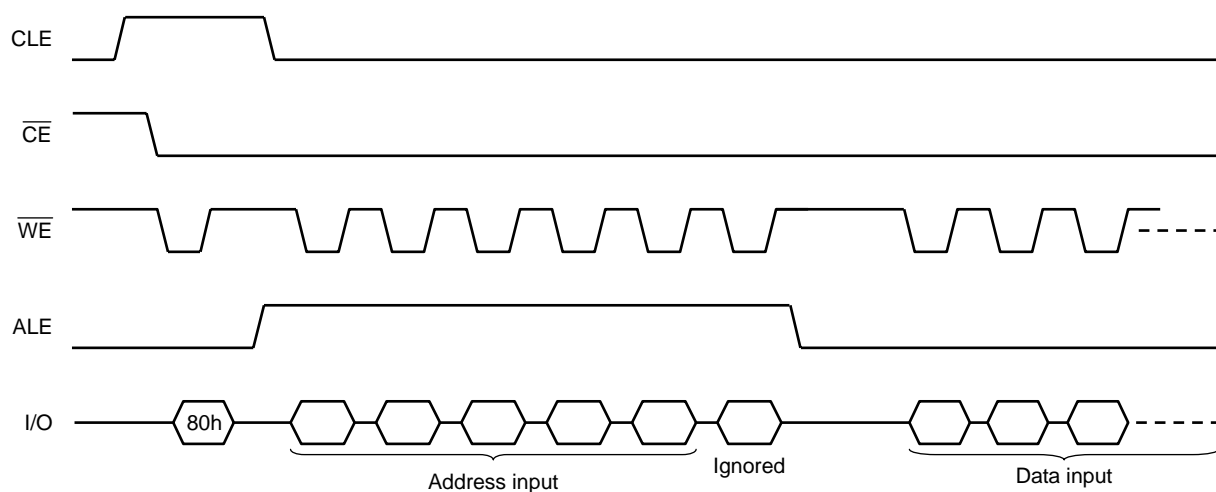
(10) Note regarding the  $\overline{WP}$  signal

The Erase and Program operations are automatically reset when  $\overline{WP}$  goes Low. The operations are enabled and disabled as follows:

Enable ProgrammingDisable ProgrammingEnable ErasingDisable Erasing

## (11) When six address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip.

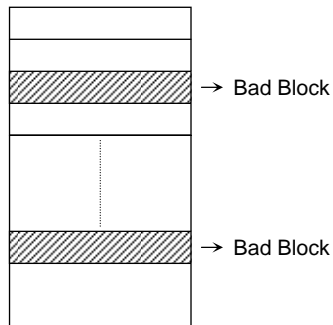
Read operationProgram operation

## (12) Several programming cycles on the same page (Partial Page Program)

This device does not support partial page programming.

## (13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



At the time of shipment, the bad block information is marked on each bad block. Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

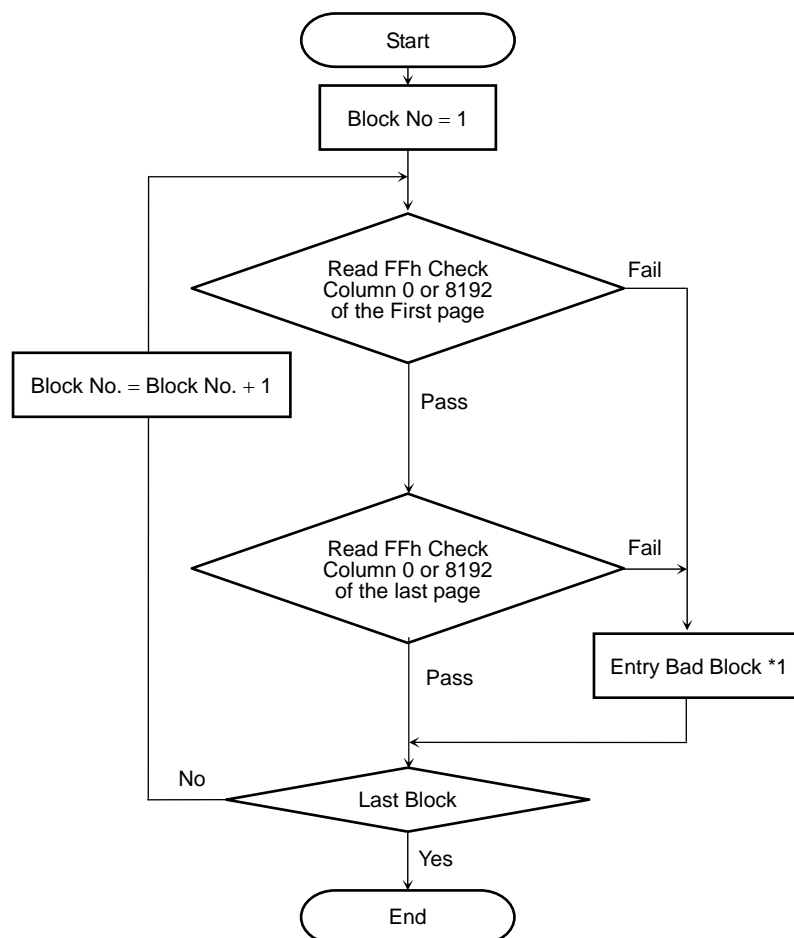
A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	984	—	1028	Block

### Bad Block Test Flow

Regarding invalid blocks, bad block mark is in either the 1st or the last page.



\*1: No erase operation is allowed to detected bad blocks

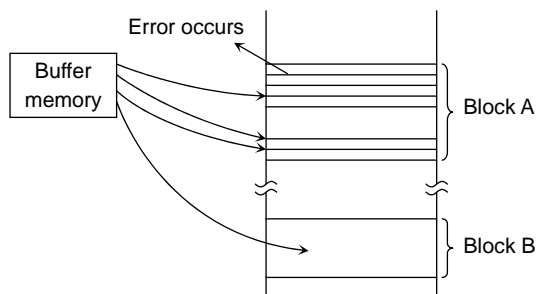
## (14) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Random Bit	Programming Failure "1 to 0"	ECC

- ECC: Error Correction Code. 24 bit correction per 1KBytes is necessary.
- Block Replacement

Program

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A ( by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

- (15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.
- (16) If FF reset command is input before completion of write operation to page B, it may cause damage to data not only to the programmed page, but also to the adjacent page A. Regarding page A and B, please see Page 33.

## (17) Reliability Guidance

This reliability guidance is intended to notify some guidance related to using MLC NAND flash with 24bit ECC for each 1024 bytes. For detailed reliability data, please refer to TOSHIBA's reliability note. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

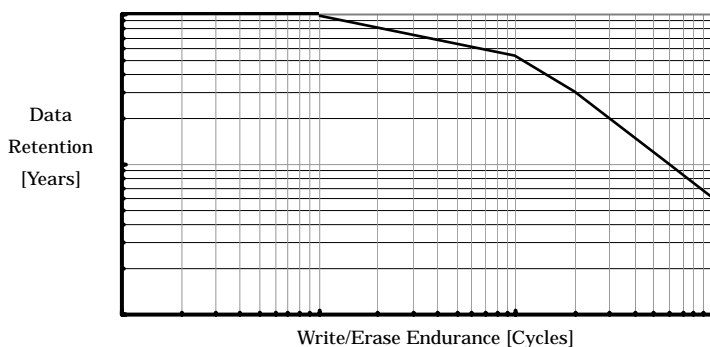
- **Write/Erase Endurance**

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

- **Data Retention**

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.

Here is the combined characteristics image of Write/Erase Endurance and Data Retention.



- **Read Disturb**

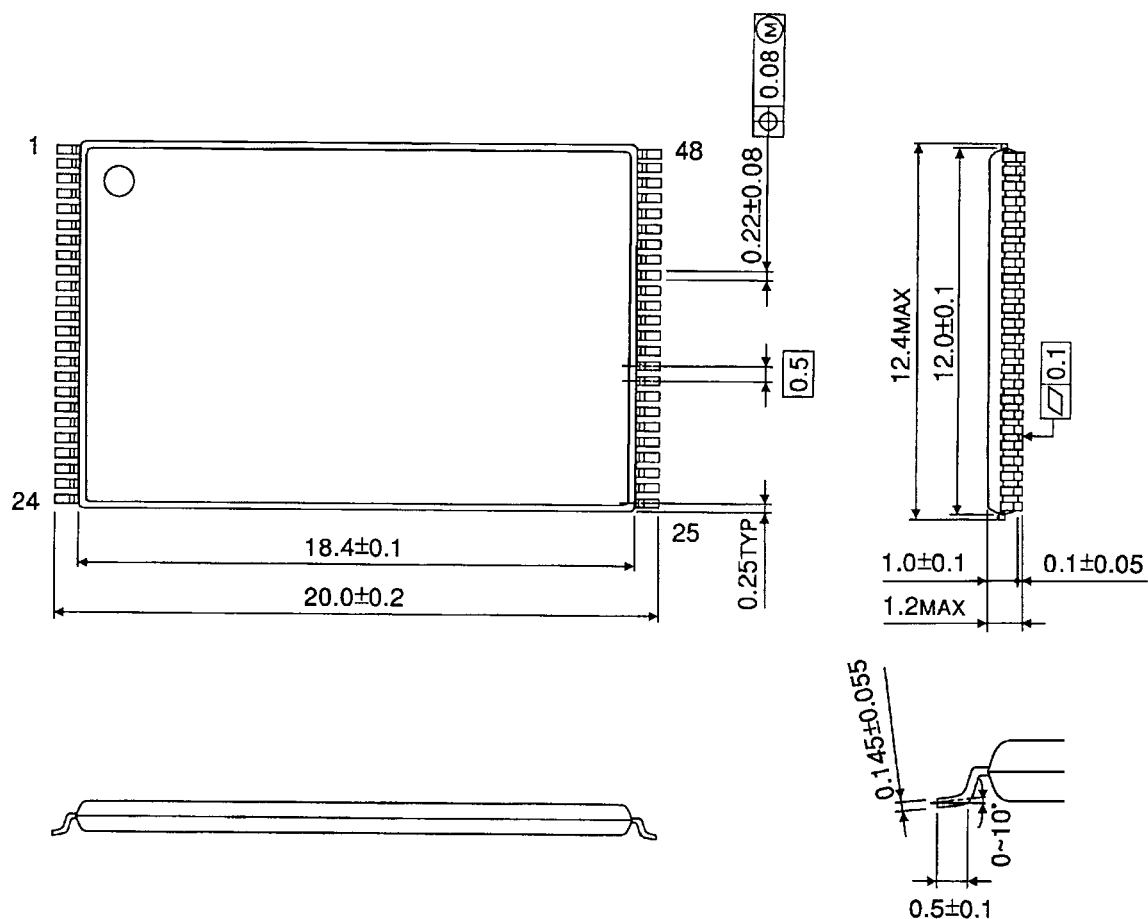
A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.



# Package Dimensions

TSOP I 48-P-1220-0.50

Unit : mm



Weight: 0.53 g (typ.)

**Revision History**

Date	Rev.	Description
2008-10-07	1.00	Original version
2009-1-21	1.01	ICCS 50uA    100uA

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060915EBA\_R6

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