

TENTATIVE

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

32 MBIT (4 M × 8 BITS) CMOS NAND E²PROMDESCRIPTION

The TC5832FT device is a single 5.0-volt 33 M (34,603,008) bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 528 byte × 16 pages × 512 blocks. The device has a 528-byte, static register which allows the program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (8 K bytes + 256 bytes: 528 bytes × 16 pages).

The TC5832FT is a serial type of memory device which utilizes the I/O pins for both address and data input/output as well as command inputs. The Erase and Program operations are automatically executed, making the device most suitable for applications such as solid state file storage, voice recording, image file memory for still cameras and other systems which require high-density, and non-volatile memory data storage.

FEATURES

- Organization
 - Memory cell array 528 × 8 K × 8
 - Register 528 × 8
 - Page size 528 bytes
 - Block size (8 K + 256) bytes
- Mode
 - Read, Reset, Auto Page Program
 - Auto Block Erase, Suspend/Resume
 - Status Read
- Mode control
 - Serial input/output
 - Command control
- Power supply
 - V_{CC} = 5.0 V ± 0.5 V
- Access time
 - Cell array - Register 10 μs max
 - Serial Read Cycle 50 ns min
- Operating current
 - Read (50ns cycle) 15 mA typ
 - Program (ave.) 40 mA typ
 - Erase (ave.) 20 mA typ
 - Standby 100 μA
- Package
 - 400mil TSOP Type II
 - TC5832FT : TSOP II 44/40 - P - 400 - 0.80B
 - (Weight : 0.48 g Typ.)

PIN ASSIGNMENT (TOP VIEW)

TC5832FT			
V _{SS}	1	44	V _{CC}
CLE	2	43	$\overline{\text{CE}}$
ALE	3	42	$\overline{\text{RE}}$
WE	4	41	R/ $\overline{\text{B}}$
$\overline{\text{WP}}$	5	40	OP
NC	6	39	NC
NC	7	38	NC
NC	8	37	NC
NC	9	36	NC
NC	10	35	NC
	11	34	
	12	33	
NC	13	32	NC
NC	14	31	NC
NC	15	30	NC
NC	16	29	NC
NC	17	28	NC
I/O 1	18	27	I/O 8
I/O 2	19	26	I/O 7
I/O 3	20	25	I/O 6
I/O 4	21	24	I/O 5
V _{SS}	22	23	V _{CC}

PIN NAMES

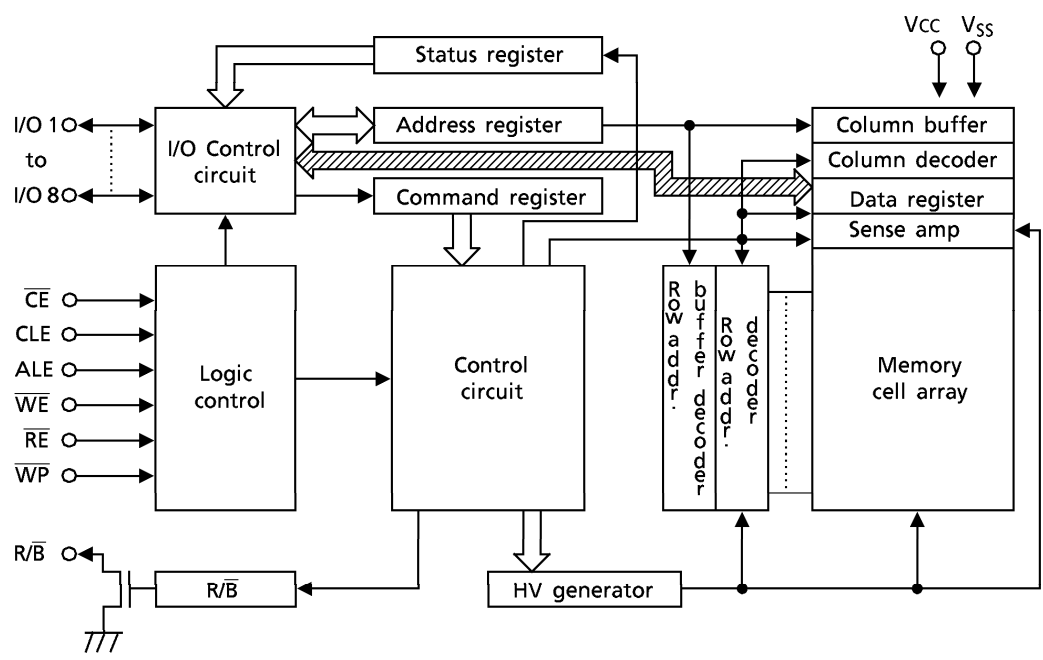
I/O 1 to 8	I/O port
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RE}}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{\text{WP}}$	Write Protect
R/ $\overline{\text{B}}$	Ready/Busy
OP	Option Pin
V _{CC}	Power Supply
V _{SS}	Ground

OP : GND Input : 528 Byte / Page Operation
 V_{CC} Input : 512 Byte / Page Operation

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{CC}	Power supply	- 0.6 to 7.0	V
V _{IN}	Input Voltage	- 0.6 to 7.0	V
V _{I/O}	Input / Output Voltage	- 0.6 V to V _{CC} + 0.5 V (≦ 7.0 V)	V
P _D	Power Dissipation	0.5	W
T _{SOLDER}	Soldering Temperature (10 s)	260	°C
T _{STG}	Storage Temperature	- 55 to 150	°C
T _{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
C _{IN}	Input	V _{IN} = 0 V	-	5	10	pF
C _{OUT}	Output	V _{OUT} = 0 V	-	5	10	pF

* This parameter is periodically sampled and is not tested for every component.

VALID BLOCK (1)

SYMBOL	PARAMETER	TC5832FT			UNIT
		MIN	TYP	MAX	
N _{VB}	Valid Block Number	502	508	512	Blocks

(1) The TC5832FT occasionally contains unusable blocks. Refer to Application Note (17) toward the end of this document.

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{CC}	Power Supply	4.5	5	5.5	V
V _{IH}	High Level Input Voltage	2.2	–	V _{CC} + 0.5	V
V _{IL}	Low Level Input Voltage	– 0.3*	–	0.8	V

* – 2 V (pulse width ≤ 20 ns)

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{CC} = 5.0 V ± 0.5 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I _{IL}	Input Leak Current	V _{IN} = 0 V to V _{CC}	–	–	± 10	μA
I _{LO}	Output Leak Current	V _{OUT} = 0.4 V to V _{CC}	–	–	± 10	μA
I _{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V _{IL} , I _{out} = 0 mA, t _{cycle} = 50 ns	–	15	30	mA
I _{CCO3}	Operating Current (Command Input)	t _{cycle} = 50 ns	–	15	30	mA
I _{CCO4}	Operating Current (Data Input)	t _{cycle} = 50 ns	–	40	60	mA
I _{CCO5}	Operating Current (Address Input)	t _{cycle} = 50 ns	–	15	30	mA
I _{CCO7}	Programming Current	–	–	40	60	mA
I _{CCO8}	Erasing Current	–	–	20	40	mA
I _{CCS1}	Standby Current	$\overline{CE}$ = V _{IH}	–	–	1	mA
I _{CCS2}	Standby Current	$\overline{CE}$ = V _{CC} – 0.2 V	–	–	100	μA
V _{OH}	High Level Output Voltage	I _{OH} = – 400 μA	2.4	–	–	V
V _{OL}	Low Level Output Voltage	I _{OL} = 2.1 mA	–	–	0.4	V
I _{OL (R/B)}	Output Current of (R/B) Pin	V _{OL} = 0.4 V	–	8	–	mA

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = 0^\circ$ to 70°C , $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$) (1)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
t_{CLS}	CLE Set-Up Time	0	–	ns	
t_{CLH}	CLE Hold Time	10	–	ns	
t_{CS}	$\overline{CE}$ Set-Up Time	0	–	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	–	ns	
t_{WP}	Write Pulse Width	25	–	ns	
t_{ALS}	ALE Set-Up Time	0	–	ns	
t_{ALH}	ALE Hold Time	10	–	ns	
t_{DS}	Data Set-Up Time	20	–	ns	
t_{DH}	Data Hold Time	10	–	ns	
t_{WC}	Write Cycle Time	50	–	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	–	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	–	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	–	ns	
t_{RP}	Read Pulse Width	35	–	ns	
t_{RC}	Read Cycle Time	50	–	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	–	35	ns	
t_{CEH}	$\overline{CE}$ High Time for the Last Address in Serial Read Cycle	100	–	ns	(3)
t_{READ}	$\overline{RE}$ Access Time (ID Read)	–	35	ns	
t_{OH}	Data Output Hold Time	10	–	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	–	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	–	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	–	ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Falling Edge	0	–	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	–	35	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	–	45	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	–	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	–	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	–	ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (ID Read)	100	–	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	100	–	ns	
t_R	Memory Cell Array to Starting Address	–	10	μs	
t_{WB}	$\overline{WE}$ High to Busy	–	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	50	–	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)	–	200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (in Case of Interruption by $\overline{CE}$ in Read Mode)	–	600	ns	(2)
t_{RST}	Device Resetting Time (Read/Program/Erase/after Suspend Command)	–	6/10/500/5	μs	

AC TEST CONDITIONS

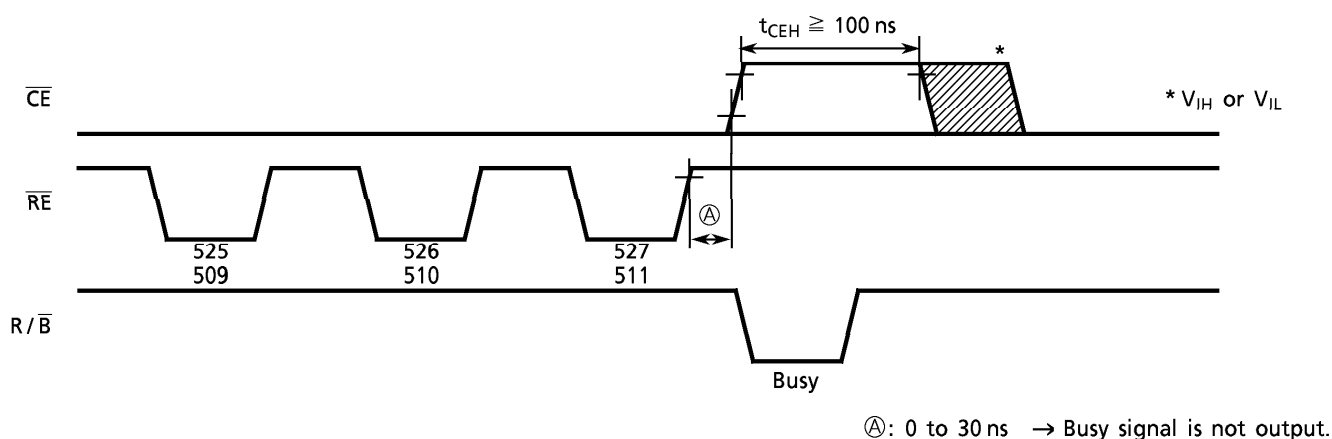
Input level : 2.4 V / 0.6 V
 Input comparison level : 2.2 V / 0.8 V
 Output data comparison level : 2.0 V / 0.8 V
 Output load : 1 TTL & C_L (100 pF)

(1) Transition time (t_T) = 5 ns

(2) The $\overline{CE}$ High to Ready time depends on the pull-up resistor tied to the $R/\overline{B}$ pin. (Refer to Application Note (10) toward the end of this document.)

(3) If the delay between $\overline{RE}$ and $\overline{CE}$ is less than 200 ns and t_{CEH} is greater than or equal to 100 ns, reading will stop.

If the $\overline{RE}$ -to- $\overline{CE}$ delay is less than 30 ns, the device will not turn to the Busy state.



PROGRAMMING AND ERASING CHARACTERISTICS ($T_a = 0^\circ$ to 70°C , $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$)

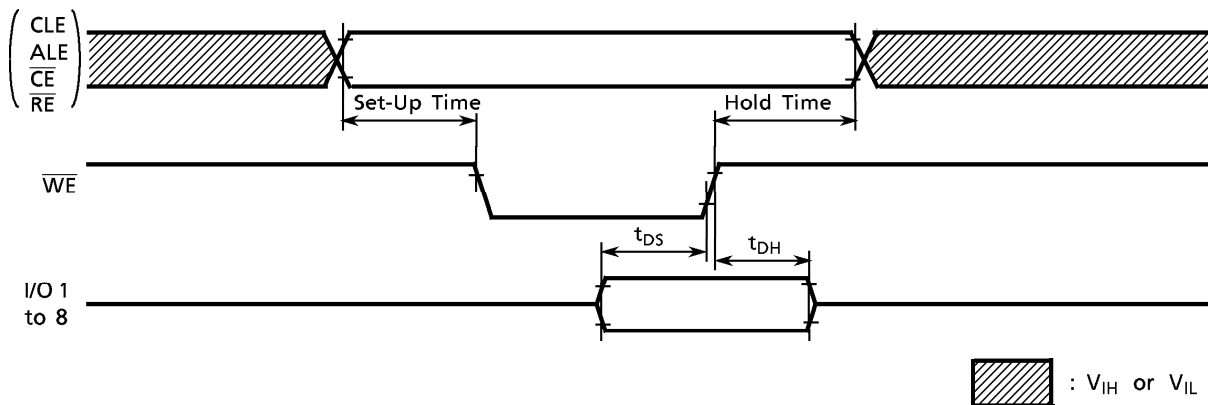
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
t_{PROG}	Average Programming Time		300	1500	μs	
N	Number of Programming Cycles on Same Page			10		(1)
t_{BERASE}	Block Erasing Time		6	50	ms	
t_{SR}	Suspend Input to Ready			0.5	ms	
P/E	Number of Program/Erase Cycles			1×10^6		(2)

(1) Refer to Application Note (15) toward the end of this document.

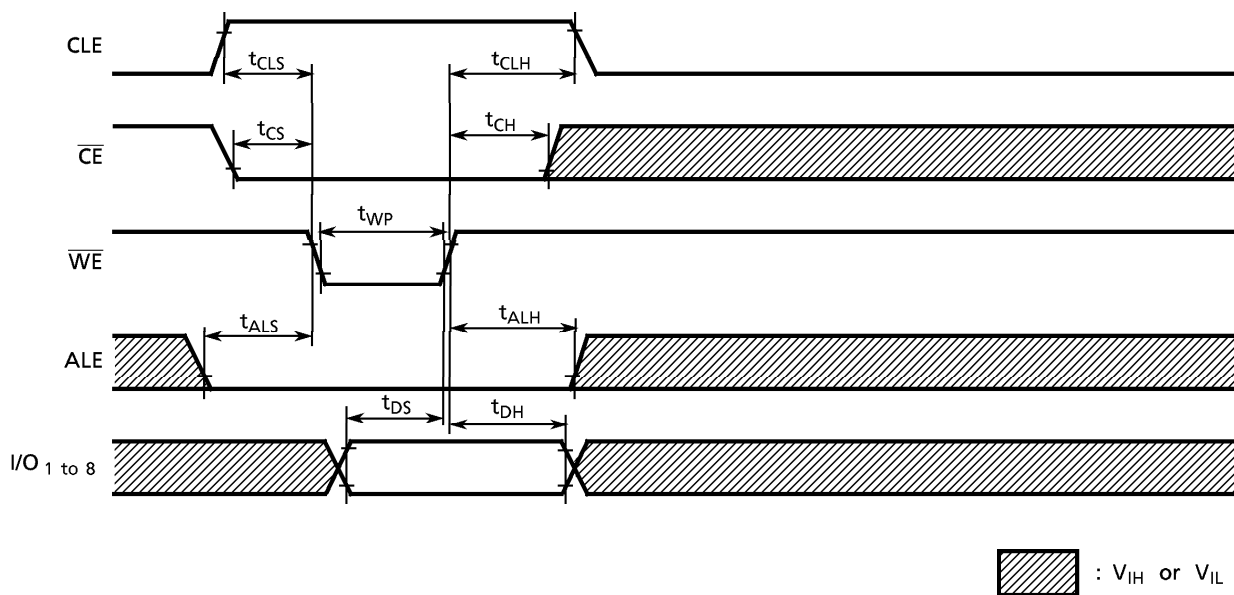
(2) Refer to Application Note (18) toward the end of this document.

TIMING DIAGRAMS

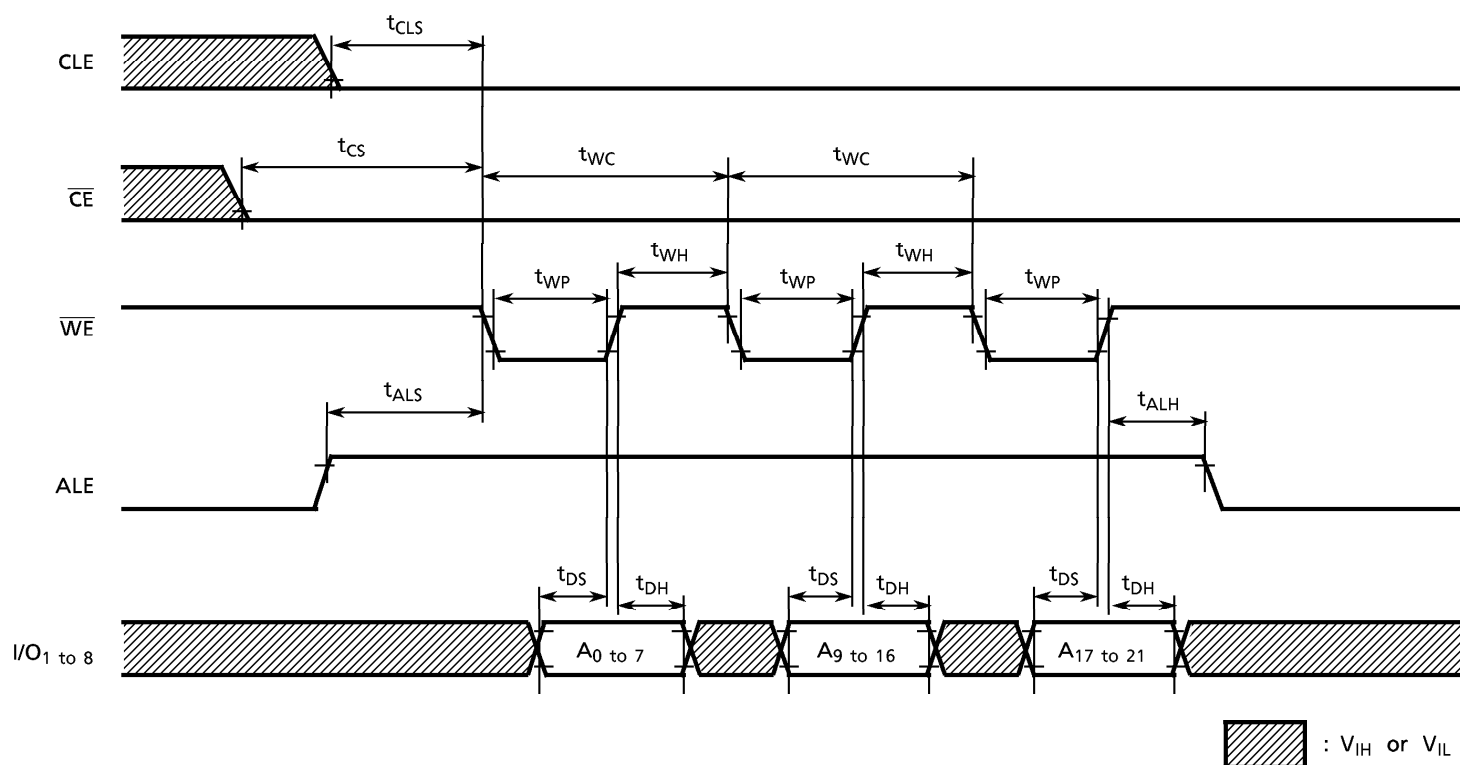
Latch Timing Diagram for Command/Address/Data



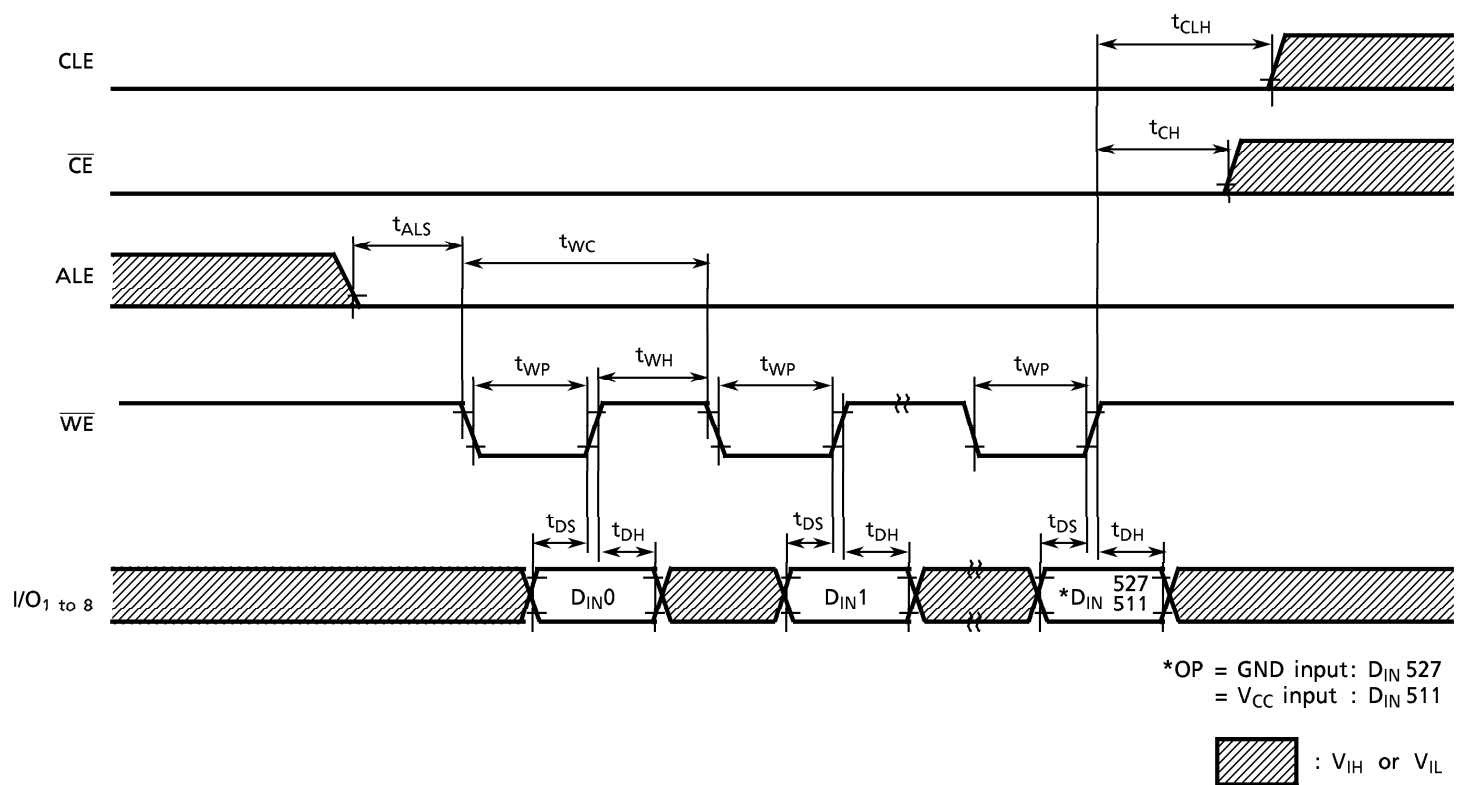
Command Input Cycle Timing Diagram



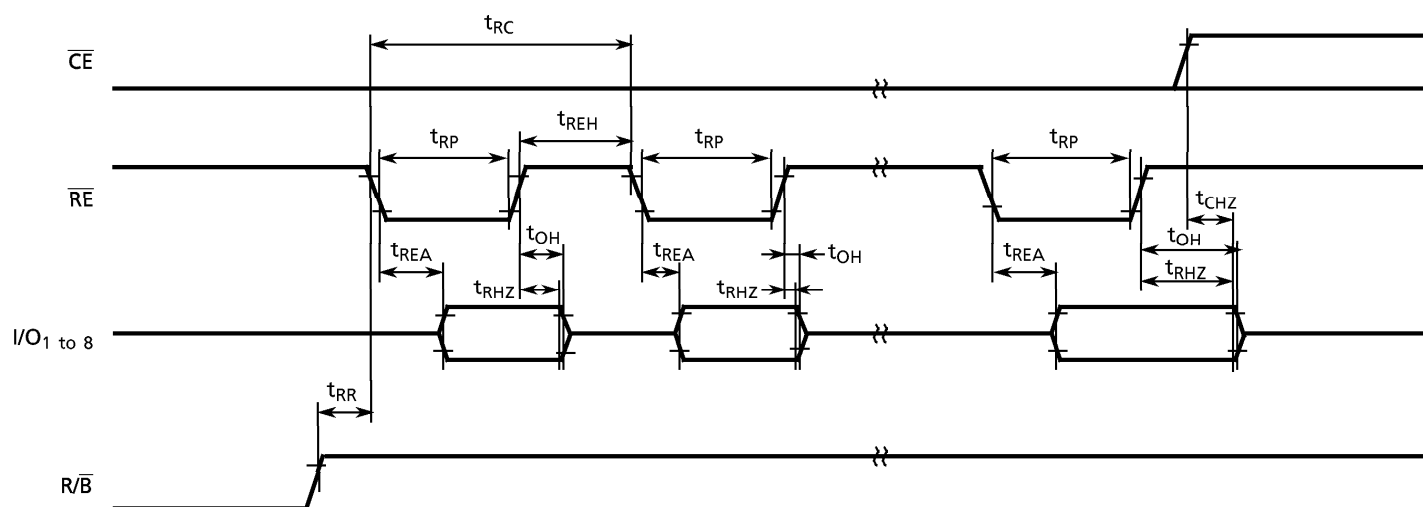
Address Input Cycle Timing Diagram



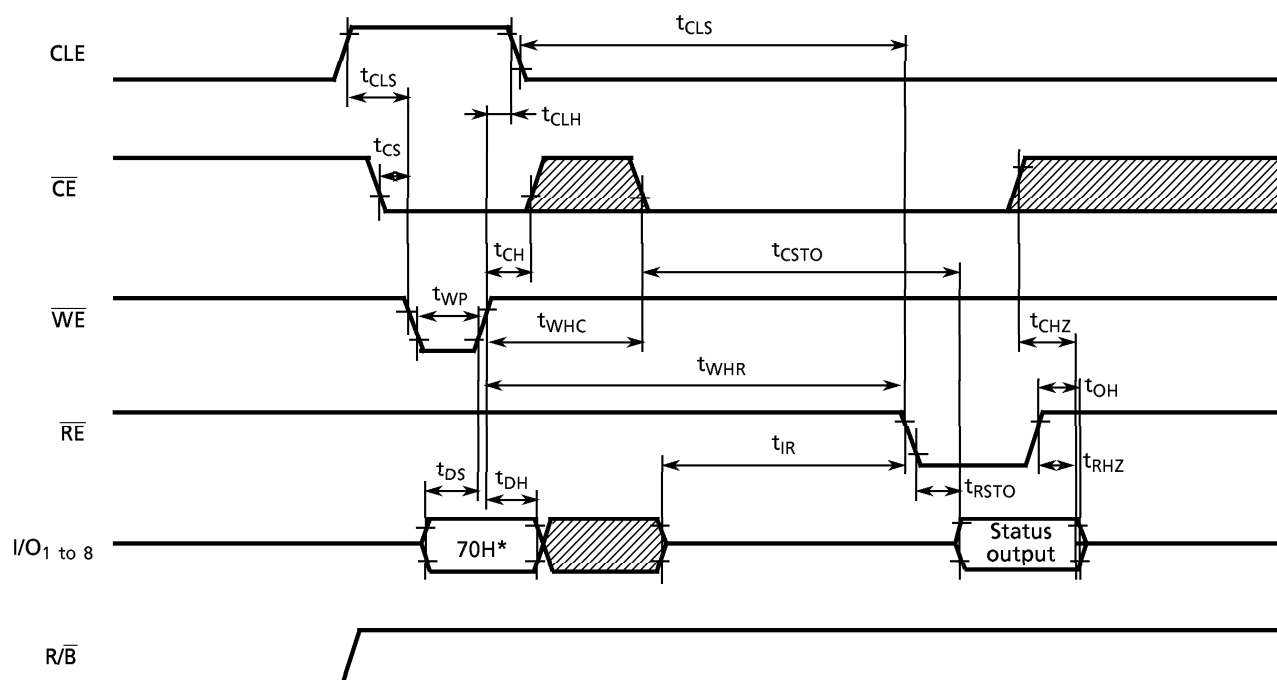
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



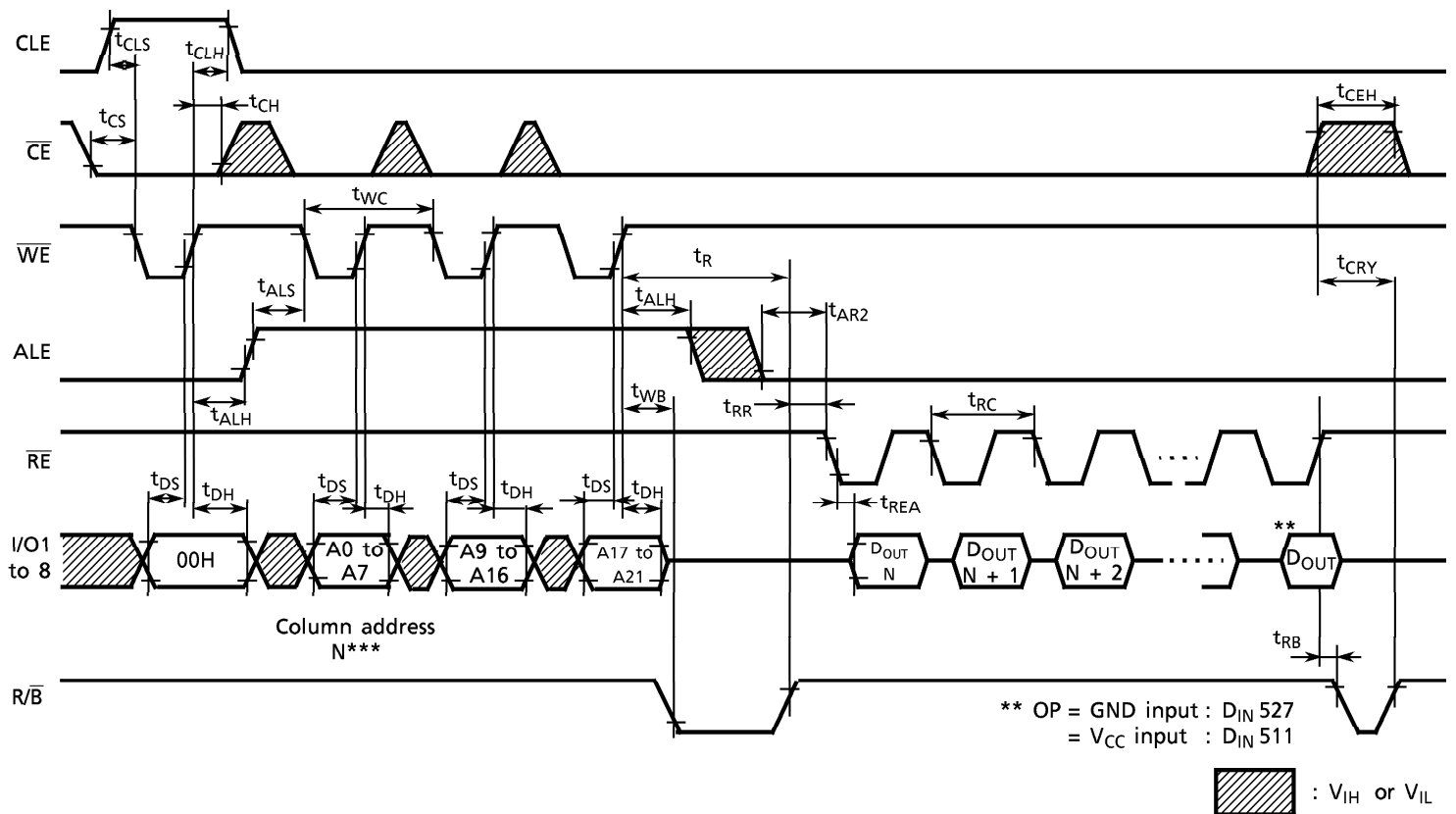
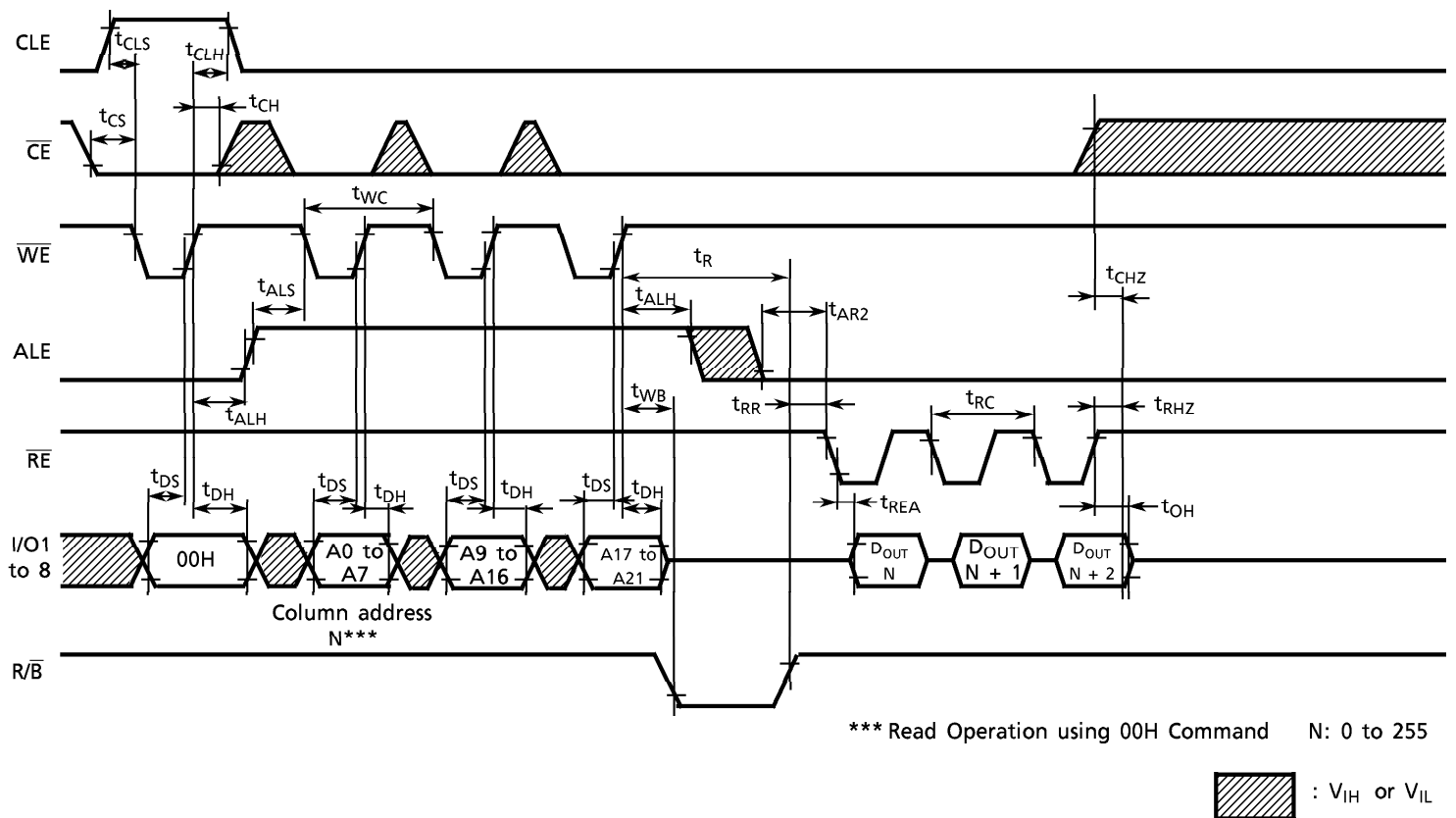
Status Read Cycle Timing Diagram



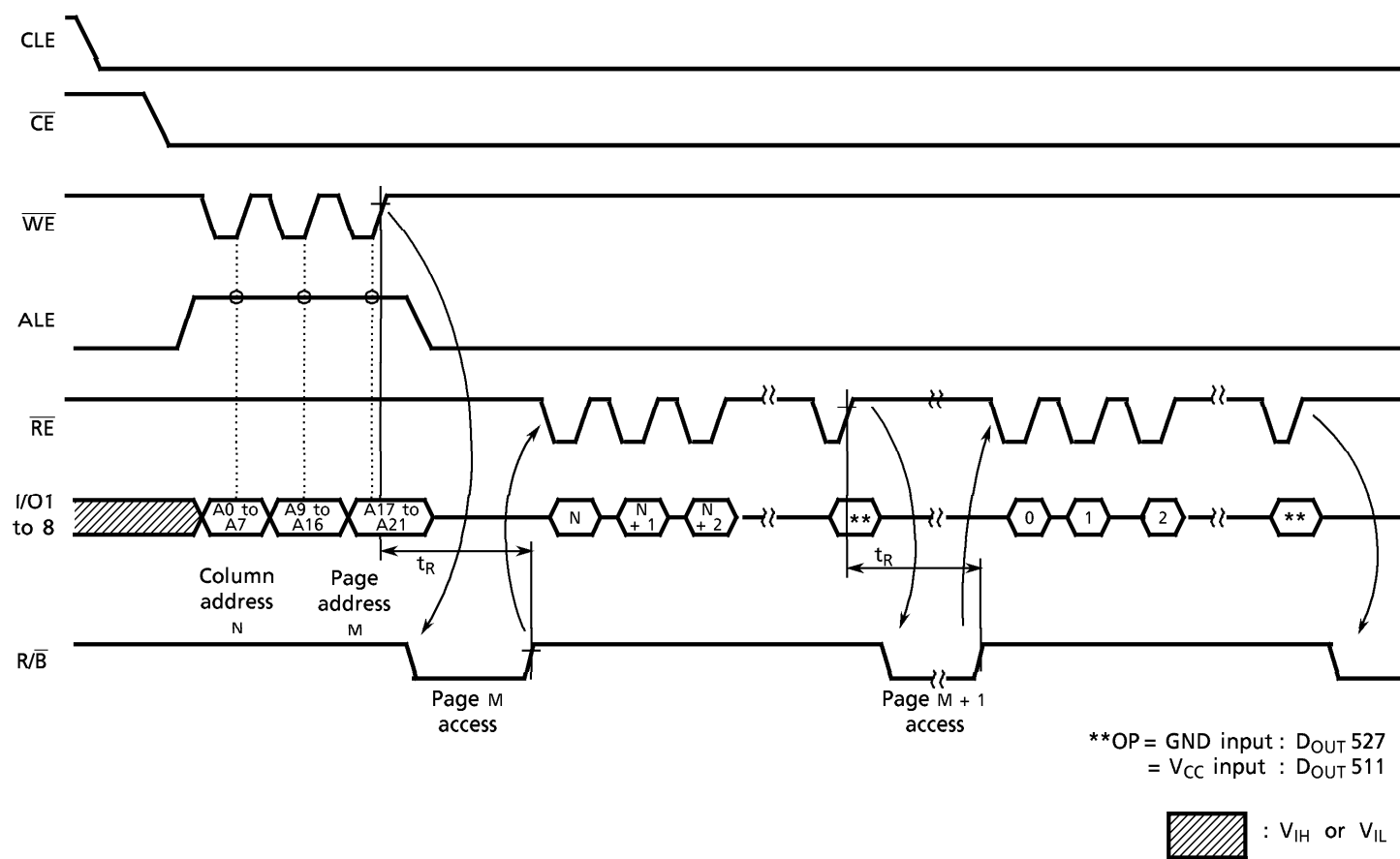
* 70H - 70 in HEX data

 : V_{IH} or V_{IL}

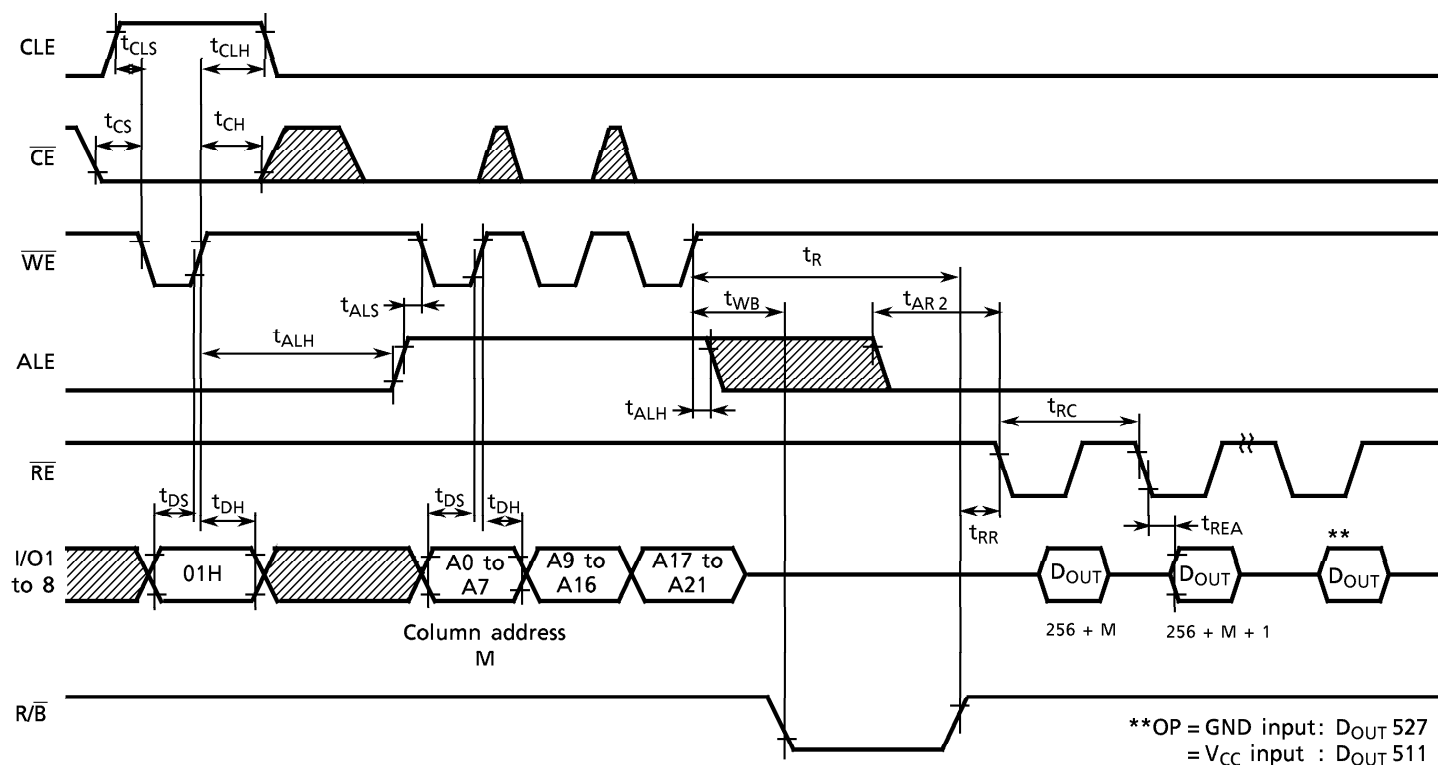
Read Cycle (1) Timing Diagram

Read Cycle (1) Timing Diagram: Interrupted by $\overline{CE}$ 

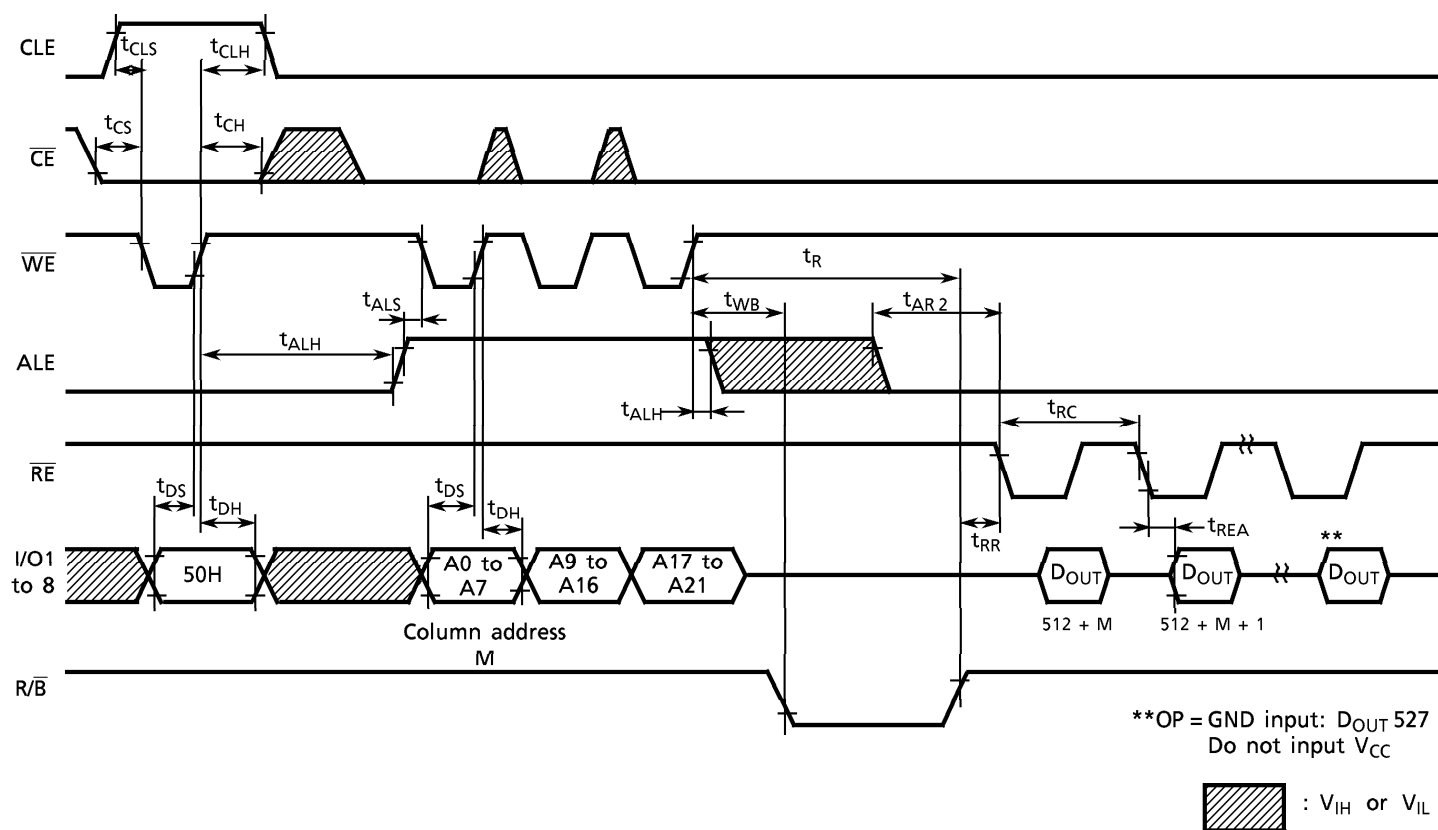
Sequential Read Timing Diagram



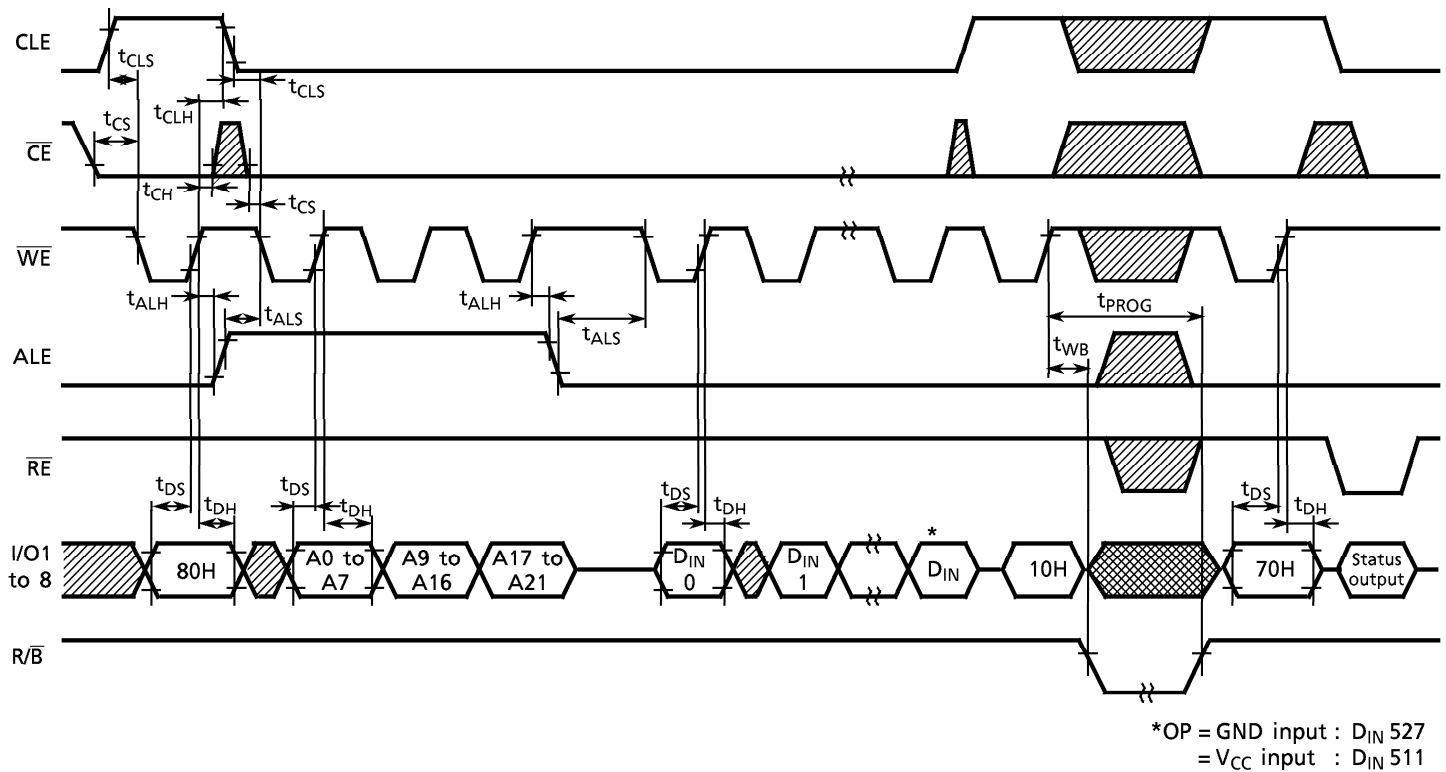
Read Cycle (2) Timing Diagram



Read Cycle (3) Timing Diagram

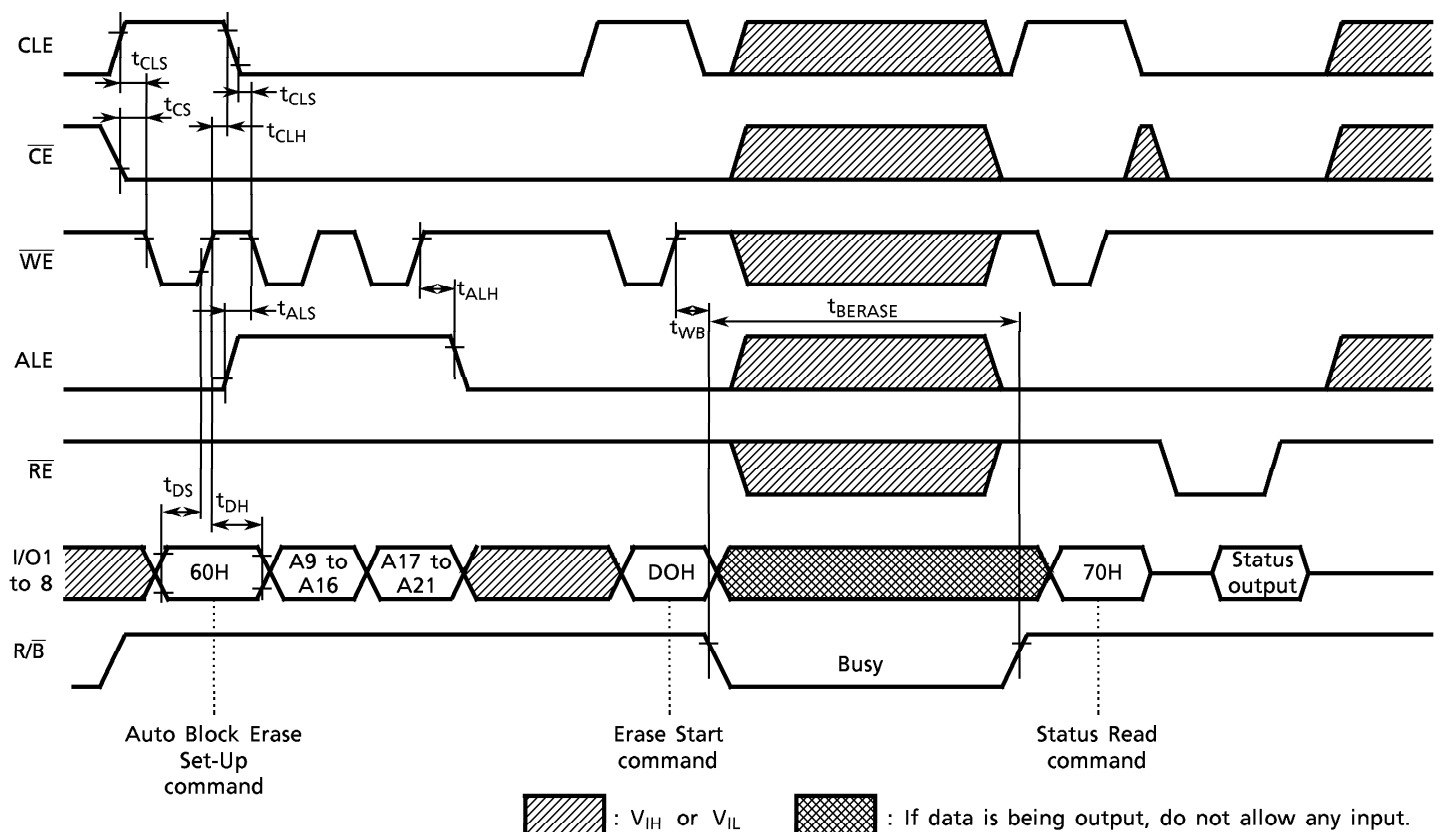


Auto Program Operation Timing Diagram


 : V_{IH} or V_{IL}

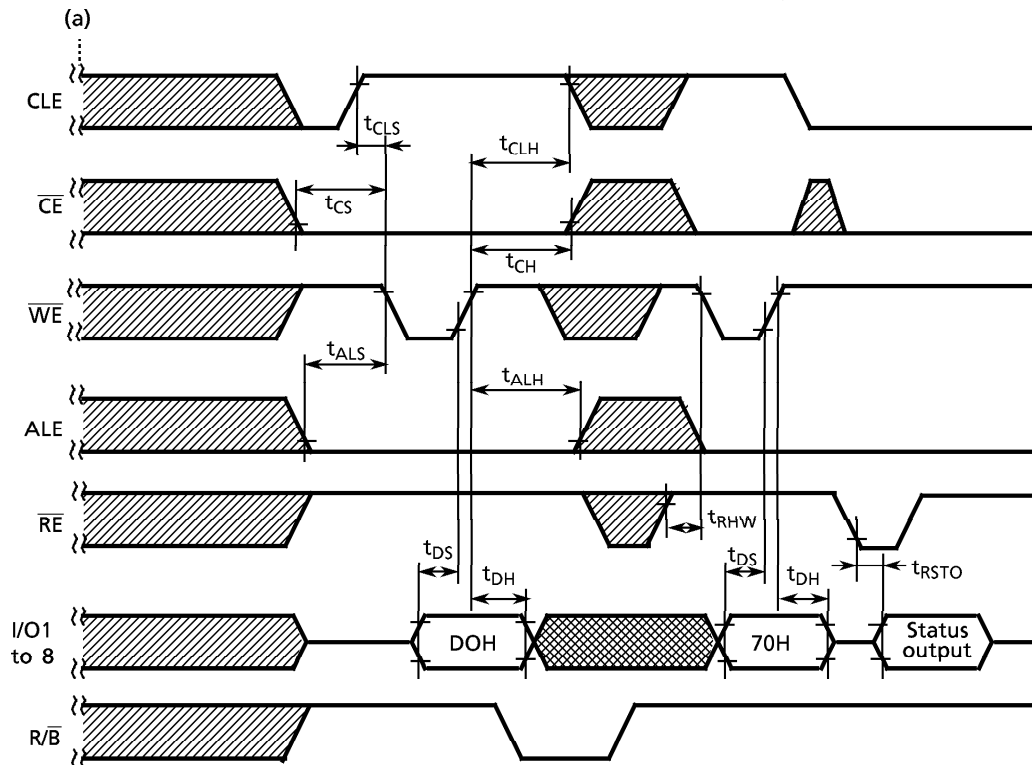
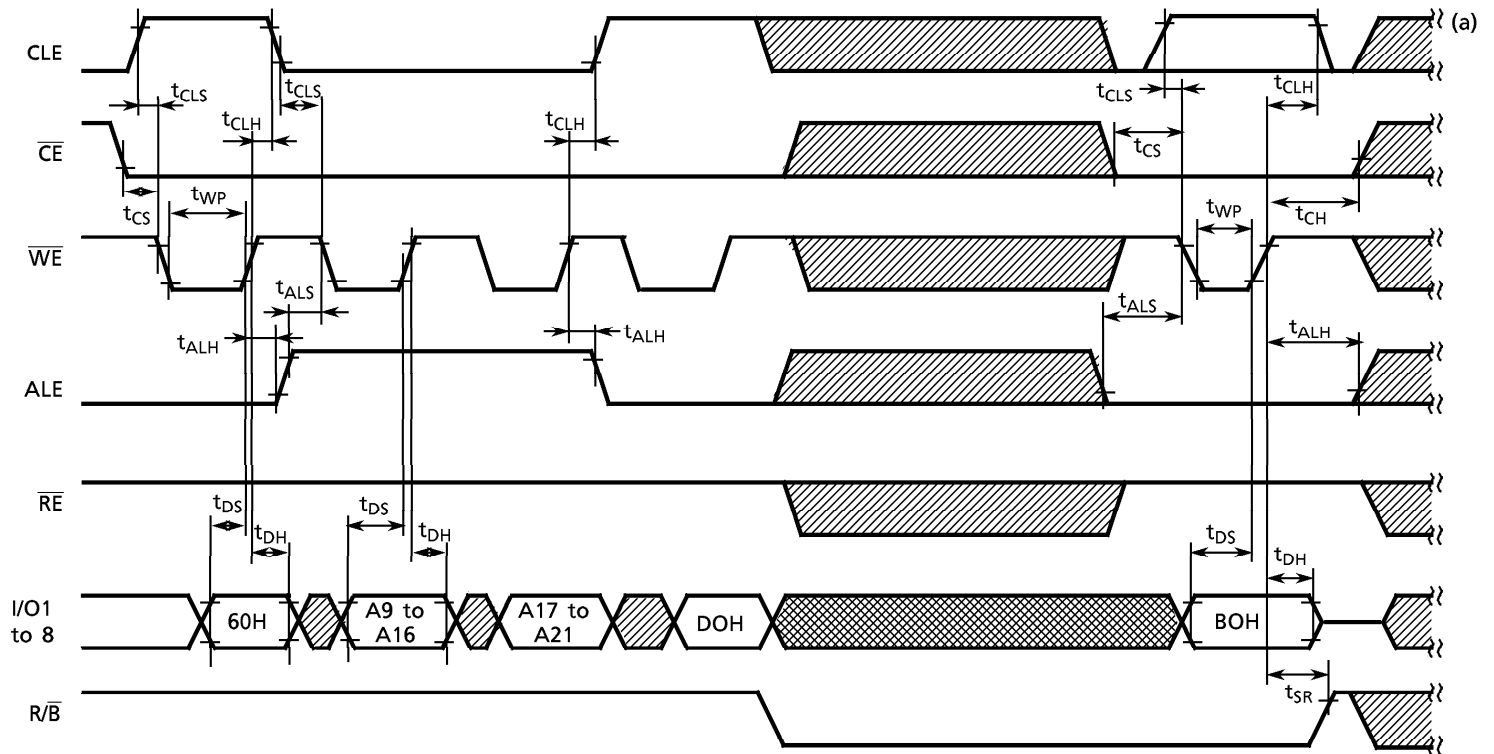
: If data is being output, do not allow any input.

Auto Block Erase Timing Diagram

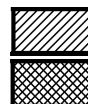

 : V_{IH} or V_{IL}

: If data is being output, do not allow any input.

Suspend/Resume Block Erase Operation Timing Diagram

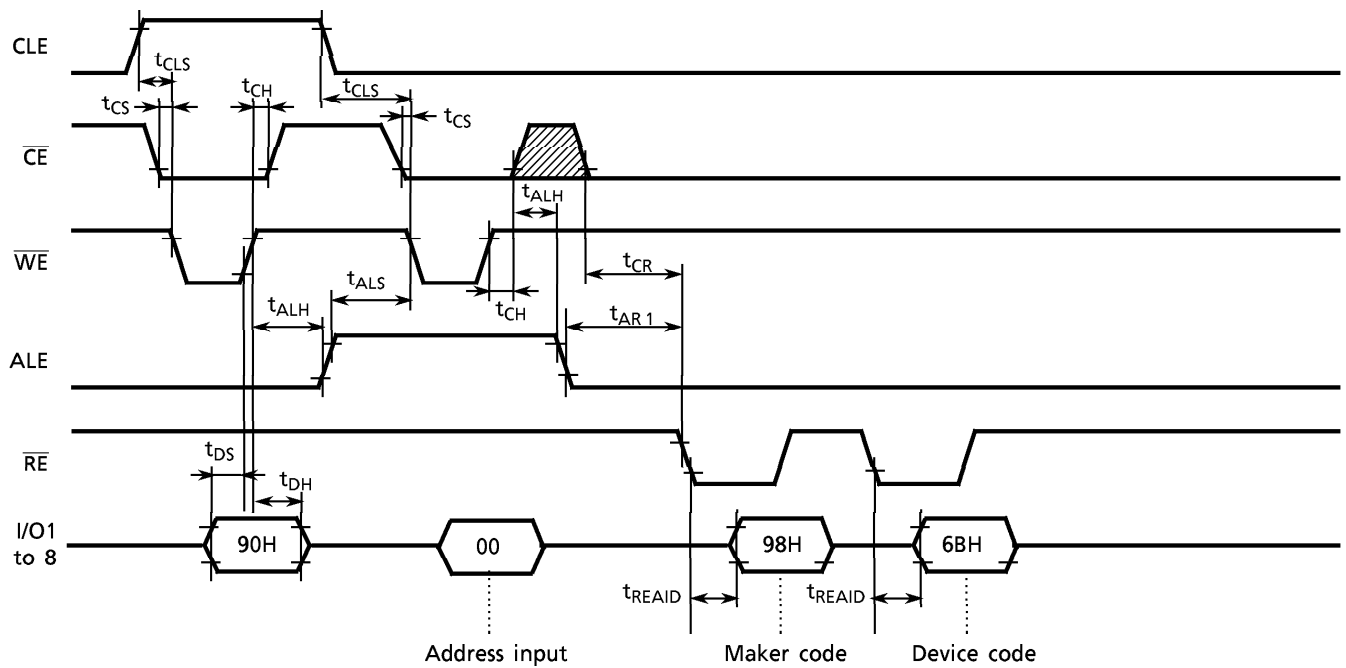


(a): Continued

: V_{IH} or V_{IL}

: If data is being output, do not allow any input.

ID Read Operation Timing Diagram



 : V_{IH} or V_{IL}

PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data register. Address information is latched on the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable: $\overline{CE}$

The device goes into a low power standby mode during a Read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in the Busy state ($R/\overline{B} = L$), such as during a Program or Erase operation, and will not go into Standby mode even if a $\overline{CE}$ high signal is input. The $\overline{CE}$ signal must stay low during the Read mode Busy state to ensure that memory signal array data is correctly transferred to the data register.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address + 1) on this falling edge.

I/O Port: I/O 1 to 8

The I/O 1 to 8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when input signals are invalid.

Ready/Busy: $R/\overline{B}$

The $R/\overline{B}$ output signal is used to indicate the operating condition of the device. The $R/\overline{B}$ signal is in the Busy state ($R/\overline{B} = L$) during the Program, Erase or Read operations and will return to Ready state ($R/\overline{B} = H$) after completion of the operation. The output buffer for this signal is an open drain.

Option Pin: OP

The OP signal is used to change the page size. The device is in 528 byte/page mode when $OP = GND$, and 512 byte/page mode when $OP = V_{CC}$.

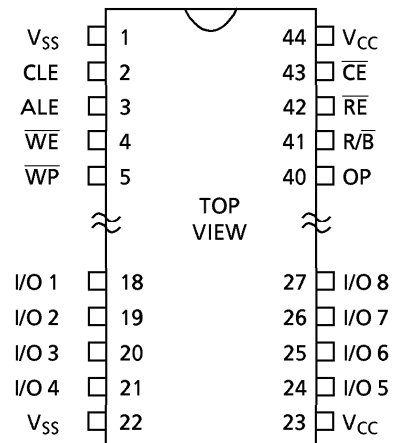


Figure 1. Pinout

Schematic Cell Layout and Address Assignment

The Program operation is implemented in a page units while the Erase operation is carried out in block units.

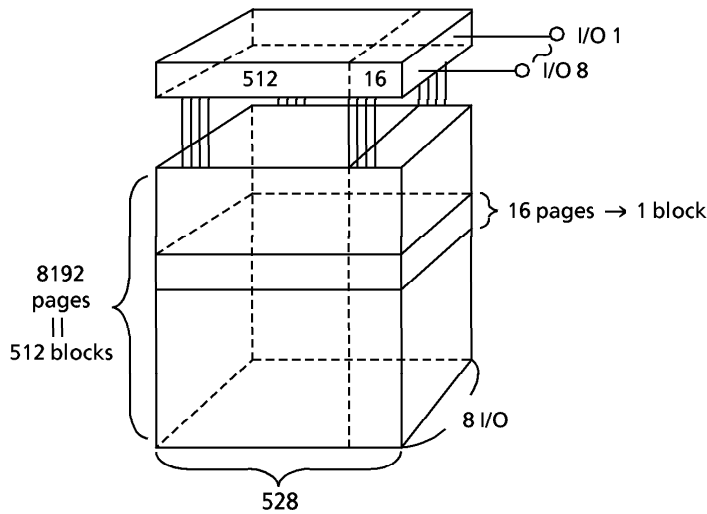


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are for main memory and 16 bytes are for redundancy or other uses.

1 Page = 528 bytes

1 Block = 528 bytes × 16 pages = (8 K + 256) bytes

Total Device Density = 528 bytes × 16 pages × 512 blocks
≈ 33 Mbits (4.125 Mbytes)

The address is acquired through the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	I/O 8
First cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second cycle	A9	A10	A11	A12	A13	A14	A15	A16
Third cycle	A17	A18	A19	A20	A21	* L	* L	* L

A0 to A7 : column address
A9 to A21 : page address
(A13 to A21: block address
A9 to A12 : NAND address in block)

*: A8 is initially set to "Low" or "High" by a "00H" Command or a "01H" Command.

*: I/O 6 to 8 must be set low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read, Erase Suspend and Reset are controlled by the eleven different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{\text{CE}}$, $\overline{\text{WE}}$, $\overline{\text{RE}}$ and $\overline{\text{WP}}$ signals, as shown in Table 2.

Table 2. Logic Table

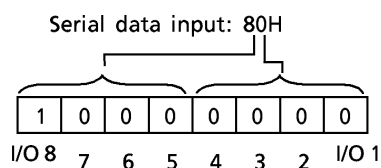
	CLE	ALE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	$\overline{\text{WP}}$
Command Input	H	L	L		H	*
Data Input	L	L	L		H	*
Address Input	L	H	L		H	*
Serial Data Output	L	L	L	H		*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

H: V_{IH} , L: V_{IL} , *: V_{IH} or V_{IL}

Table 3. Command table (HEX data)

	FIRST CYCLE	SECOND CYCLE	ACCEPTABLE COMMAND WHILE BUSY
Serial Data Input	80	–	
Read Mode (1)	00	–	
Read Mode (2)	01	–	
Read Mode (3)	50	–	
Reset	FF	–	○
Auto Program	10	–	
Auto Block Erase	60	D0	
Suspend In Erasing	B0	–	○
Resume	D0	–	
Status Read	70	–	○
ID Read	90	–	

Bit assignment of HEX data
(Example)



Once the device is set to Read mode by the “00H”, “01H” or “50H” command, additional Read commands are not needed for sequential page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

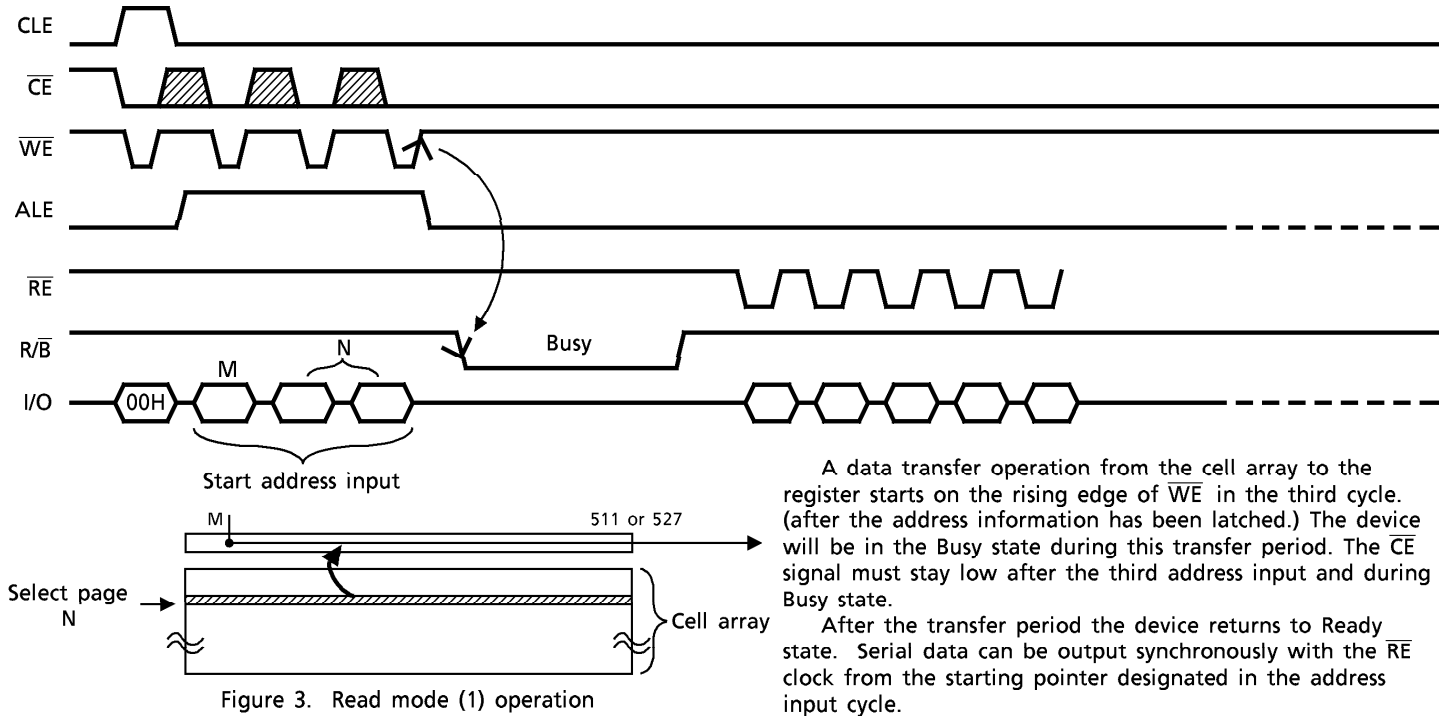
	CLE	ALE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	I/O 1 TO I/O 8	POWER
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

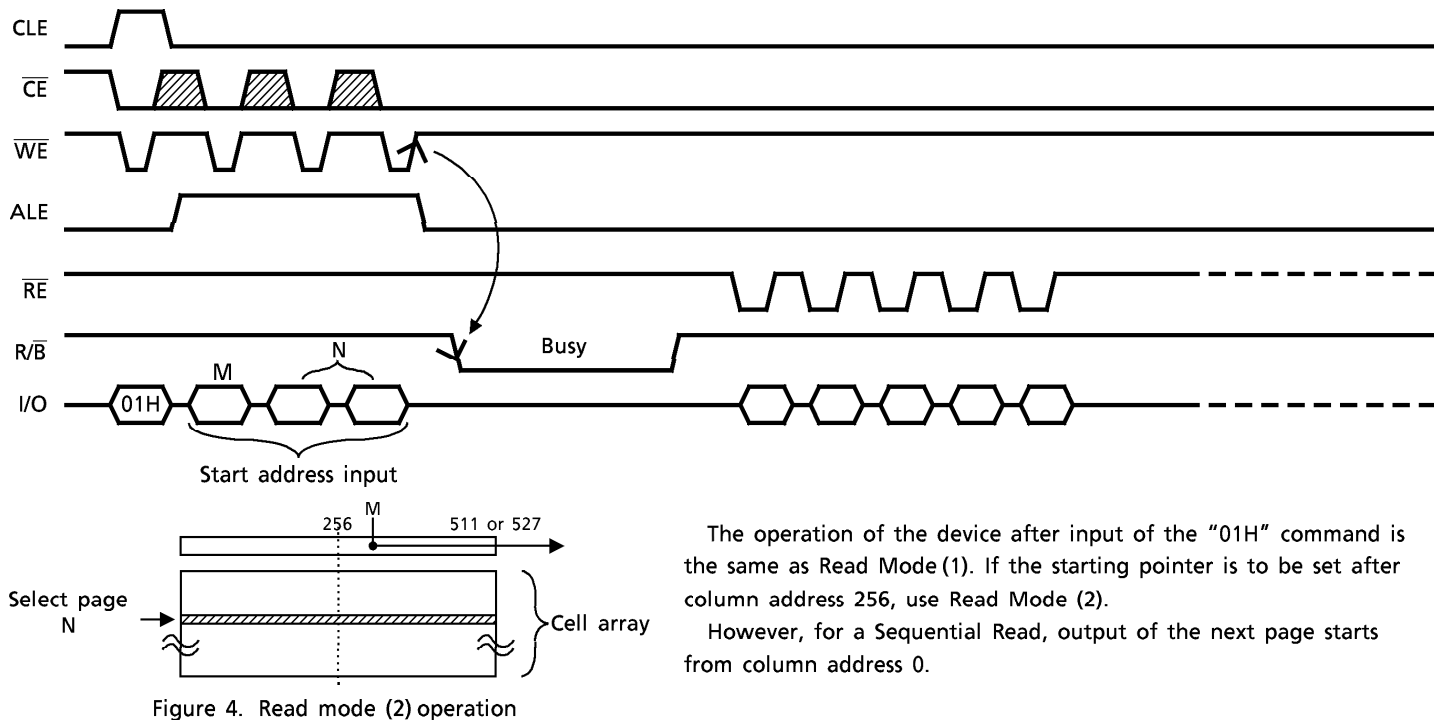
DEVICE OPERATION

Read Mode (1)

Read mode (1) is set by issuing a '00H' command to the command register. Refer to Figure 3 below for timing details and a block diagram.



Read Mode (2)



Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The starting pointer is therefore assigned between bytes 512 and 527.

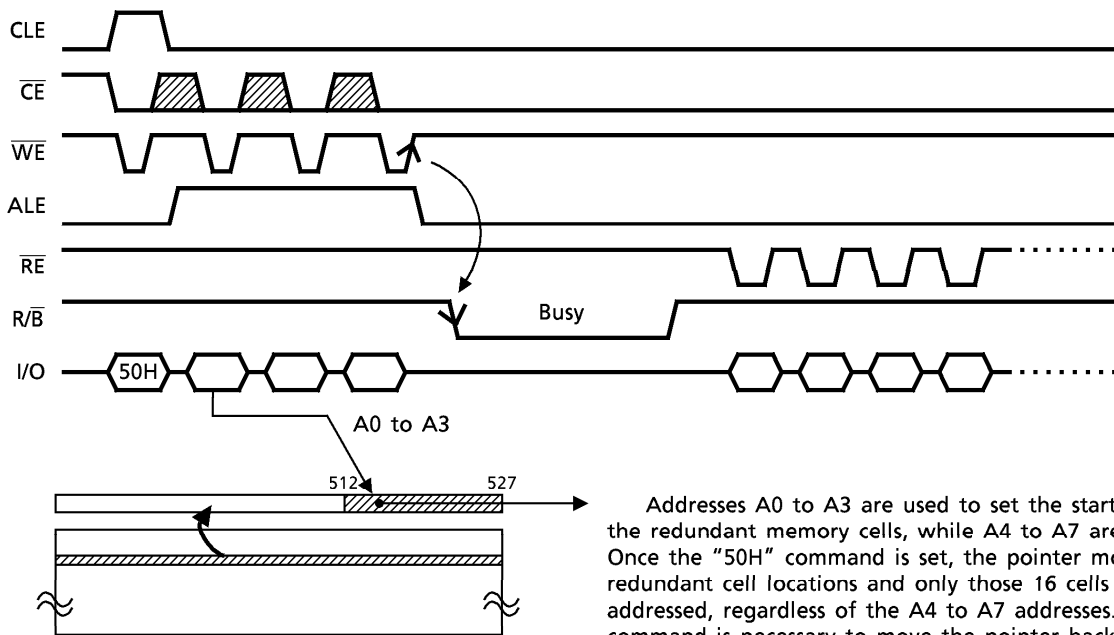
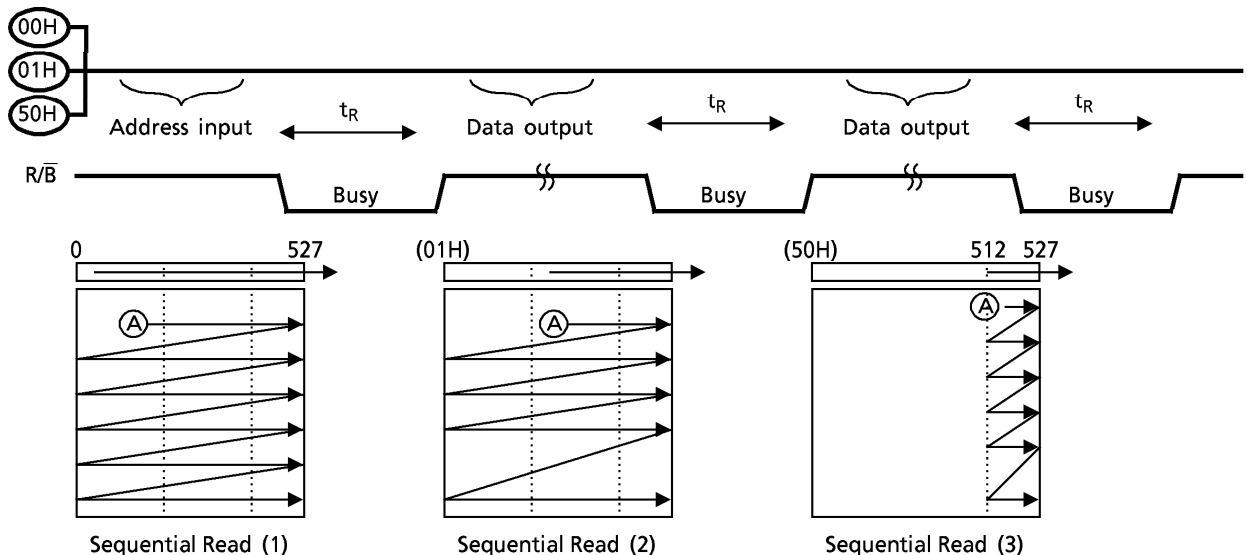


Figure 5. Read mode (3) operation

Read mode (3) operation is invalid when OP is at the V_{CC} level.

Sequential Read (1)(2)(3)

This mode allows the sequential reading of pages without additional address input.



Sequential Read modes (1) and (2) output addresses 0 to 527 as shown above while Sequential Read mode (3) outputs the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address ** on each $\overline{RE}$ clock signal.

** OP = GND : column address 527.
 V_{CC} : column address 511.

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the pass/fail result of a Program or Erase operation, and determine if the device is in Suspend or Protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT
I/O 1	Pass / Fail	Pass : "0" Fail : "1"
I/O 2	Not used	"0"
I/O 3	Not used	"0"
I/O 4	Not used	"0"
I/O 5	Not used	"0"
I/O 6	Suspend	Suspended: "1" Not Suspended: "0"
I/O 7	Ready / Busy	Ready : "1" Busy : "0"
I/O 8	Write protect	Protect : "0" Not Protect : "1"

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

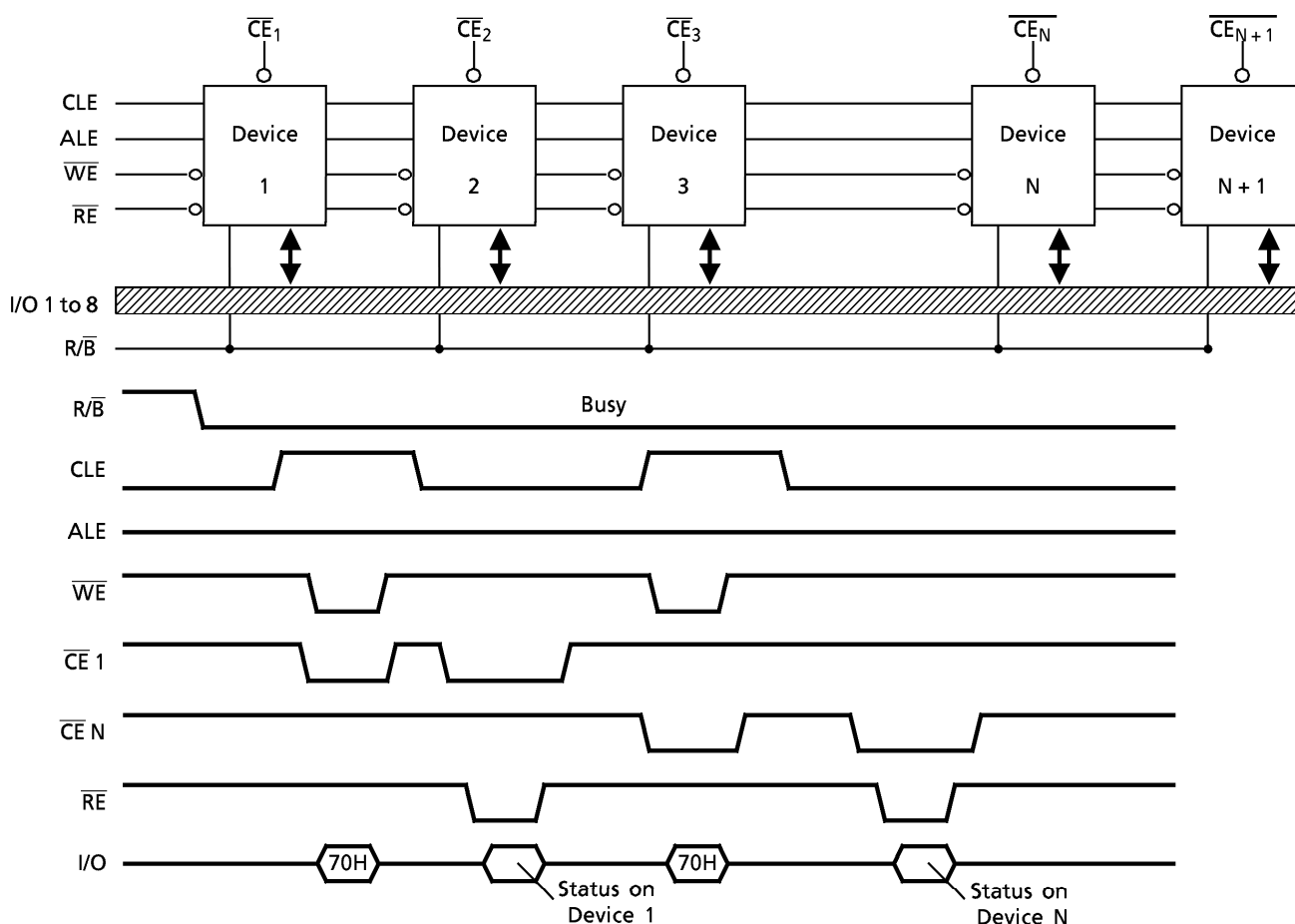
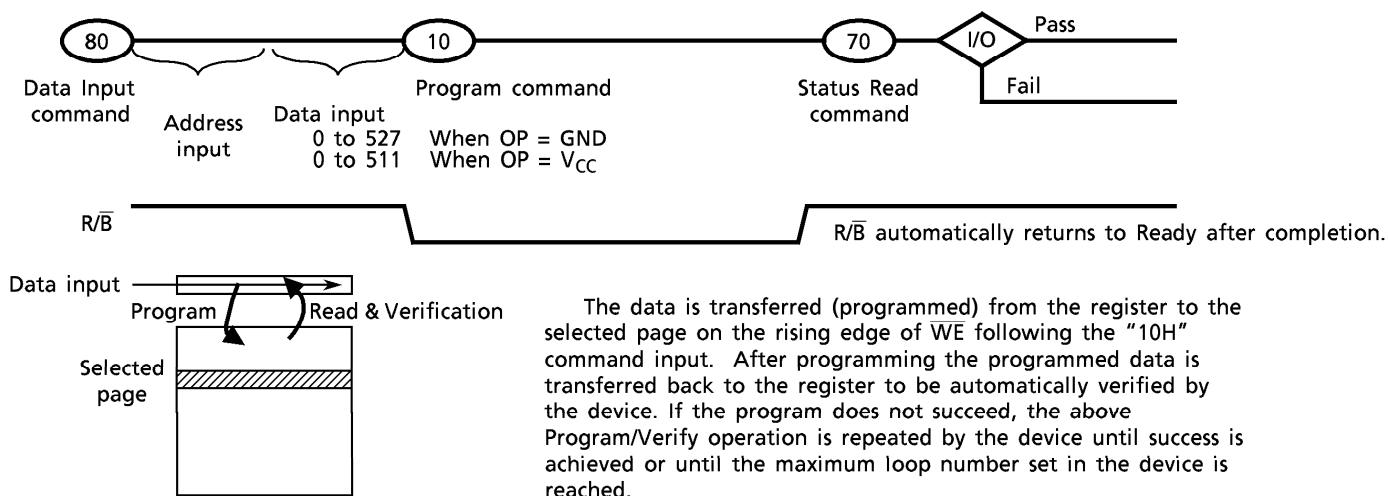


Figure 6. Status read timing application example

SYSTEM DESIGN NOTE : If the $\overline{R/B}$ pin signals of multiple devices are common-wired as shown in the diagram, the Status Read Function can be used to determine the status of each individually selected device.

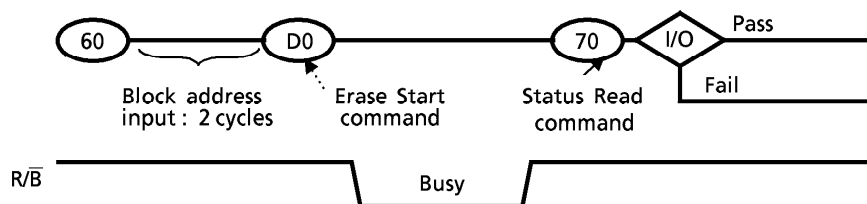
Auto Page Program

The device implements the Automatic Page Program operation after receiving a "10H" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



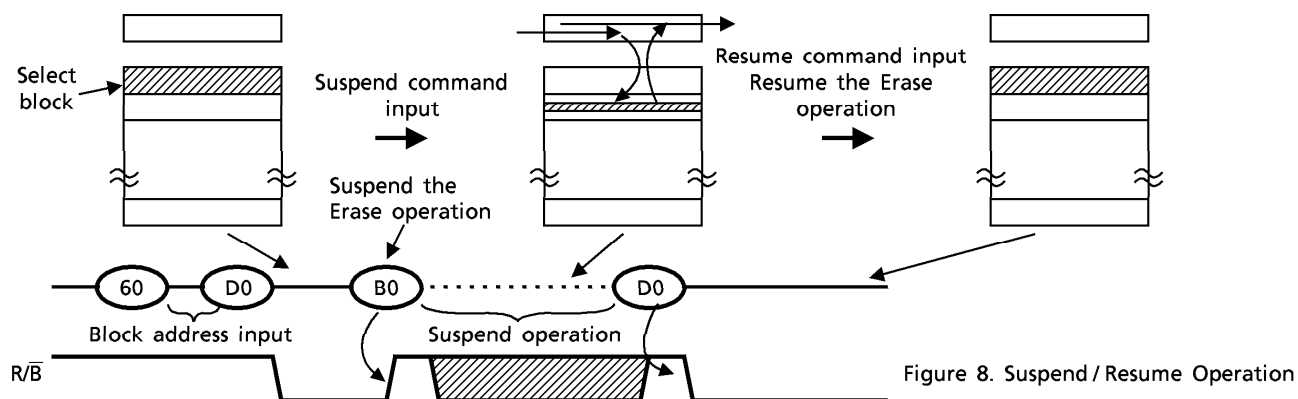
Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Execution command "D0H" which follows the Erase Set-Up command "60H". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



Suspend / Resume

The device has the ability to suspend the Erase operation to allow Program or Read operations to be performed on the device. The block diagram and command sequence for this operation are shown below. (Refer to the detailed timing chart)



The B0...D0 Suspend/Resume cycle can be repeated up to 20 times during a Block Erase operation. After the Resume command has been input, the Erase operation continues from the point at which it left off and does not have to be restarted.

Reset

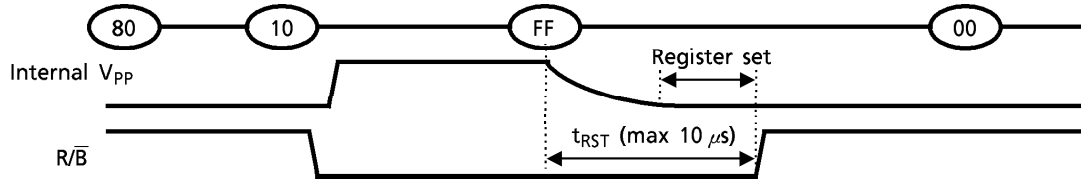
The Reset mode stops all operations. For example, in the case of a Program or Erase operation the regulated voltage is discharged to 0 volts and the device will go into Wait state. The address and data registers are set as follows after a Reset:

- Address Register : All "0"
- Data Register : All "1"
- Operation Mode : Wait State

The response after an "FFH" Reset command input during each operation is as follows:

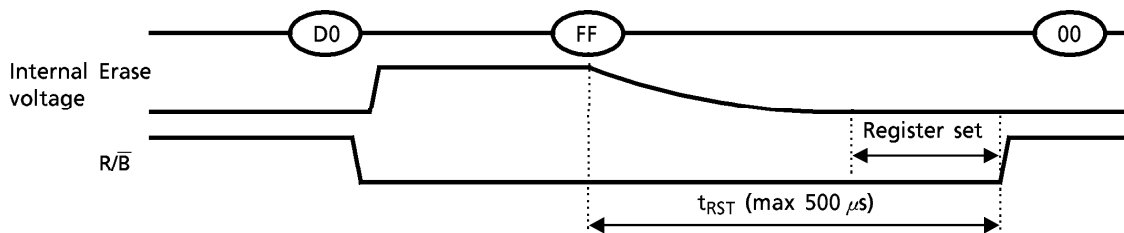
- When a Reset (FFH) command is input during programming

Figure 9.



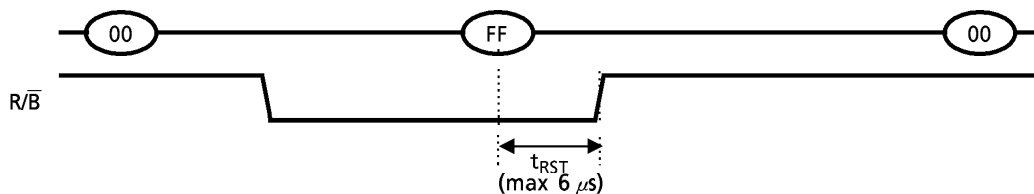
- When a Reset (FFH) command is input during erasing

Figure 10.



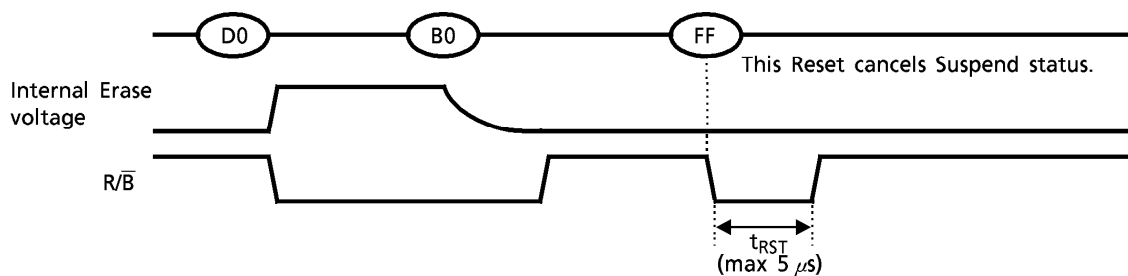
- When a Reset (FFH) command is input during a Read operation

Figure 11.



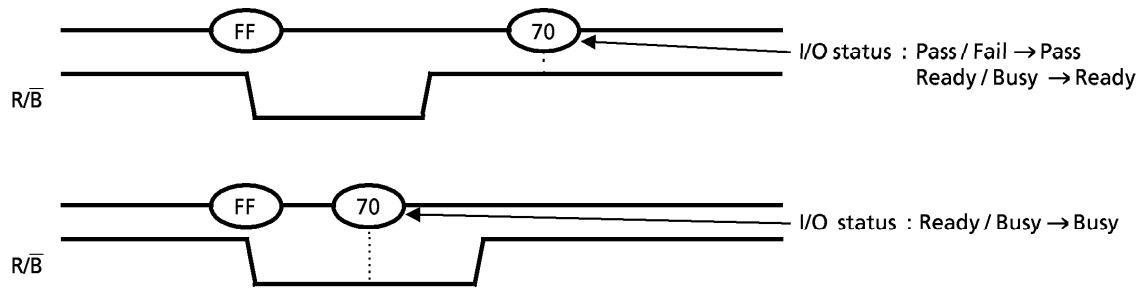
- When a Reset (FFH) command is input after Suspend

Figure 12.



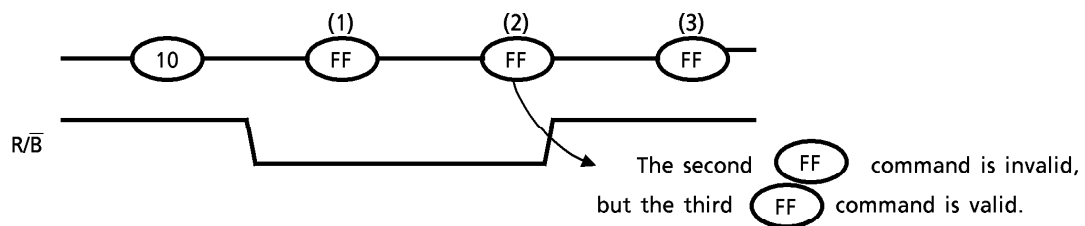
- When a Status Read command (70H) is input after a Reset

Figure 13.



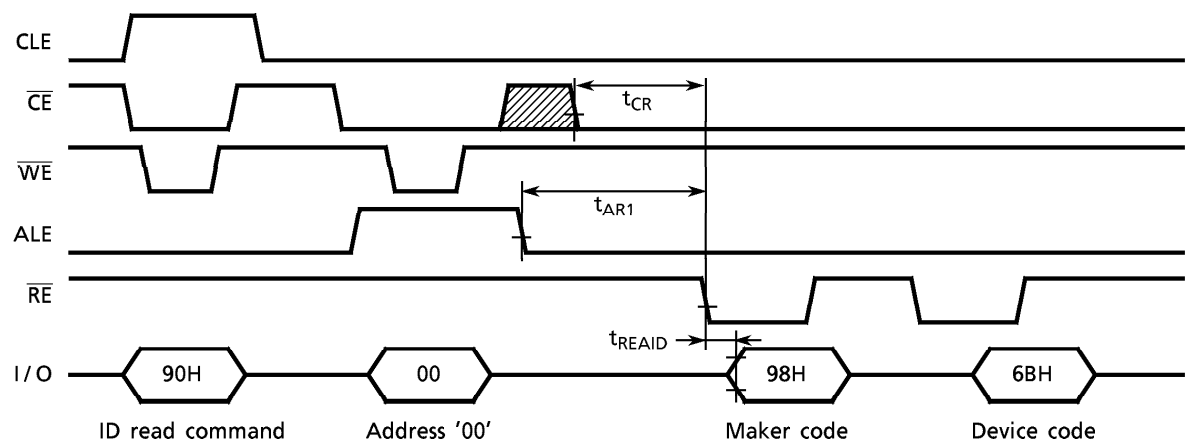
- When more than one Reset commands are input in succession

Figure 14.



ID Read

The TC5832 contains ID codes to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions :



For the access time of t_{READ} , t_{CR} and t_{AR1} refer to AC CHARACTERISTICS.

Figure 15. ID read timing

Table 6. Code table

	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	HEX DATA
Maker code	1	0	0	1	1	0	0	0	98H
Device code	0	1	1	0	1	0	1	1	6BH

DEVICE PHYSICS

Program Operation

Figure 16 shows the NAND memory cell level details of the programming mechanism. The Program operation is used to write “0” data into an erased memory cell (“1” data cell) using a tunneling mechanism. An example Program operation to program “0” data into TR1 and “1” data into TR2 is as follows:

- (1) A high level is applied to Select line 1 and a low level is applied to Select line 2 so that the device is connected to the Bit line and disconnected from the ground line.
- (2) V_{pp} (≈ 20 V) is applied to the selected word line and an inhibit voltage of V_{PI} (≈ 10 V) is applied to the unselected word lines.
- (3) 0 volts is applied to the bit line tied to cell transistor TR1 and the inhibit voltage V_{DPI} (≈ 10 V) is applied to the bit line tied to TR2.
- (4) V_{pp} is applied between the control gate and the channel in TR1, as shown in Figure 16, which causes electrons to be injected from the channel to the floating gate by a tunneling mechanism.
- (5) The injected electrons are captured in the floating gate surrounded by an oxide layer and will remain, even after power is cut off, until they are removed by an Erase operation.
- (6) Although 20 volts is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10 V because the voltage of the channel is 10 V. Therefore, tunneling does not take place. (i.e. the electron is not injected into the floating gate.)
- (7) Tunneling does not take place in the unselected pages because of the 10 V (V_{PI}) applied to the unselected word lines which makes the voltage difference between the control gate and channel only 10 volts.

Thus the floating gate of the “0” cell is charged to “Minus” and that of the “1” cell is charged to “Plus”.

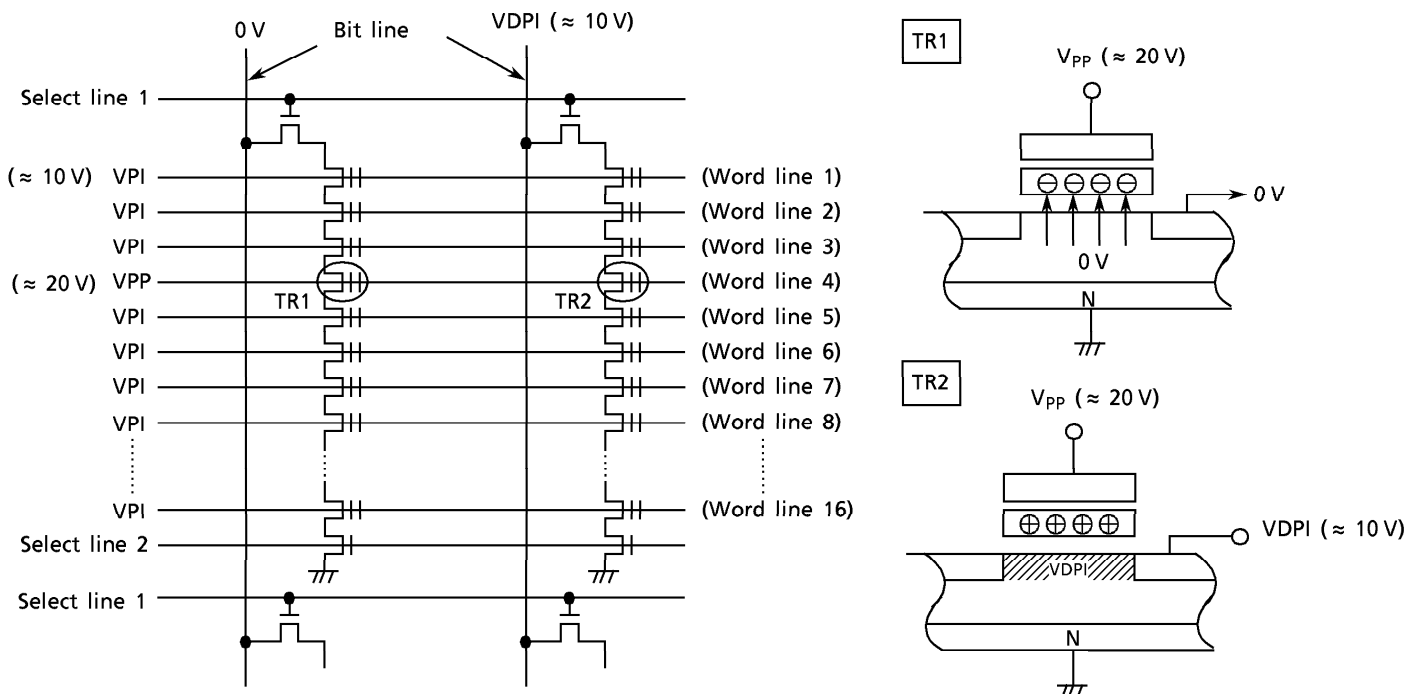


Figure 16. Program Device Physics

Erase Operation

Figure 17 shows the NAND memory cell level details of the Erase mechanism. The Erase operation is used to turn the "0" (programmed) cells back to "1" in a block. The captured electrons are pulled out from the floating gate to the substrate by a tunneling mechanism.

0 volts is applied to the control gate and V_{pp} (≈ 20 V) is applied to the substrate so that a 20-volt potential is created and the electrons in the floating gate are pulled out by the tunneling mechanism.

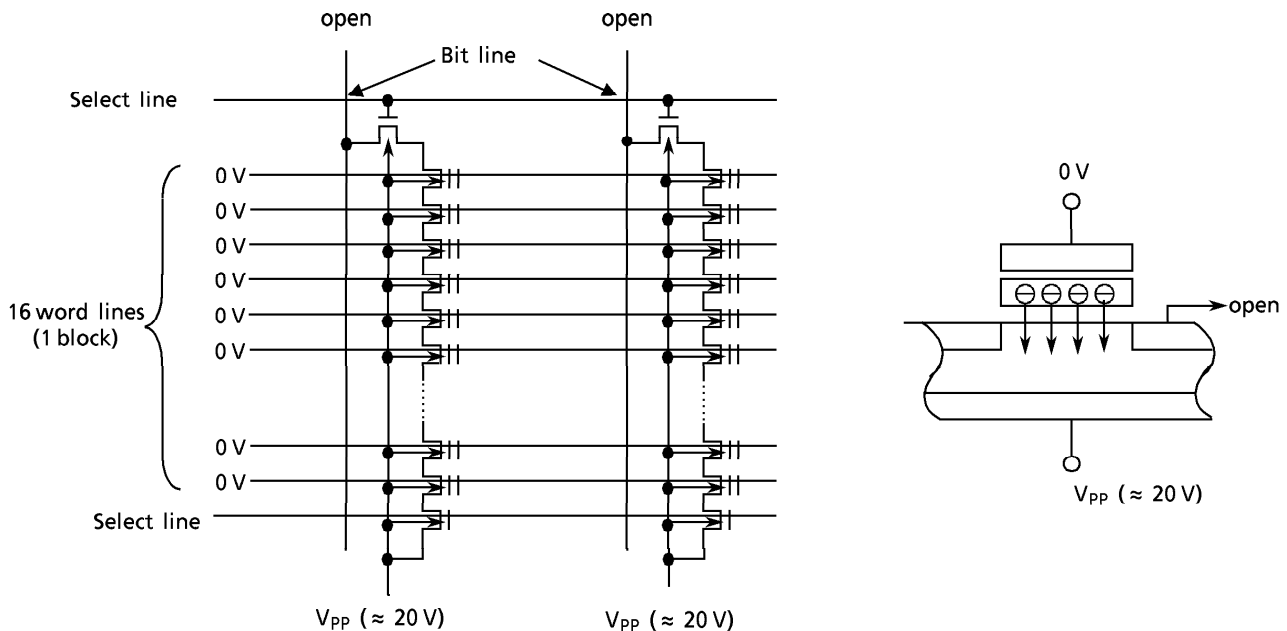


Figure 17. Erase Device Physics

Read operation

After programming the state of the memory cell is either "0" (minus charge on the floating gate) or "1" (plus charge on the floating gate). Each state is indicated as the "threshold voltage (V_{th})" which is a characterization parameter of the MOS transistor as shown in Figure 18. The threshold voltage of a transistor with data "0" is distributed in the "plus" region while a transistor with data "1" is distributed in the "minus" region. The distribution band depends on the fluctuation of the transistor.

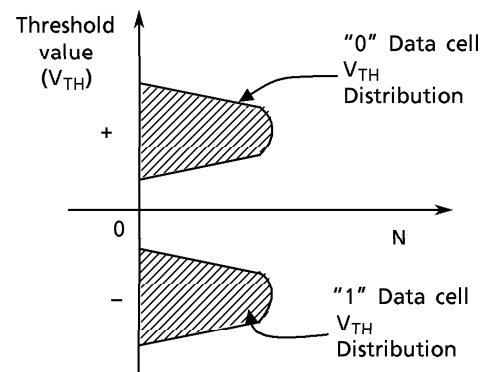


Figure 18. V_{TH} Distribution for "0" and "1" data cells

Figure 19 shows memory cell level details of the Read operation mechanism:

- (1) A high voltage is applied to Select lines 1 and 2 in the block which includes the selected page, so that the 16 NAND memory cells are connected to the Bit line and ground.
- (2) 0 volts is applied to the control gates of the selected page and a high level voltage is applied to the control gates of the unselected pages.
- (3) In Figure 19, transistor TR2 with data "1" turns on, transistor TR1 with data "0" turns off, and all other unselected transistors turn on.
- (4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground, while the precharged bit line tied to TR1 remains high because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as "1" and "0" respectively.

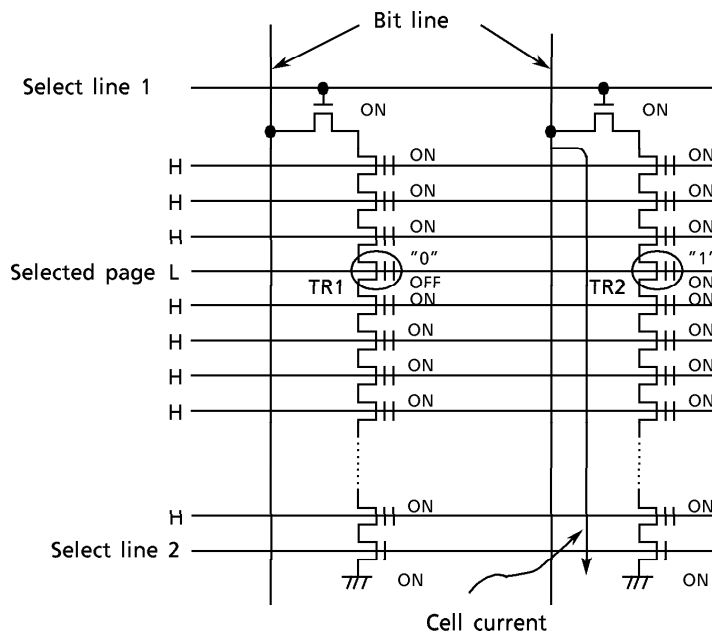


Figure 19. Read Device Physics

APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Data input as a command other than the specified commands in Table 3 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Pointer control for "00H", "01H", "50H"

The device has three read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and figure 20 shows a block diagram of the modes' operations.

Table 7. Pointer Destination

READ MODE	COMMAND	POINTER
(1)	00H	0 to 255
(2)	01H	256 to 511
(3)	50H	512 to 527

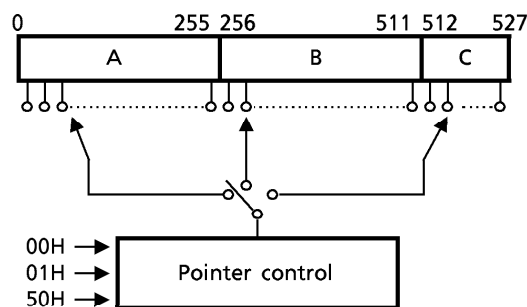
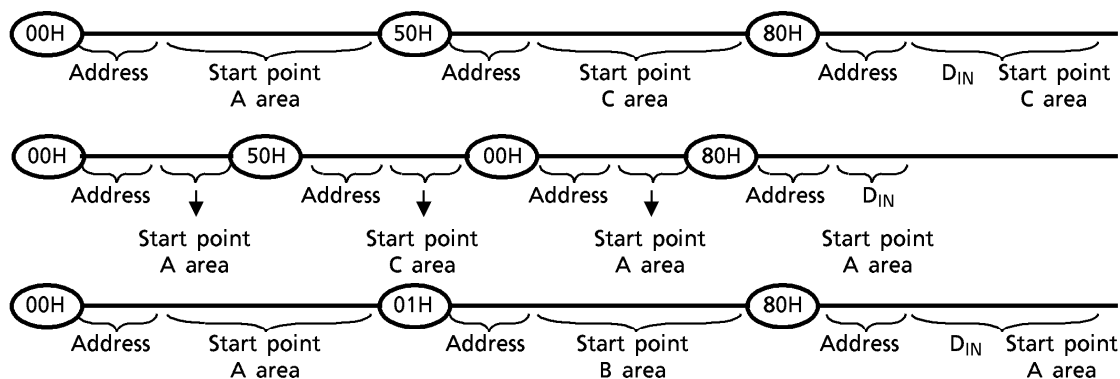


Figure 20. Pointer control

The pointer is set to region "A" by the "00H" command, to region "B" by the "01H" command, and to region "C" by the "50H" command.

(Example)

The "00H" command needs to be input to set the pointer back to region "A" when the pointer is in region "C".



To program region "C" only, set the start point to region "C" using the "50H" command. If region "C" only is to be programmed, or if $OP = V_{CC}$, the contents of the data register must be set to "1" in advance using the "FFH" command.

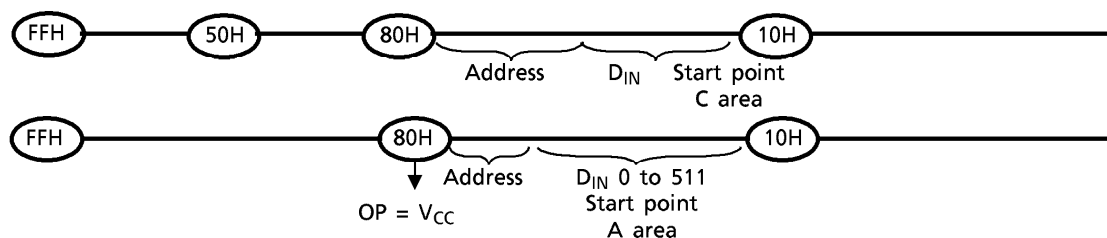


Figure 21. Example for Pointer Set

(5) Suspend command "B0H"

The following issues need to be observed when the device is interrupted by a "B0H" command during block erasing.

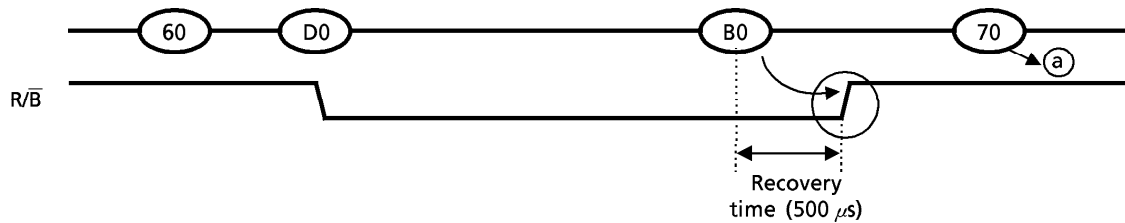


Figure 24.

The device status changes from Busy to Ready when "B0H" is input. However, the following two cases cannot be distinguished from one another.

- After a "B0H" command input, Busy → Ready
- After an Erase operation is completed with a "D0H" command, Busy → Ready

Therefore, the device status needs to be checked to see whether or not the "B0H" command has been accepted by issuing a "70H" command after the device goes to Ready.

① The device responds as follows when a "D0H" command (Resume) is input instead of "70H".

- "B0H" has been accepted: Erase operation is executed. (The device is Busy.)
- "B0H" has not been accepted. (Erase operation has been completed)
: "D0H" command cannot be accepted. (The device is Ready.)

The two cases above can be checked by monitoring the R/B signal.

(6) When auto programming fails.

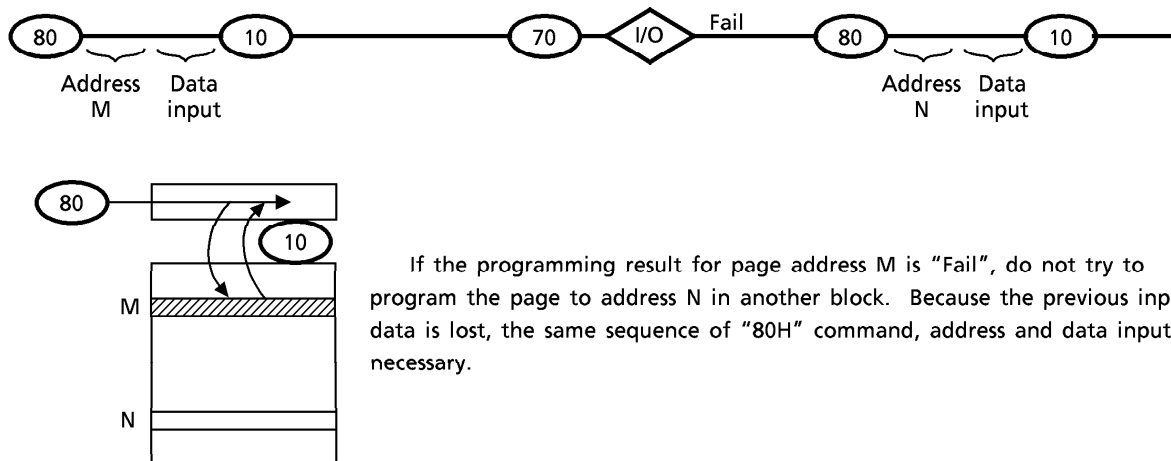


Figure 25.

If the programming result for page address M is "Fail", do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of "80H" command, address and data input is necessary.

(7) Data transfer

The data in page address M cannot be automatically tranferred to page address N. If the following sequence is executed, the data will be inverted. (i.e. "1" data will become "0" and "0" will become "1".)

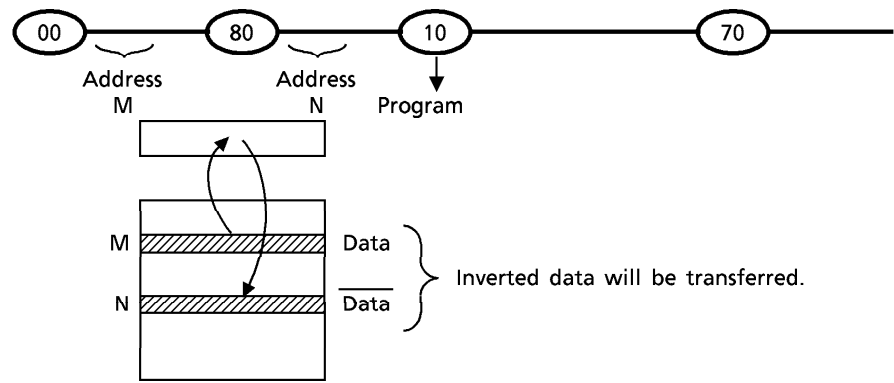
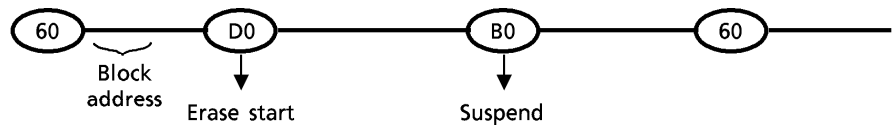


Figure 26.

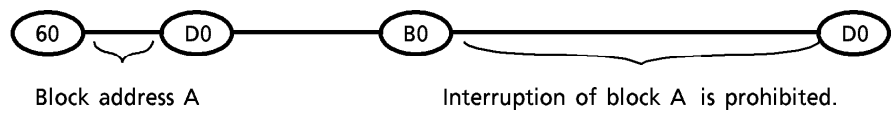
(8) Block Erase after Suspend command "B0H"



A Block Erase command is prohibited when the device has been suspended by the input of a "B0H" command during a Block Erase operation. Only a Program or Read operation is allowed during this Erase Suspend interruption.

(9) Interruption of block erasure

After the input of a "B0H" command, neither a Program nor a Read operation is allowed for the block which is currently being erased



(10) $R/\overline{B}$: Termination for the Ready/Busy pin ($R/\overline{B}$)

A pull-up resistor must be used for termination because the $R/\overline{B}$ buffer consists of an open drain circuit.

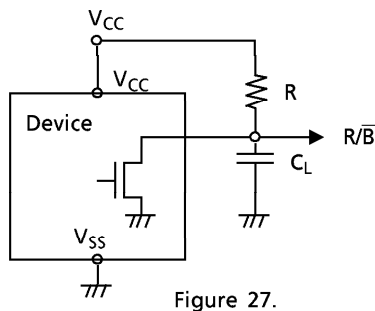
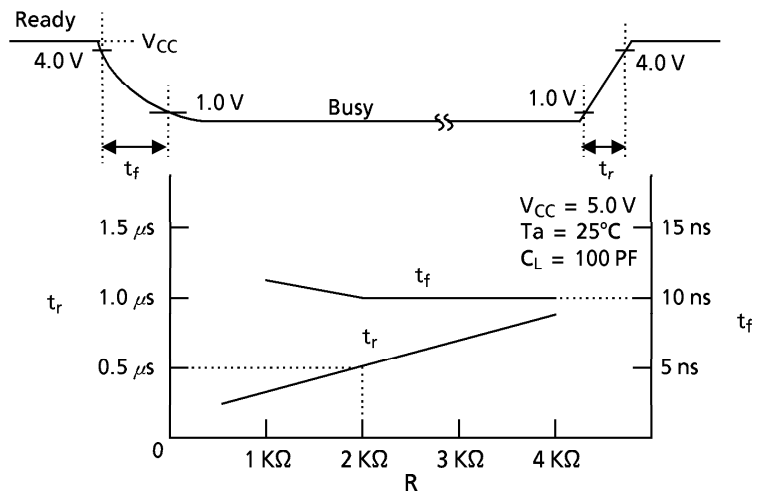


Figure 27.

This data may vary from device to device.
We recommend that you use this data as a
reference when selecting a resistor value.



(11) Status after Power On

Although the device is set to Read mode after power-up, the following sequence is needed because all input signals may not be stable at power on.

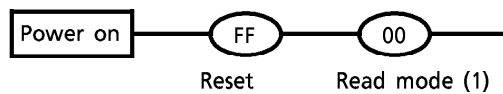


Figure 28.

(12) Power On/Off Sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power on/off. The following timing is necessary:

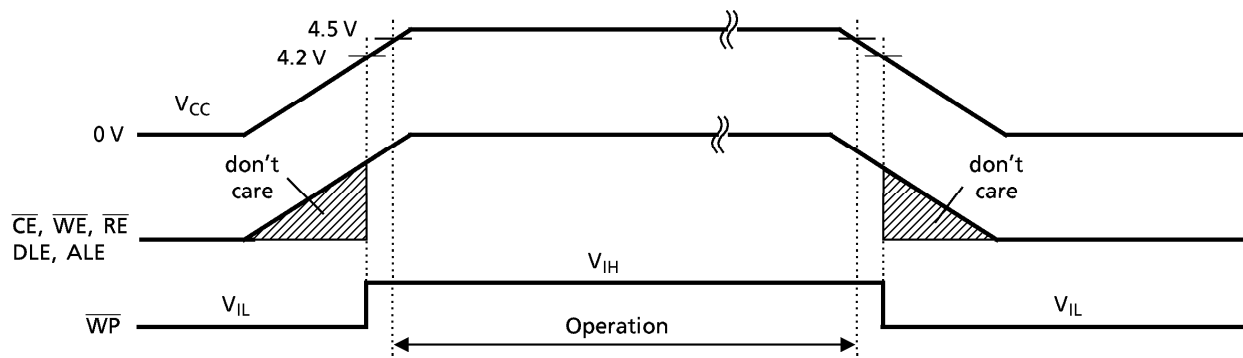
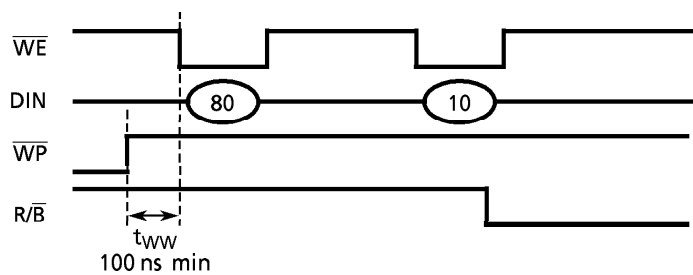
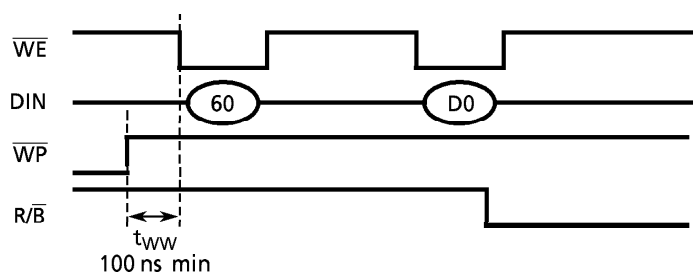


Figure 29. Power On/Off Sequence

(13) Set-up for $\overline{WP}$ Signal

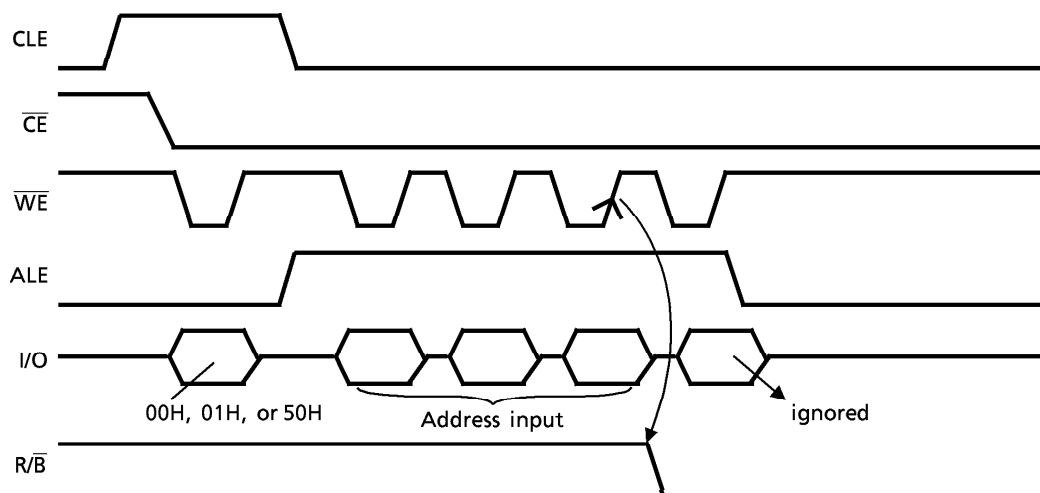
The Erase and Program operations are automatically reset when $\overline{WP}$ goes low. The following conditions must be met:

ProgramErase

(14) When four address cycles are input

Although the device may acquire the fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when $\overline{WE}$ goes high in the third cycle.

Figure 30.

Programming operation

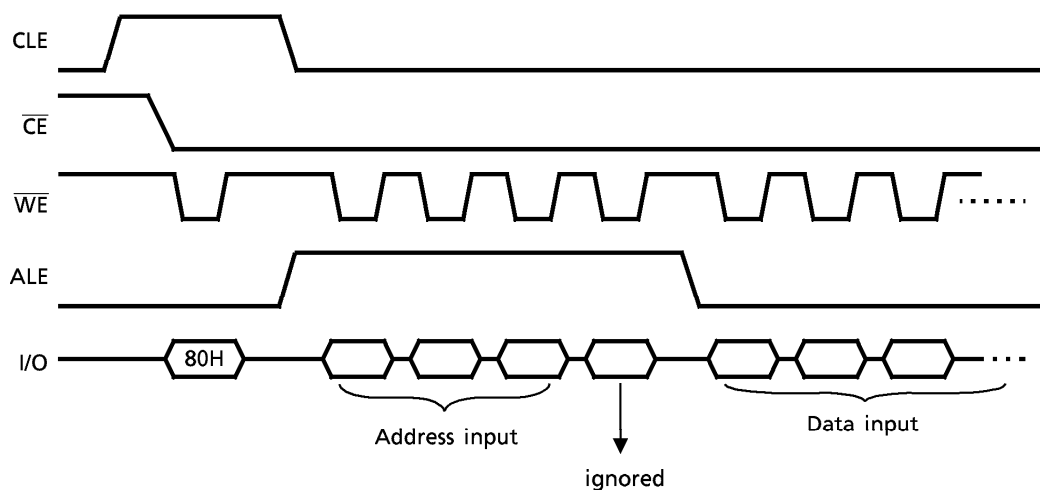


Figure 31.

(15) Number of programming cycle on the same page (Partial Page Program)

A page can be divided into up to 10 segments. Each segment can be programmed individually as shown below.

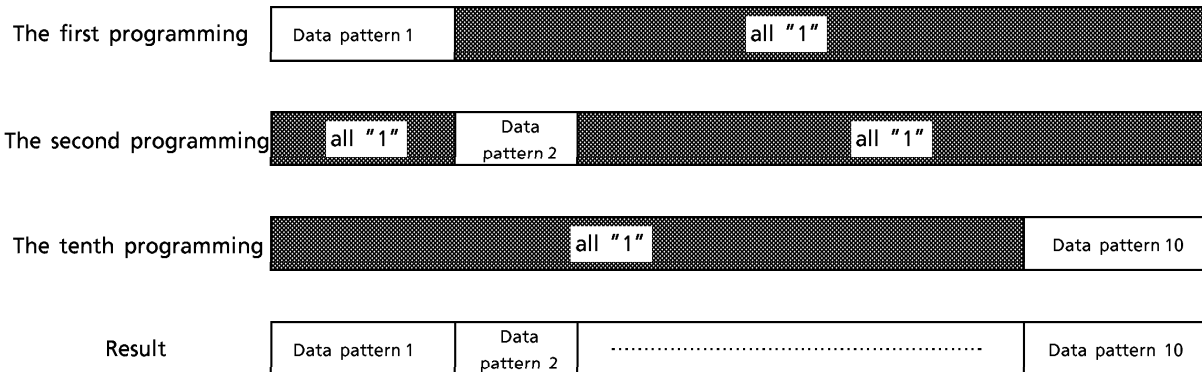


Figure 35.

Note: The input data for unprogrammed or previously programmed page segments must be "1".
(i.e. Set all page bytes outside the segment to be programmed to "1".)

(16) Note regarding the $\overline{RE}$ Signal

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by the "00H", "01H" or "50H" command, the internal column address counter is incremented by the $\overline{RE}$ clock independent of the timing of the address input. If the $\overline{RE}$ clocks are input before address input and the pointer reaches the last column address, an internal read operation (array → register) will occur and the device will be in the Busy state. (Refer to Figure 33)

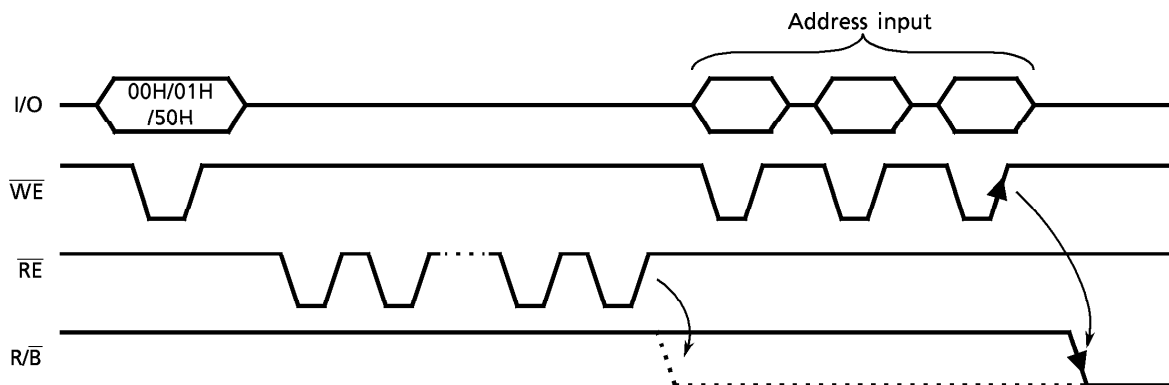


Figure 33.

Hence the $\overline{RE}$ clocks must be inputted after address input.

(17) Invalid block (bad block)

The device contains unusable blocks. Therefore, the following issues must be recognized:

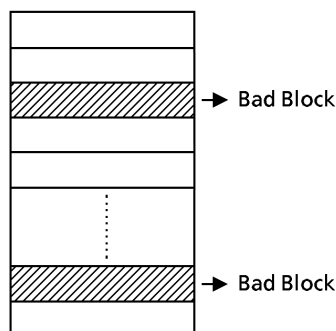


Figure 34.

Check if the device has any bad blocks after device installation into the system. Do not try to access bad blocks. A bad block does not affect the performance of good blocks because it is isolated from the bit line by the select gate.

The number of valid blocks is as follows:

	MIN	TYP	MAX	UNIT
Valid (Good) Block Number	502	508	512	Block

Figure 36 shows the bad block test flow.

(18) Failure Phenomena for Program and Erase Operations.

The device may fail during program or erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Program Failure	Status Read after Prog. → Block Replacement
Single Bit*	Program Failure '1' → '0'	(1) Block Verify after Prog. → Retry
		(2) ECC

* : (1) or (2)

- ECC : Error Correcting code → Hamming Code etc.
Example : 1 bit correction & 2 bit detection.
- Block Replacement

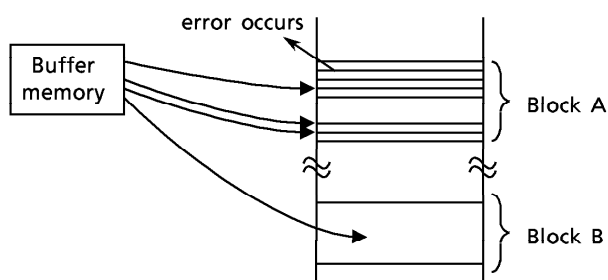
Program

Figure 35.

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a 'bad block' table or an another appropriate scheme.)

Erase

When an error occurs for an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme).

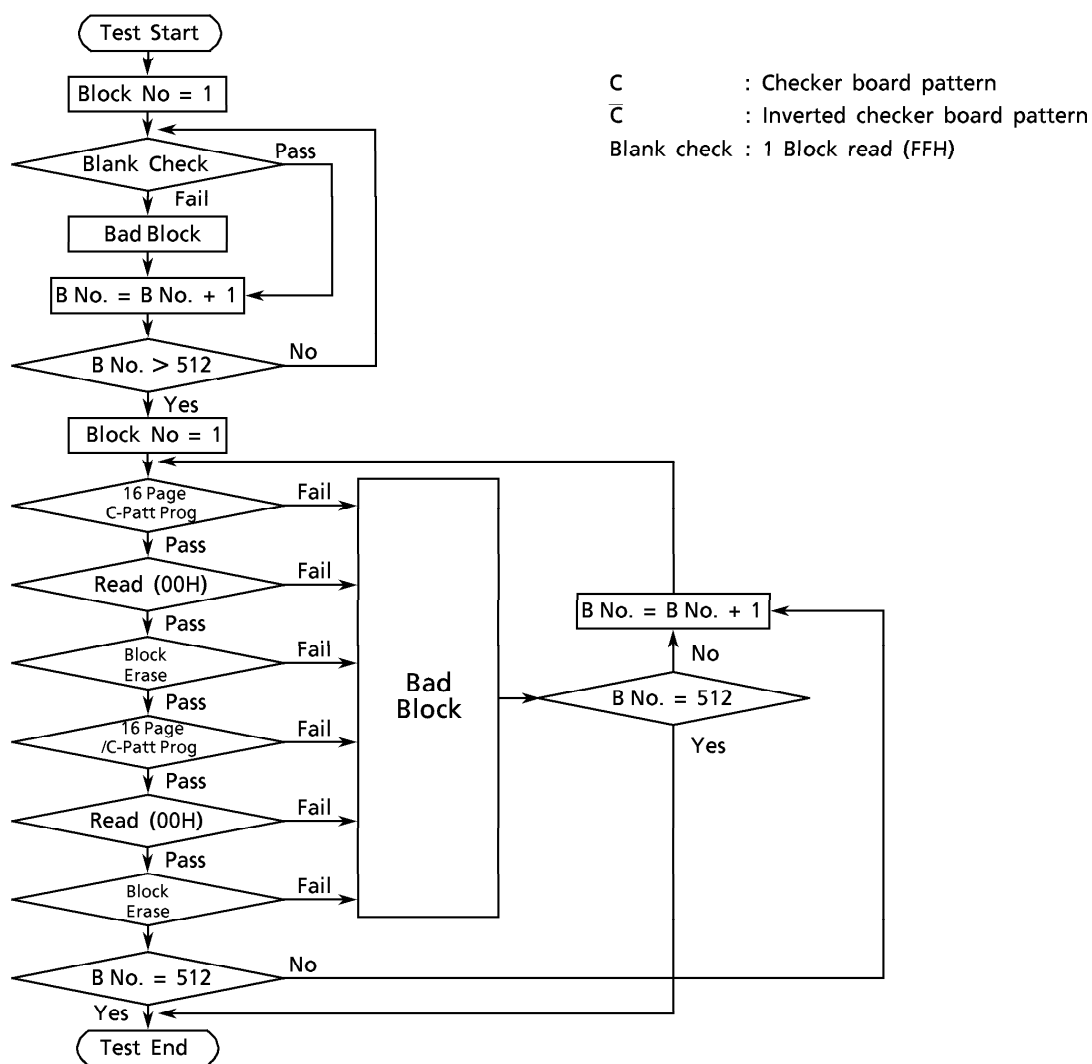
BAD BLOCK TEST FLOW

Figure 36.

PACKAGE DIMENSIONS

Plastic TSOP

TSOP II 44/40 - P - 400 - 0.80B

UNITS : mm

