

## 524,288-WORD BY 8-BIT STATIC RAM

### DESCRIPTION

The TC55V4000ST is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 0.5  $\mu$ A standby current (at  $V_{DD} = 3$  V,  $T_a = 25^\circ\text{C}$ ) when chip enable ( $\overline{CE}$ ) is asserted high. There are two control inputs.  $\overline{CE}$  is used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55V4000ST is available in a normal pinout plastic 32-pin thin-small-outline package (TSOP).

### FEATURES

- Low-power dissipation  
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.6 V
- Power down features using  $\overline{CE}$
- Data retention supply voltage of 1.5 to 3.6 V
- Direct TTL compatibility for all inputs and outputs
- Standby Current (maximum):

3.6 V	7 $\mu$ A
3.0 V	5 $\mu$ A

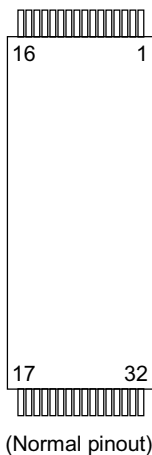
- Access Times (maximum):

	TC55V4000ST	
	-70	-85
Access Time	70 ns	85 ns
$\overline{CE}$ Access Time	70 ns	85 ns
$\overline{OE}$ Access Time	35 ns	45 ns

- Package:  
TSOP 32-P-0.50 (ST) (Weight: 0.24 g typ)

### PIN ASSIGNMENT (TOP VIEW)

#### 32 PIN TSOP

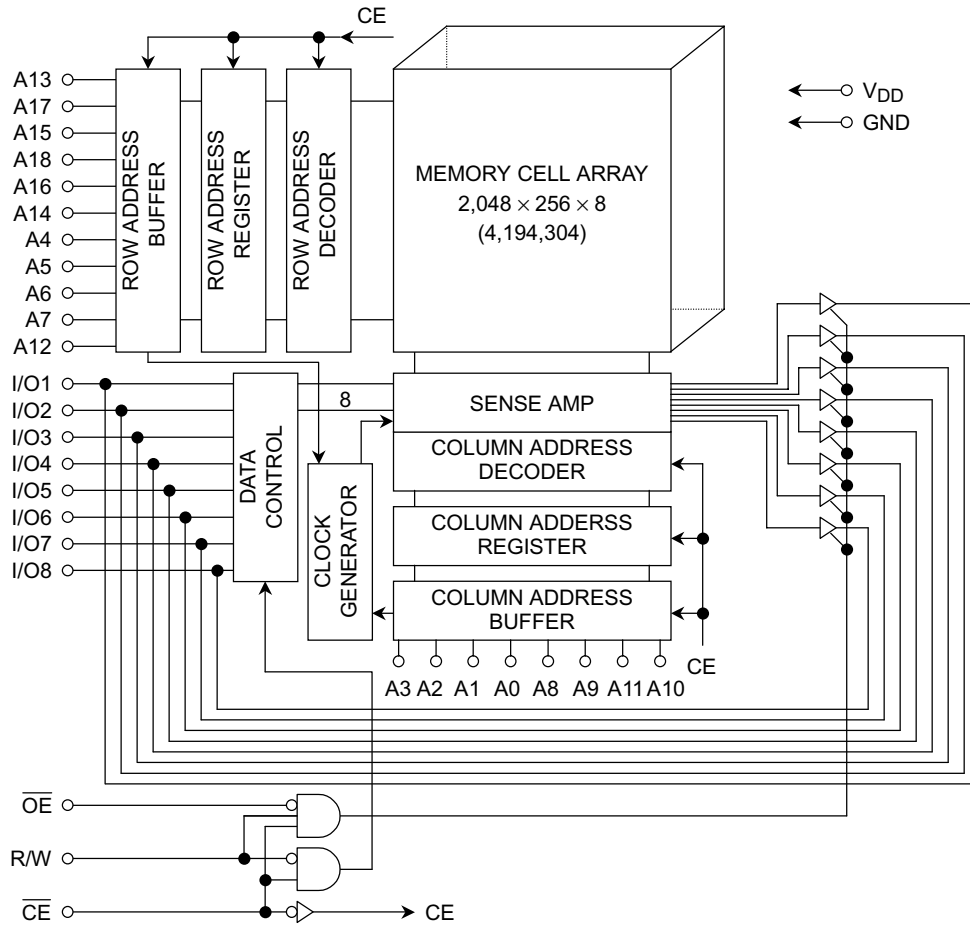


### PIN NAMES

A0~A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1~I/O8	Data Inputs/Outputs
$V_{DD}$	Power
GND	Ground

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A11	A9	A8	A13	R/W	A17	A15	$V_{DD}$	A18	A16	A14	A12	A7	A6	A5	A4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A3	A2	A1	A0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A10	$\overline{OE}$

## BLOCK DIAGRAM



## OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	Output	$I_{DDO}$
Write	L	*	L	Input	$I_{DDO}$
Output Deselect	L	H	H	High-Z	$I_{DDO}$
Standby	H	*	*	High-Z	$I_{DSD}$

\* = don't care  
H = logic high  
L = logic low

## MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
$V_{DD}$	Power Supply Voltage	-0.3~4.6	V
$V_{IN}$	Input Voltage	-0.3~4.6	V
$V_{I/O}$	Input/Output Voltage	-0.5~ $V_{DD} + 0.5$	V
$P_D$	Power Dissipation	0.6	W
$T_{solder}$	Soldering Temperature (10s)	260	°C
$T_{stg}$	Storage Temperature	-55~150	°C
$T_{opr}$	Operating Temperature	-40~85	°C

\*: -3.0 V when measured at a pulse width of 50ns

**DC RECOMMENDED OPERATING CONDITIONS** ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ )

SYMBOL	PARAMETER	2.3 V~3.6 V			UNIT
		MIN	TYP	MAX	
$V_{DD}$	Power Supply Voltage	2.3	3.0	3.6	V
$V_{IH}$	Input High Voltage	2.2	—	$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	-0.3*	—	$V_{DD} \times 0.22$	V
$V_{DH}$	Data Retention Supply Voltage	1.5	—	3.6	V

\*: -3.0 V when measured at a pulse width of 50 ns

**DC CHARACTERISTICS** ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 2.3$  to  $3.6$  V)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V~V <sub>DD</sub>				—	—	±1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> – 0.5 V				–0.5	—	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V				2.1	—	—	mA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}$ = V <sub>IH</sub> or $\overline{OE}$ = V <sub>IH</sub> or R/W = V <sub>IL</sub> , V <sub>OUT</sub> = 0 V~V <sub>DD</sub>				—	—	±1.0	μA
I <sub>DDO1</sub>	Operating Current	$\overline{CE}$ = V <sub>IL</sub> and R/W = V <sub>IH</sub> , I <sub>OUT</sub> = 0 mA, Other Input = V <sub>IH</sub> /V <sub>IL</sub>	V <sub>DD</sub> = 3.0 V ± 10%	t <sub>cycle</sub>	min	—	—	50	mA
					1 μs	—	—	10	
I <sub>DDO2</sub>		$\overline{CE}$ = 0.2 V and R/W = V <sub>DD</sub> – 0.2 V, I <sub>OUT</sub> = 0 mA, Other Input = V <sub>DD</sub> – 0.2 V/0.2 V			min	—	—	45	mA
					1 μs	—	—	5	
I <sub>DDS1</sub>	Standby Current	$\overline{CE}$ = V <sub>IH</sub>				—	—	3	mA
I <sub>DDS2</sub>		$\overline{CE}$ = V <sub>DD</sub> – 0.2 V, V <sub>DD</sub> = 1.5 V~3.6 V	V <sub>DD</sub> = 3.0 V ± 10%	Ta = 25°C	—	—	0.6	μA	
				Ta = –40~85°C	—	—	6		
			V <sub>DD</sub> = 3.3 V ± 0.3 V	Ta = 25°C	—	—	0.7		
				Ta = –40~85°C	—	—	7		
			V <sub>DD</sub> = 3 V	Ta = 25°C	—	0.05	0.5		
				Ta = –40~40°C	—	—	1		
				Ta = –40~85°C	—	—	5		

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

## AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = -40° to 85°C, VDD = 2.7 to 3.6 V)

### READ CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	70	—	85	—	ns
t <sub>ACC</sub>	Address Access Time	—	70	—	85	
t <sub>CO</sub>	Chip Enable Access Time	—	70	—	85	
t <sub>OE</sub>	Output Enable Access Time	—	35	—	45	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	—	5	—	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	—	0	—	
t <sub>OD</sub>	Chip Enable High to Output High-Z	—	30	—	35	
t <sub>ODO</sub>	Output Enable High to Output High-Z	—	30	—	35	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	70	—	85	—	ns
t <sub>WP</sub>	Write Pulse Width	50	—	55	—	
t <sub>CW</sub>	Chip Enable to End of Write	60	—	70	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	R/W Low to Output High-Z	—	25	—	35	
t <sub>OEW</sub>	R/W High to Output Active	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	30	—	35	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

### AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.4 V
Timing measurements	VDD × 0.5
Reference level	VDD × 0.5
t <sub>R</sub> , t <sub>F</sub>	5 ns

**AC CHARACTERISTICS AND OPERATING CONDITIONS**(Ta = -40° to 85°C, V<sub>DD</sub> = 2.3 to 3.6 V)**READ CYCLE**

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	85	—	100	—	ns
t <sub>ACC</sub>	Address Access Time	—	85	—	100	
t <sub>CO</sub>	Chip Enable Access Time	—	85	—	100	
t <sub>OE</sub>	Output Enable Access Time	—	45	—	50	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	—	5	—	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	—	0	—	
t <sub>OD</sub>	Chip Enable High to Output High-Z	—	35	—	40	
t <sub>ODO</sub>	Output Enable High to Output High-Z	—	35	—	40	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	

**WRITE CYCLE**

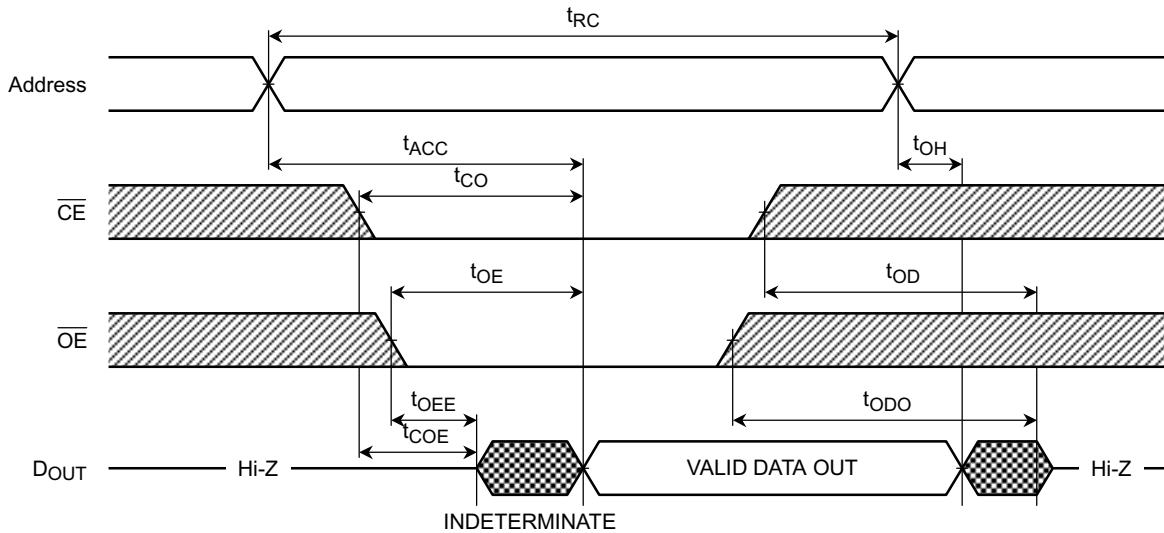
SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	85	—	100	—	ns
t <sub>WP</sub>	Write Pulse Width	55	—	60	—	
t <sub>CW</sub>	Chip Enable to End of Write	70	—	80	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	R/W Low to Output High-Z	—	35	—	40	
t <sub>OEW</sub>	R/W High to Output Active	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	40	—	40	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

**AC TEST CONDITIONS**

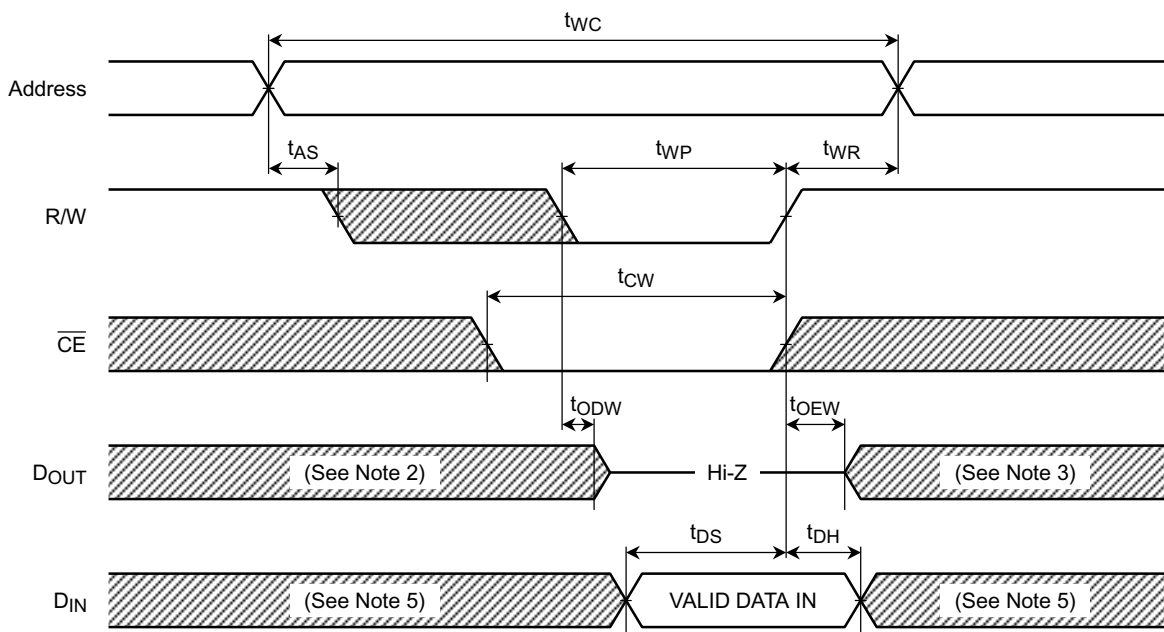
PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	V <sub>DD</sub> - 0.2 V, 0.2 V
Timing measurements	V <sub>DD</sub> × 0.5
Reference level	V <sub>DD</sub> × 0.5
t <sub>R</sub> , t <sub>F</sub>	5 ns

## TIMING DIAGRAMS

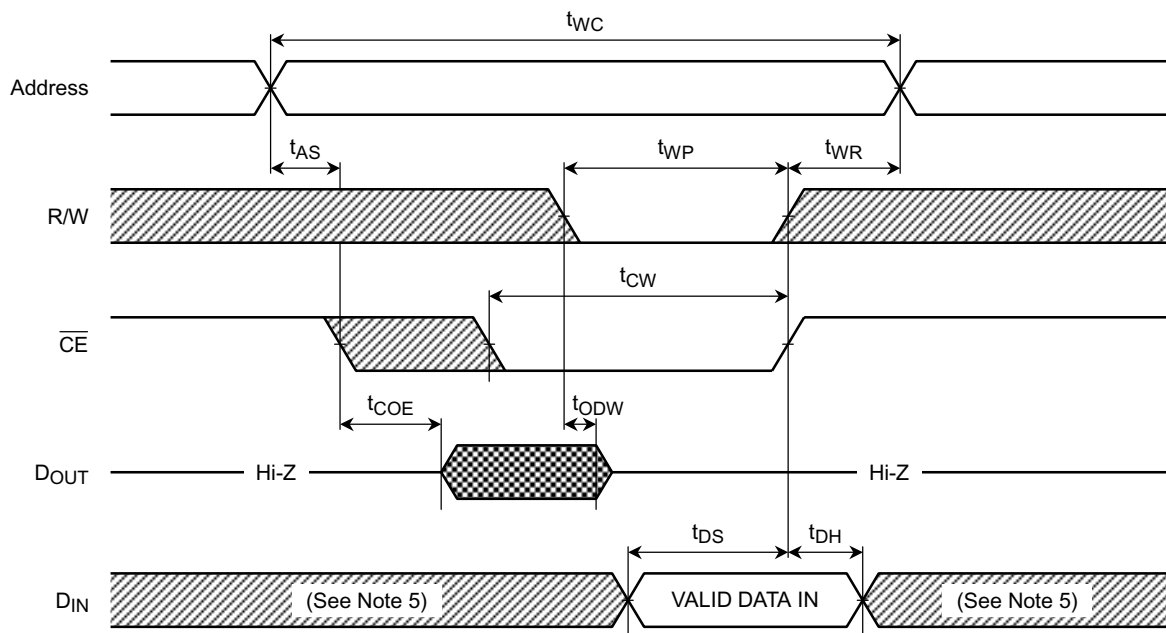
### READ CYCLE (See Note 1)



### WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



## WRITE CYCLE 2 ( $\overline{CE}$ CONTROLLED) (See Note 4)



### Note:

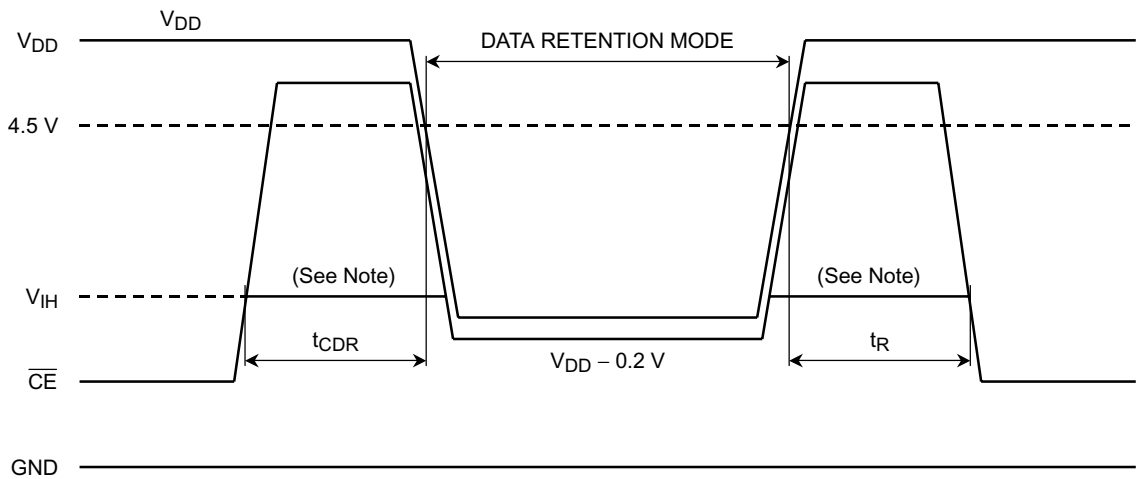
- (1) R/W remains HIGH for the read cycle.
- (2) If  $\overline{CE}$  goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If  $\overline{CE}$  goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

**DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)**

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage			1.5	—	3.6	V
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.0 V	Ta = -40~40°C	—	—	1	μA
			Ta = -40~85°C	—	—	5	
		V <sub>DH</sub> = 3.6 V	Ta = -40~85°C	—	—	7	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time			0	—	—	ns
t <sub>R</sub>	Recovery Time			t <sub>RC</sub> (See Note)	—	—	ns

Note: Read cycle time

**CE CONTROLLED DATA RETENTION MODE**



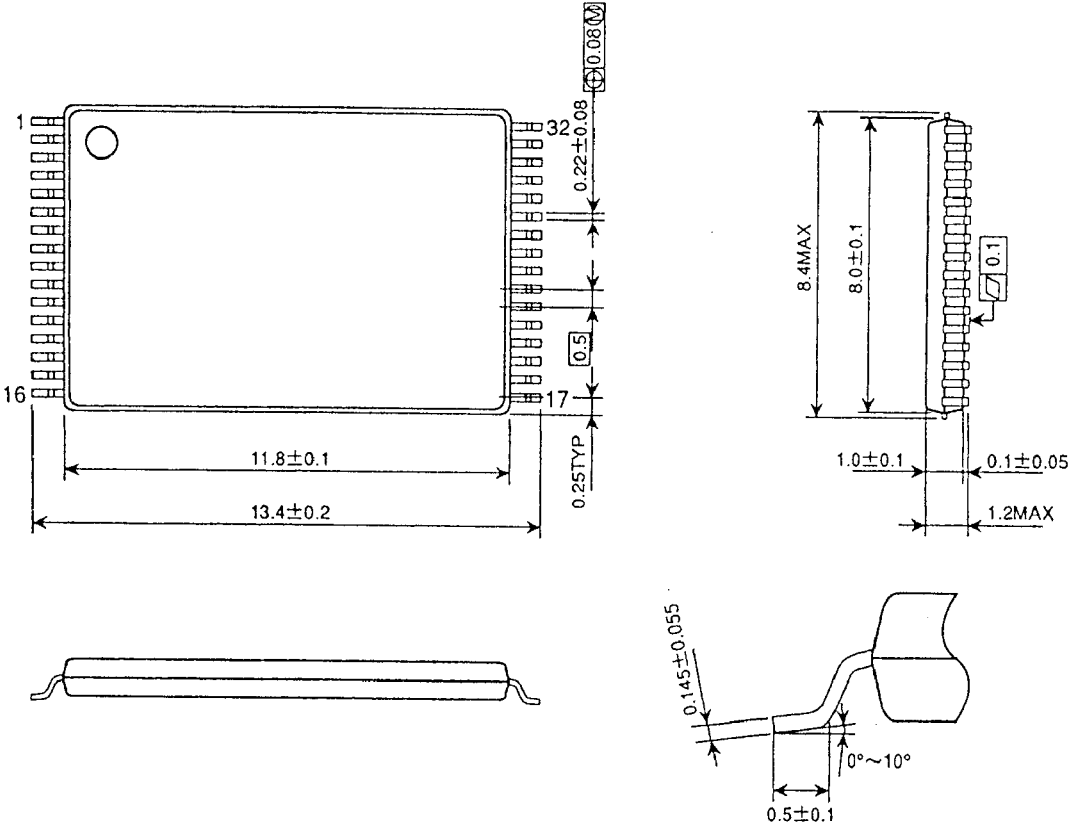
Note: When  $\overline{CE}$  is operating at the V<sub>IH</sub> level (2.2V), the standby current is given by I<sub>DDS1</sub> during the transition of V<sub>DD</sub> from 3.6 to 2.4V.



PACKAGE DIMENSIONS

TSOPI32-P-0.50

Unit: mm



Weight: 0.24 g (typ)

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