

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

## 1,048,576-WORD BY 16-BIT CMOS STATIC RAM

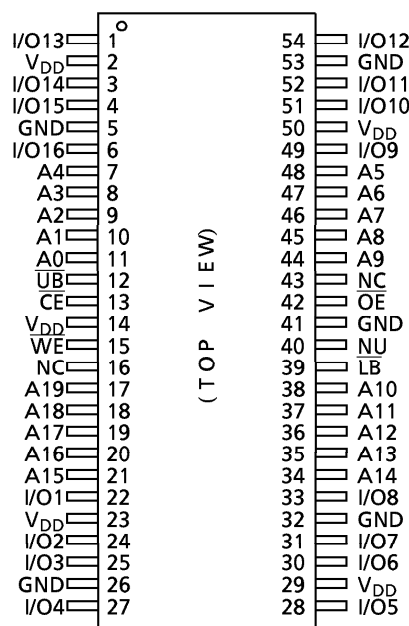
**DESCRIPTION**

The TC55V16100FTI is a 16,777,216-bit high-speed static random access memory (SRAM) organized as 1,048,576 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable ( $\overline{CE}$ ) can be used to place the device in a low-power mode, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control signals ( $\overline{LB}$ ,  $\overline{UB}$ ) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. It guarantees  $-40^{\circ}$  to  $85^{\circ}\text{C}$  operating temperature so it is suitable for use in wide operating temperature system. The TC55V16100FTI is available in plastic 54-pin TSOP with 400mil width for high density surface assembly.

**FEATURES**

- Fast access time(the following are maximum values)
  - TC55V16100FTI-12: 12 ns
  - TC55V16100FTI-15: 15 ns
- Low-power dissipation
- Single power supply voltage :  $3.3\text{V} \pm 0.3\text{V}$
- Fully static operation
- Operating temperature range :  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- All inputs and outputs are LVTTL compatible
- Output buffer control using  $\overline{OE}$
- Data byte control using  $\overline{LB}$  (I/O1 to I/O8) and  $\overline{UB}$  (I/O9 to I/O16)
- Package:
  - TSOP II 54-P-400-0.80B (Weight: 0.55g typ)

Standby : 4mA(max)

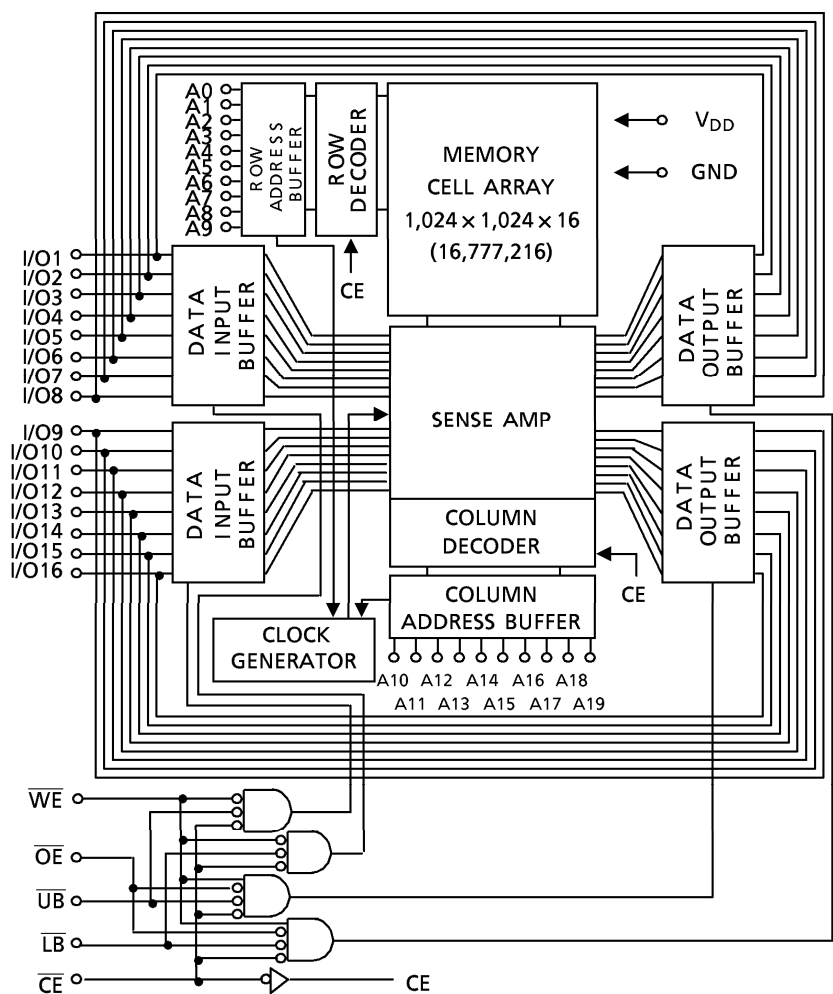
**PIN ASSIGNMENT****PIN NAMES**

|                                   |                          |
|-----------------------------------|--------------------------|
| A0 to A19                         | Address Inputs           |
| I/O1 to I/O16                     | Data Inputs / Outputs    |
| $\overline{CE}$                   | Chip Enable Input        |
| $\overline{WE}$                   | Write Enable Input       |
| $\overline{OE}$                   | Output Enable Input      |
| $\overline{LB}$ , $\overline{UB}$ | Data Byte Control Inputs |
| $V_{DD}$                          | Power (+ 3.3V)           |
| GND                               | Ground                   |
| NC                                | No Connection            |
| NU                                | Not Usable               |

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BLOCK DIAGRAM



MAXIMUM RATINGS

| SYMBOL              | RATING                        | VALUE                             | UNIT |
|---------------------|-------------------------------|-----------------------------------|------|
| V <sub>DD</sub>     | Power Supply Voltage          | - 0.5 to 4.6                      | V    |
| V <sub>IN</sub>     | Input Terminal Voltage        | - 0.5* to 4.6                     | V    |
| V <sub>I/O</sub>    | Input/Output Terminal Voltage | - 0.5* to V <sub>DD</sub> + 0.5** | V    |
| P <sub>D</sub>      | Power Dissipation             | 1.8                               | W    |
| T <sub>solder</sub> | Soldering Temperature (10 s)  | 260                               | °C   |
| T <sub>strg</sub>   | Storage Temperature           | - 65 to 150                       | °C   |
| T <sub>opr</sub>    | Operating Temperature         | - 40 to 100                       | °C   |

\* : -1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
\*\* : V<sub>DD</sub>+1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = - 40° to 85°C)

| SYMBOL          | PARAMETER            | MIN    | TYP | MAX                     | UNIT |
|-----------------|----------------------|--------|-----|-------------------------|------|
| V <sub>DD</sub> | Power Supply Voltage | 3.0    | 3.3 | 3.6                     | V    |
| V <sub>IH</sub> | Input High Voltage   | 2.0    | -   | V <sub>DD</sub> + 0.3** | V    |
| V <sub>IL</sub> | Input Low Voltage    | - 0.3* | -   | 0.8                     | V    |

\* : -1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
\*\* : V<sub>DD</sub>+1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

**DC CHARACTERISTICS** ( $T_a = -40^\circ \text{ to } 85^\circ \text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

| SYMBOL      | PARAMETER                                | TEST CONDITION                                                                                                                          | MIN            | TYP | MAX | UNIT          |
|-------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------|-----|-----|---------------|
| $I_{IL}$    | Input Leakage Current<br>(Except NU pin) | $V_{IN} = 0 \text{ to } V_{DD}$                                                                                                         | -1             | -   | 1   | $\mu\text{A}$ |
| $I_{LO}$    | Output Leakage Current                   | $\overline{CE} = V_{IH} \text{ or } \overline{WE} = V_{IL} \text{ or } \overline{OE} = V_{IH}$<br>$V_{OUT} = 0 \text{ to } V_{DD}$      | -1             | -   | 1   | $\mu\text{A}$ |
| $I_{I(NU)}$ | Input Current<br>(NU pin)                | $V_{IN} = 0 \text{ to } 0.8\text{V}$                                                                                                    | -1             | -   | 20  | $\mu\text{A}$ |
|             |                                          | $V_{IN} = 0 \text{ to } 0.2\text{V}$                                                                                                    | -1             | -   | 1   |               |
| $V_{OH}$    | Output High Voltage                      | $I_{OH} = -2\text{mA}$                                                                                                                  | 2.4            | -   | -   | V             |
|             |                                          | $I_{OH} = -100\mu\text{A}$                                                                                                              | $V_{DD} - 0.2$ | -   | -   |               |
| $V_{OL}$    | Output Low Voltage                       | $I_{OL} = 2\text{mA}$                                                                                                                   | -              | -   | 0.4 |               |
|             |                                          | $I_{OL} = 100\mu\text{A}$                                                                                                               | -              | -   | 0.2 |               |
| $I_{DDO}$   | Operating Current                        | $\overline{CE} = V_{IL}$ , $I_{out} = 0\text{mA}$<br>$\overline{OE} = V_{IH}$<br>Other Inputs = $V_{DD} - 0.2\text{V}$ or $0.2\text{V}$ | tcycle = 12ns  | -   | 420 | mA            |
|             |                                          |                                                                                                                                         | tcycle = 15ns  | -   | 380 |               |
| $I_{DDS1}$  | Standby Current                          | $\overline{CE} = V_{IH}$ , Other Inputs = $V_{IH}$ or $V_{IL}$                                                                          | -              | -   | 105 | mA            |
| $I_{DDS2}$  |                                          | $\overline{CE} = V_{DD} - 0.2\text{V}$<br>Other Inputs = $V_{DD} - 0.2\text{V}$ or $0.2\text{V}$                                        | -              | -   | 4   |               |

**CAPACITANCE** ( $T_a = 25^\circ \text{C}$ ,  $f = 1.0 \text{ MHz}$ )

| SYMBOL    | PARAMETER                | TEST CONDITION         | MAX | UNIT |
|-----------|--------------------------|------------------------|-----|------|
| $C_{IN}$  | Input Capacitance        | $V_{IN} = \text{GND}$  | 6   | pF   |
| $C_{I/O}$ | Input/Output Capacitance | $V_{I/O} = \text{GND}$ | 8   | pF   |

Note: This parameter is periodically sampled and is not 100% tested.

**OPERATING MODE**

| MODE            | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O1 to I/O8   | I/O9 to I/O16  | POWER     |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|-----------|
| Read            | L               | L               | H               | L               | L               | Output         | Output         | $I_{DDO}$ |
|                 |                 |                 |                 | H               | L               | High Impedance | Output         | $I_{DDO}$ |
|                 |                 |                 |                 | L               | H               | Output         | High Impedance | $I_{DDO}$ |
| Write           | L               | x               | L               | L               | L               | Input          | Input          | $I_{DDO}$ |
|                 |                 |                 |                 | H               | L               | High Impedance | Input          | $I_{DDO}$ |
|                 |                 |                 |                 | L               | H               | Input          | High Impedance | $I_{DDO}$ |
| Outputs Disable | L               | H               | H               | x               | x               | High Impedance | High Impedance | $I_{DDO}$ |
|                 | L               | x               | x               | H               | H               |                |                |           |
| Standby         | H               | x               | x               | x               | x               | High Impedance | High Impedance | $I_{DDS}$ |

x: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V.  
You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS (Ta = -40°C to 85°C (Note 1), V<sub>DD</sub> = 3.3V ± 0.3V)

## READ CYCLE

| SYMBOL           | PARAMETER                                       | TC55V16100FTI-12 |     | TC55V16100FTI-15 |     | UNIT |
|------------------|-------------------------------------------------|------------------|-----|------------------|-----|------|
|                  |                                                 | MIN              | MAX | MIN              | MAX |      |
| t <sub>RC</sub>  | Read Cycle Time                                 | 12               | –   | 15               | –   | ns   |
| t <sub>ACC</sub> | Address Access Time                             | –                | 12  | –                | 15  |      |
| t <sub>CO</sub>  | Chip Enable Access Time                         | –                | 12  | –                | 15  |      |
| t <sub>OE</sub>  | Output Enable Access Time                       | –                | 6   | –                | 8   |      |
| t <sub>BA</sub>  | Upper Byte, Lower Byte Access Time              | –                | 6   | –                | 8   |      |
| t <sub>OH</sub>  | Output Data Hold Time from Address Change       | 3                | –   | 3                | –   |      |
| t <sub>COE</sub> | Output Enable Time from Chip Enable             | 3                | –   | 3                | –   |      |
| t <sub>OEE</sub> | Output Enable Time from Output Enable           | 1                | –   | 1                | –   |      |
| t <sub>BE</sub>  | Output Enable Time from Upper Byte, Lower Byte  | 1                | –   | 1                | –   |      |
| t <sub>COD</sub> | Output Disable Time from Chip Enable            | –                | 7   | –                | 8   |      |
| t <sub>ODO</sub> | Output Disable Time from Output Enable          | –                | 7   | –                | 8   |      |
| t <sub>BD</sub>  | Output Disable Time from Upper Byte, Lower Byte | –                | 7   | –                | 8   |      |

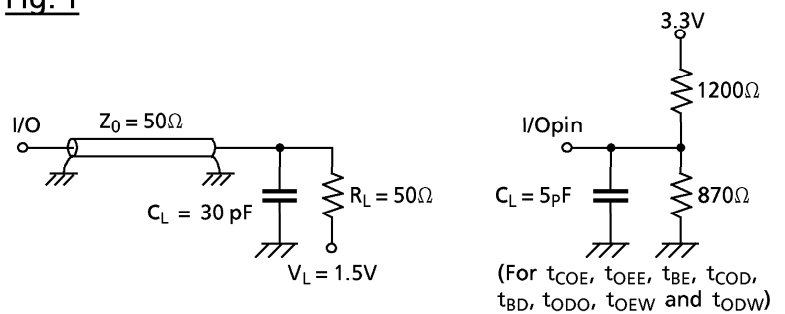
## WRITE CYCLE

| SYMBOL                      | PARAMETER                                     | TC55V16100FTI-12 |     | TC55V16100FTI-15 |     | UNIT |
|-----------------------------|-----------------------------------------------|------------------|-----|------------------|-----|------|
|                             |                                               | MIN              | MAX | MIN              | MAX |      |
| t <sub>WC</sub>             | Write Cycle Time                              | 12               | –   | 15               | –   | ns   |
| t <sub>WP</sub>             | Write Pulse Width                             | 8                | –   | 10               | –   |      |
| t <sub>CW</sub>             | Chip Enable to End of Write                   | 9                | –   | 11               | –   |      |
| t <sub>BW</sub>             | Upper Byte, Lower Byte Enable to End of Write | 9                | –   | 11               | –   |      |
| t <sub>AW</sub>             | Address Valid to End of Write                 | 9                | –   | 11               | –   |      |
| t <sub>AS</sub>             | Address Setup Time                            | 0                | –   | 0                | –   |      |
| t <sub>WR</sub>             | Write Recovery Time                           | 0                | –   | 0                | –   |      |
| t <sub>DS</sub>             | Data Setup Time                               | 7                | –   | 8                | –   |      |
| t <sub>DH</sub>             | Data Hold Time                                | 0                | –   | 0                | –   |      |
| t <sub>OE<sub>W</sub></sub> | Output Enable Time from Write Enable          | 1                | –   | 1                | –   |      |
| t <sub>OD<sub>W</sub></sub> | Output Disable Time from Write Enable         | –                | 7   | –                | 8   |      |

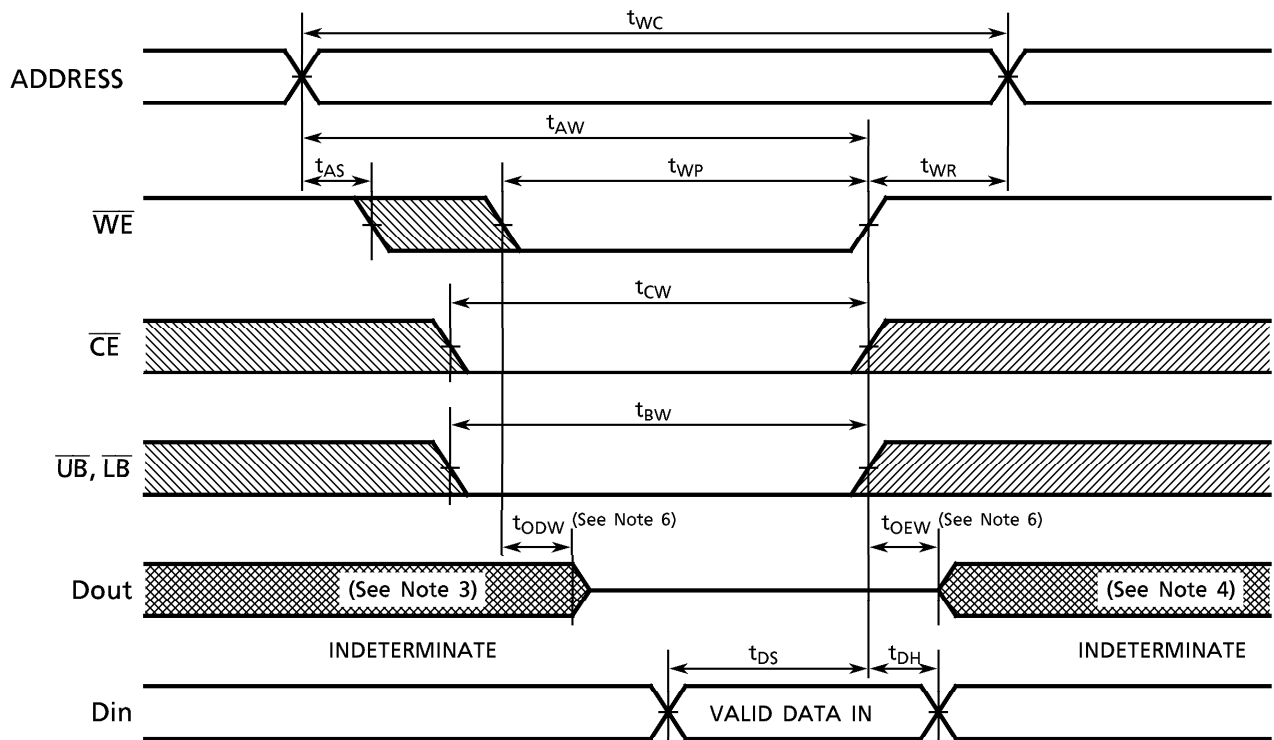
## AC TEST CONDITIONS

|                                           |           |
|-------------------------------------------|-----------|
| Input Pulse Level                         | 3.0V/0.0V |
| Input Pulse Rise and Fall Time            | 2ns       |
| Input Timing Measurement Reference Level  | 1.5V      |
| Output Timing Measurement Reference Level | 1.5V      |
| Output Load                               | Fig. 1    |

Fig. 1

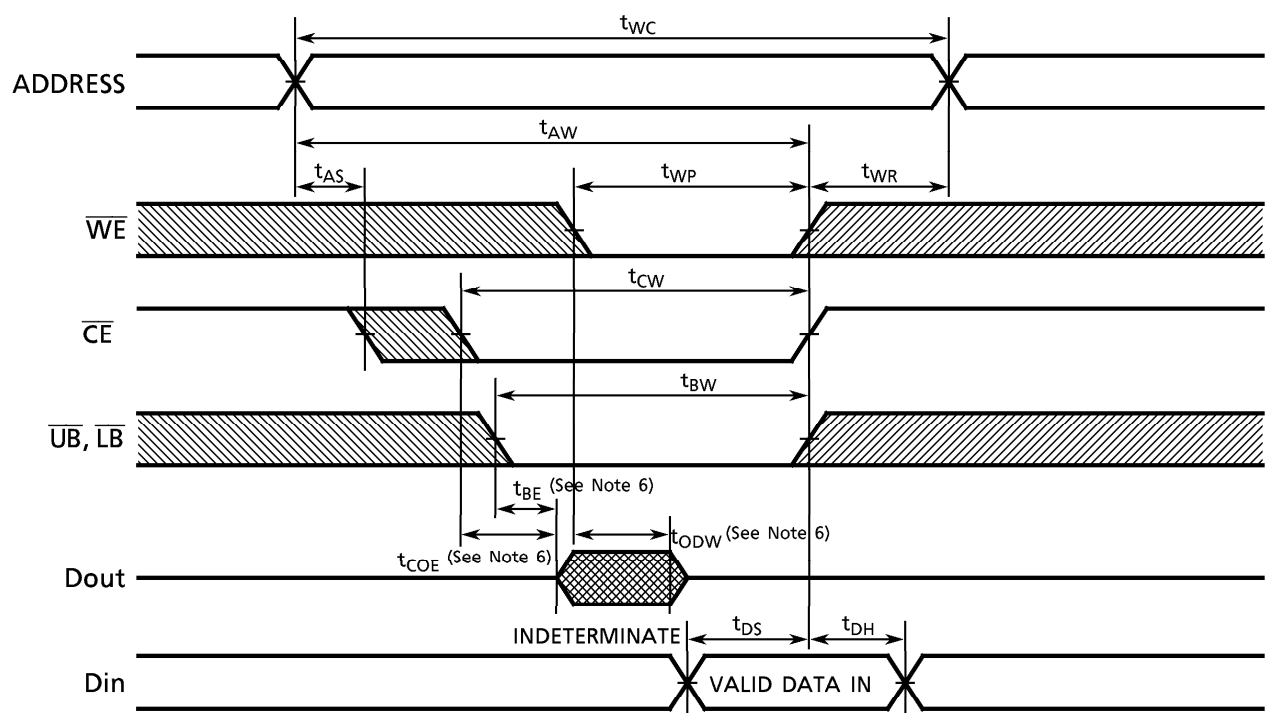


**READ CYCLE** (See Note 2)

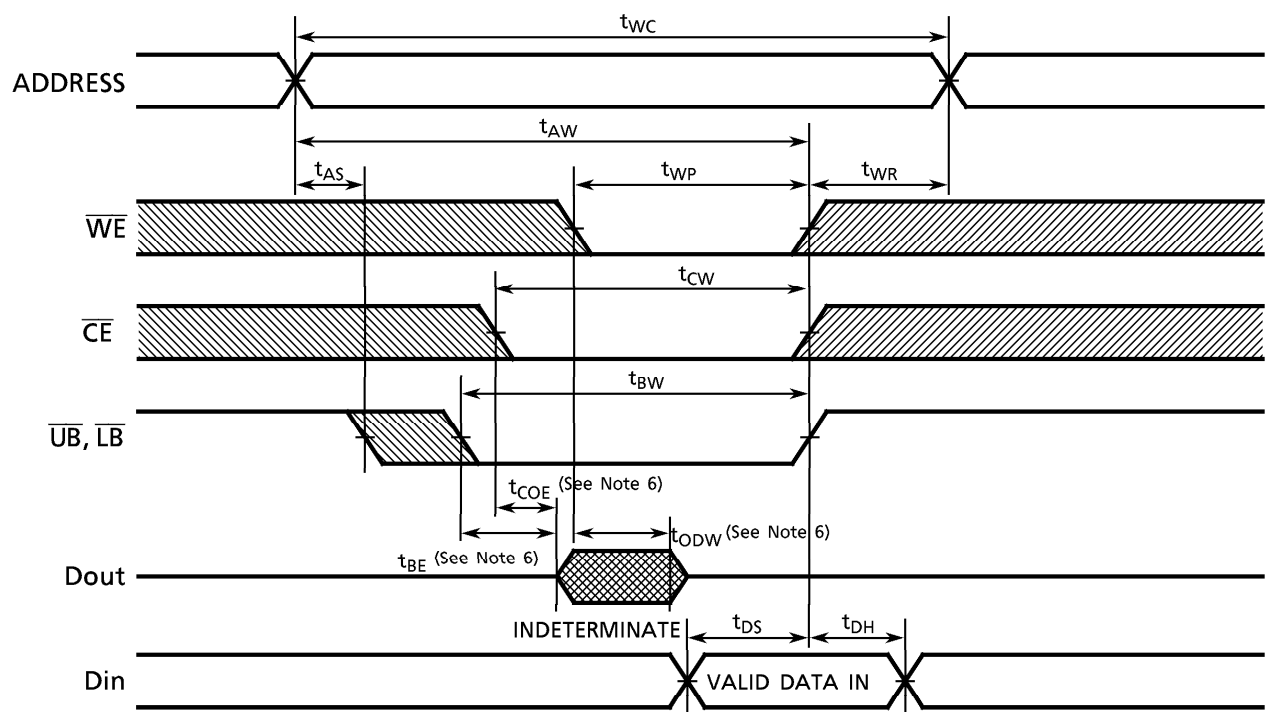


WRITE CYCLE 2 ( $\overline{\text{CE}}$  CONTROLLED) (See Note 5)

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WRITE CYCLE 3 ( $\overline{\text{UB}}, \overline{\text{LB}}$  CONTROLLED) (See Note 5)



Note: (1) Operating temperature ( $T_a$ ) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2)  $\overline{WE}$  remains HIGH for the Read Cycle.

(3) If  $\overline{CE}$  goes LOW coincident with or after  $\overline{WE}$  goes LOW, the outputs will remain at high impedance.

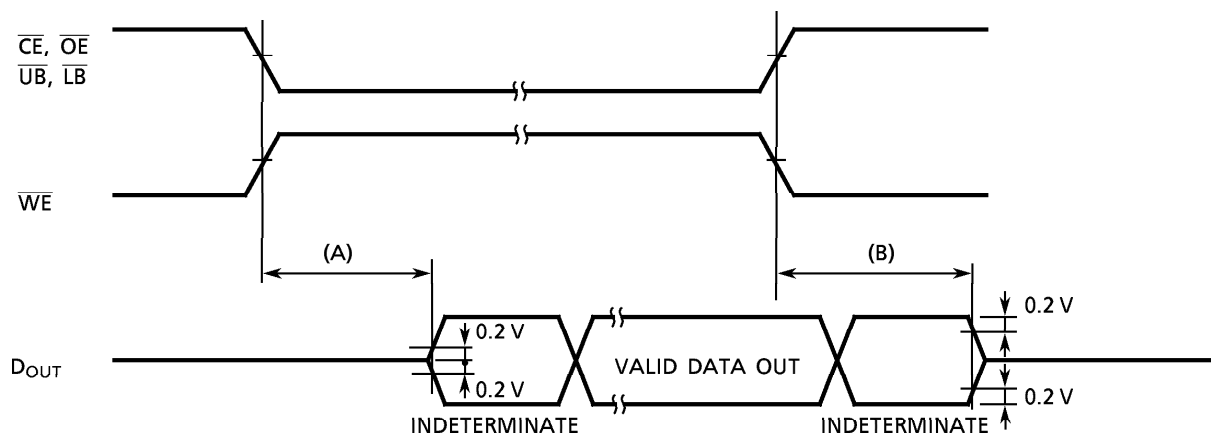
(4) If  $\overline{CE}$  goes HIGH coincident with or before  $\overline{WE}$  goes HIGH, the outputs will remain at high impedance.

(5) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A)  $t_{COE}$ ,  $t_{OEE}$ ,  $t_{BE}$ ,  $t_{OEw}$  ..... Output Enable Time

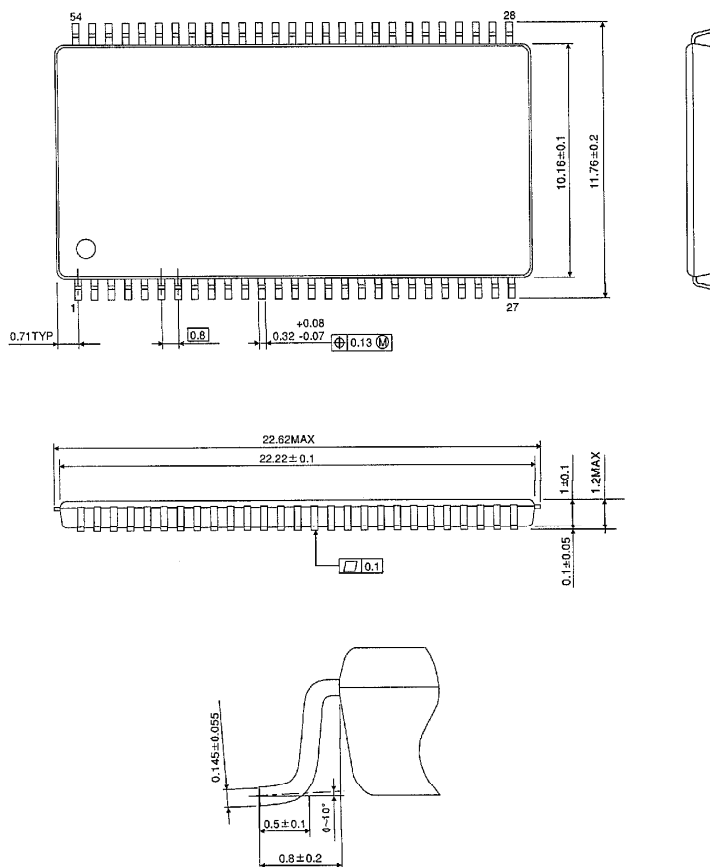
(B)  $t_{COD}$ ,  $t_{ODO}$ ,  $t_{BD}$ ,  $t_{ODW}$  ..... Output Disable Time



## PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 54-P-400-0.80B)

Unit in mm



Weight : 0.55g (Typ)