

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257CPL is a 262,144 bit CMOS static random access memory organized as 32,768 words by 8 bits and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns.

When $\overline{CE}$ is a logical high, the device is placed in a low power standby mode in which the standby current is 2 μ A at room temperature. The TC55257CPL has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, while an output enable input ($\overline{OE}$) provides fast memory access. The TC55257CPL is suitable for use in microprocessor systems where high speed, low power, and battery backup are required.

The TC55257CPL is offered in a standard dual-in-line 28-pin plastic package (0.6/0.3 inch width), a small outline plastic package, and a thin small outline plastic package (forward type, reverse type).

Features

- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 100 μ A (max.)
- Single 5V power supply
- Access time (max.)

	TC55257CPL/CFL/CSPL/CFTL/CTRL		
	-70	-85	-10
Access Time	70ns	85ns	100ns
$\overline{CE}$ Access Time	70ns	85ns	100ns
$\overline{OE}$ Access Time	35ns	45ns	50ns

- Power down feature: $\overline{CE}$
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs TTL compatible
- Package
 - TC55257CPL : DIP28-P-600
 - TC55257CFL : SOP28-P-450
 - TC55257CSPL : DIP28-P-300B
 - TC55257CFTL : TSOP28-P
 - TC55257CTRL : TSOP28-P-A

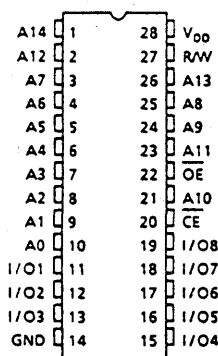
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

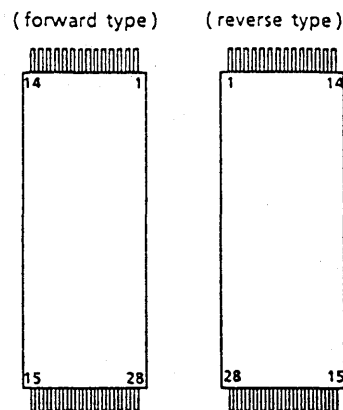
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A ₁₀

Pin Connection (Top View)

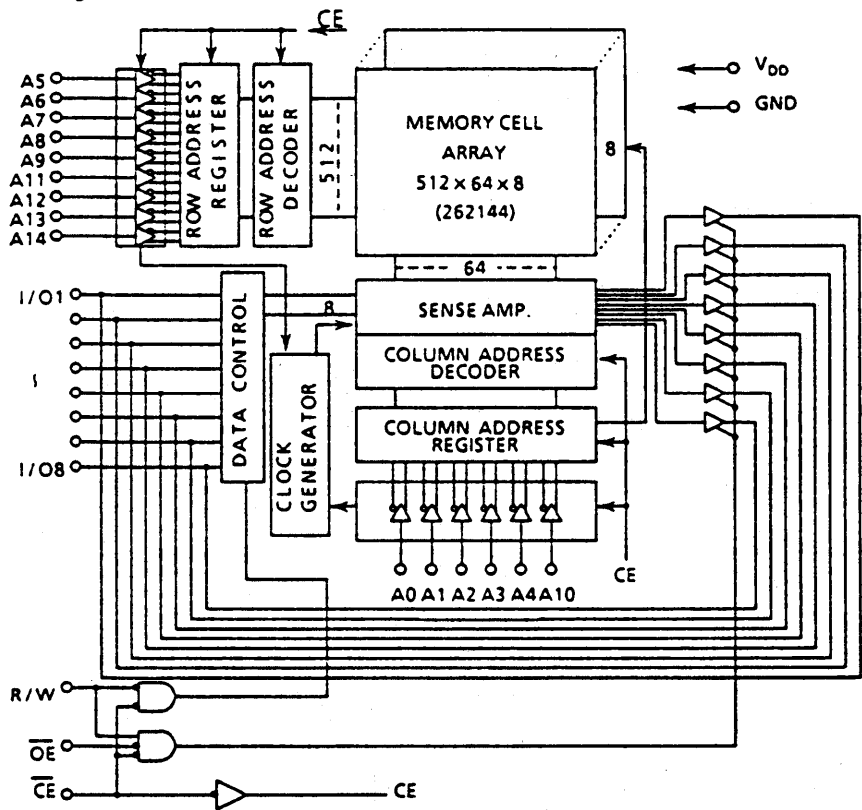
o 28 PIN DIP & SOP



o 28 PIN TSOP



Block Diagram



Operating Mode

MODE \ PIN	CE	OE	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	High-Z	I _{DDO}
Standby	H	*	*	High-Z	I _{DDS}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.8/0.6**	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	0 ~ 70	°C

* -3.0V with a pulse width of 50ns

** Package dependent: 0.6 inch 1.0W, 0.3 inch 0.8W, 0.45 inch 0.6W

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	

* -3.0V with a pulse width of 50ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{LO}	Output Leakage Current	CE = V _{IH} or R/W = V _{IL} or OE = V _{IH} V _{OUT} = 0 ~ V _{DD}		—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4V		-1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V		4.0	—	—	mA
I _{DDO1}	Operating Current	CE = V _{IL} R/W = V _{IH} Other Input = V _{IH} /V _{IL} I _{OUT} = 0mA	t _{cycle} = 1μs	—	10	—	mA
			t _{cycle} = Min. cycle	—	—	70	
I _{DDO2}		CE = 0.2V R/W = V _{DD} - 0.2V Other Input = V _{DD} - 0.2V/0.2V I _{OUT} = 0mA	t _{cycle} = 1μs	—	5	—	
			t _{cycle} = Min. cycle	—	—	60	
I _{DDS1}	Standby Current	CE = V _{IH}		—	—	3	mA
I _{DDS2}		CE = V _{DD} - 0.2V V _{DD} = 2.0V ~ 5.5V	Ta = 0 ~ 70°C	—	—	100	μA
			Ta = 25°C	—	2	—	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
		-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t _{ACC}	Address Access Time	—	70	—	85	—	100	
t _{CO}	$\overline{CE}$ Access Time	—	70	—	85	—	100	
t _{OE}	Output Enable to Output in Valid	—	35	—	45	—	50	
t _{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	—	10	—	10	—	
t _{OOE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t _{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	—	25	—	30	—	50	
t _{ODO}	Output Enable to Output in High-Z	—	25	—	30	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	10	—	

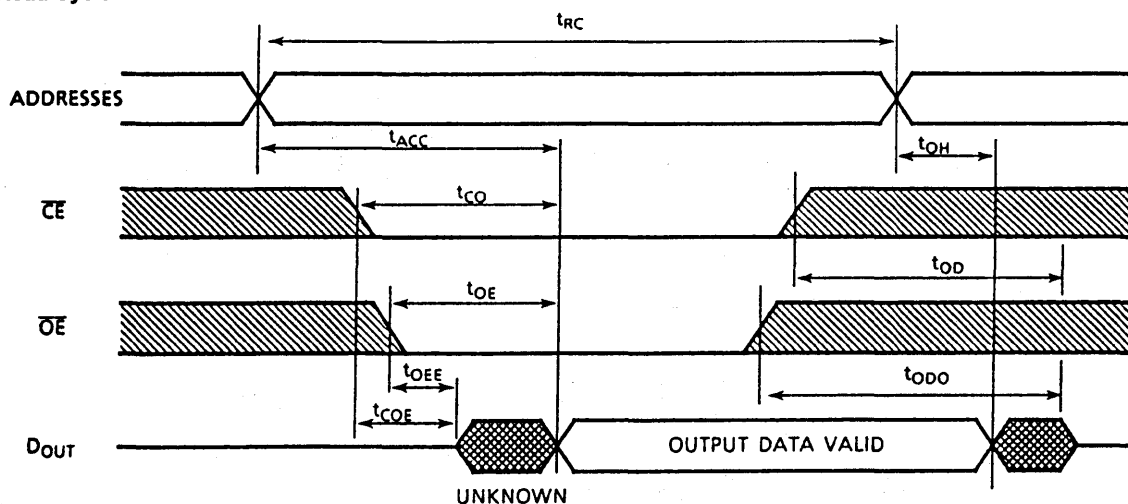
Write Cycle

		TC55257CPL/CFL/CSPL/CFTL/CTRL						UNIT
SYMBOL	PARAMETER	-70		-85		-10		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t _{WP}	Write Pulse Width	50	—	60	—	70	—	
t _{CW}	Chip Selection to End of Write	60	—	65	—	90	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{ODW}	R/W to Output in High-Z	—	25	—	30	—	50	
t _{OEW}	R/W to Output in Low-Z	5	—	5	—	5	—	
t _{DS}	Data Setup Time	30	—	40	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	1 TTL Gate and C _L = 100pF

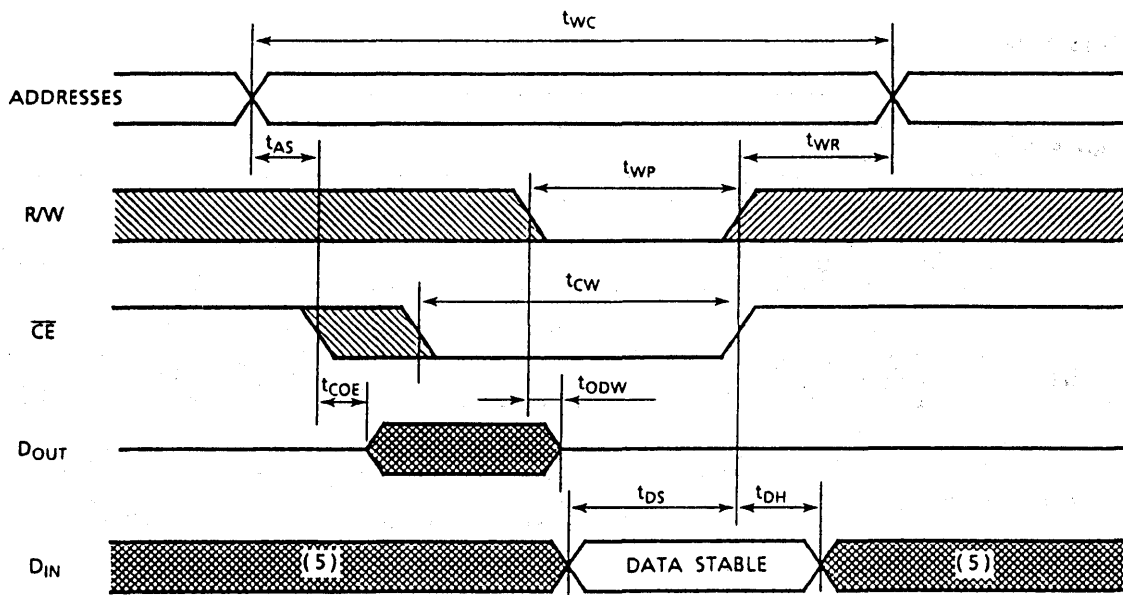
Read Cycle ⁽¹⁾



The diagram illustrates the timing relationships for a memory access cycle. The signals and their timing parameters are as follows:

- ADDRESSES:** The address bus signal. The total duration of the address being valid is t_{WC} (Write Cycle time).
- R/W:** The Read/Write control signal. It transitions from high to low for a write operation. The setup time before the address is t_{AS} . The pulse width is t_{WP} . The recovery time after the address is t_{WR} .
- $\overline{CE}$:** The Chip Enable signal. It transitions from high to low. The setup time before the address is t_{CW} . It returns to high after the address is no longer valid.
- D_{OUT} :** The data output signal. It becomes valid at the start of the write cycle. The output delay time is t_{ODW} . It becomes invalid at the end of the write cycle. The output enable time is t_{OE} .
- D_{IN} :** The data input signal. It becomes valid at the start of the write cycle. The input delay time is t_{DS} . It becomes invalid at the end of the write cycle. The input hold time is t_{DH} .

The diagram also shows the data being written (labeled (2)) and the data being read (labeled (3)). The data is stable during the write cycle (labeled (5)).

Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)

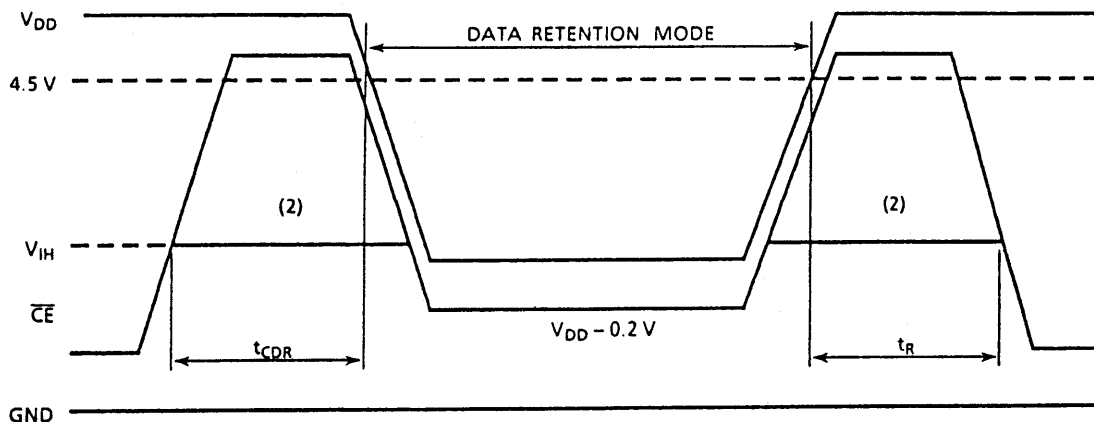
Notes:

1. R/W is high for read cycles.
2. If the $\overline{\text{CE}}$ low transition occurs coincident with or after the R/W low transition, outputs remain in a high impedance state.
3. If the $\overline{\text{CE}}$ high transition occurs coincident with or prior to the R/W high transition, outputs remain in a high impedance state.
4. If $\overline{\text{OE}}$ is high during a write cycle, the outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; therefore input signals of opposite phase must not be applied.

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DH} = 3.0V$	—	50	μA
		$V_{DH} = 5.5V$	—	100	
t_{CDR}	Chip Deselect to Data Retention Mode	0	—	—	ns
t_R	Recovery Time	$t_{RC(1)}$	—	—	

Note (1): Read Cycle Time

 $\overline{CE}$ Controlled Data Retention ModeNote (2): If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.