2,048 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5516AP/-2, TC5516APL/-2
TC5516AF/-2, TC5516AFL/-2

DESCRIPTION

The TC5516AP/AF is a 16384-bit static random access memory organized as 2048 words by 8 bit using CMOS technology, ad operates from a single 5 volt supply.

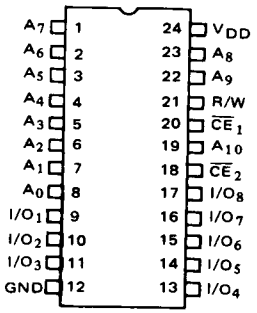
The TC5516AP/AF is featured by two chip enable inputs, that is, $\overline{CE}_1$ for fast memory access and $\overline{CE}_2$ for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for nonvolatility are required. Furthermore the TC5516APL/AFL guaranteed a standby current equal to or less than 1μA at 60℃ ambient temperature is avialable.

The TC5516AP is also featured by pin compatibility with 2716 type EPROM. This means that the TC5516AP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

FEATURES

- Standby Current
  - 0.2μA (Max.) at Ta = 25°C
  - 1.0μA (Max.) at Ta = 60°C
  - } TC5516APL/AFL
  - 1.0μA (Max.) at Ta = 25°C
  - 5.0μA (Max.) at Ta = 60°C
  - } TC5516AP/AF
- Low Power Dissipation : 200mW (Typ.) Operating
- Single 5V Power Supply : 5V ± 10%
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation
- Access Time
  - 250ns (Max.): TC5516AP/APL/AF/AFL
  - 200ns (Max.): TC5516AP-2/APL-2/AF-2/AFL-2
- Two Chip Enable ($\overline{CE}_1$, $\overline{CE}_2$) for Simple Memory Expansion and Battery Back Up.
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  - Plastic DIP : TC5516AP/APL
  - Plastic FP : TC5516AF/AFL

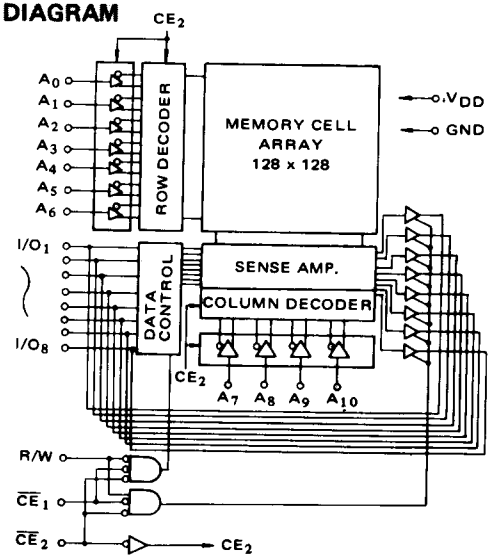
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD} + 0.3
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD} + 0.3
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}_2 = V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}_2$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE}_2 = V_{DD} - 0.5V$, V_{DD} = 2 ~ 5.5V	TC5516APL/AFL	Ta = 25°C	–	0.005	0.2	μA
				Ta = 60°C	–	–	1.0	
			TC5516AP/AF	Ta = 25°C	–	0.05	1.0	
				Ta = 60°C	–	–	5.0	
				Ta = 85°C	–	–	30	
I_{DDO1}	Operating Current	$\overline{CE}_2$ = OV, $V_{IN} = V_{IH}/V_{IL}$, I_{OUT} = 0mA			–	40	70	mA
I_{DDO2}		$\overline{CE}_2$ = OV, $V_{IN} = V_{DD}$/GND, I_{OUT} = 0mA			–	30	55	

Note: Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ±10%)

- **Read Cycle**

SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	250	–	ns
t_{ACC}	Access Time	–	200	–	250	ns
t_{CO1}	$\overline{CE}_1$ to Output Valid	–	100	–	100	ns
t_{CO2}	$\overline{CE}_2$ to Output Valid	–	200	–	250	ns
t_{COE}	$\overline{CE}_1$ or $\overline{CE}_2$ to Output Active	10	–	10	–	ns
t_{OD}	Output High-Z form Deselection	–	80	–	80	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	ns

- **Write Cycle**

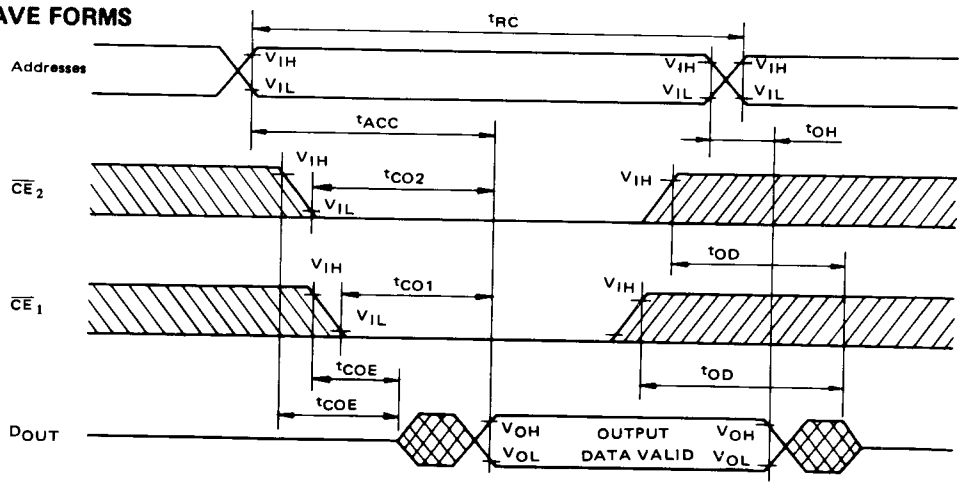
SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	250	–	ns
t_{WP}	Write Pulse Width	160	–	200	–	ns
t_{AW}	Addresss Set-Up Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	ns
t_{ODW}	Output High-Z from R/W	–	80	–	80	ns
t_{OEW}	Output Active from R/W	10	–	10	–	ns
t_{DS}	Data Set Up Time	80	–	120	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns

A.C. TEST CONDITIONS

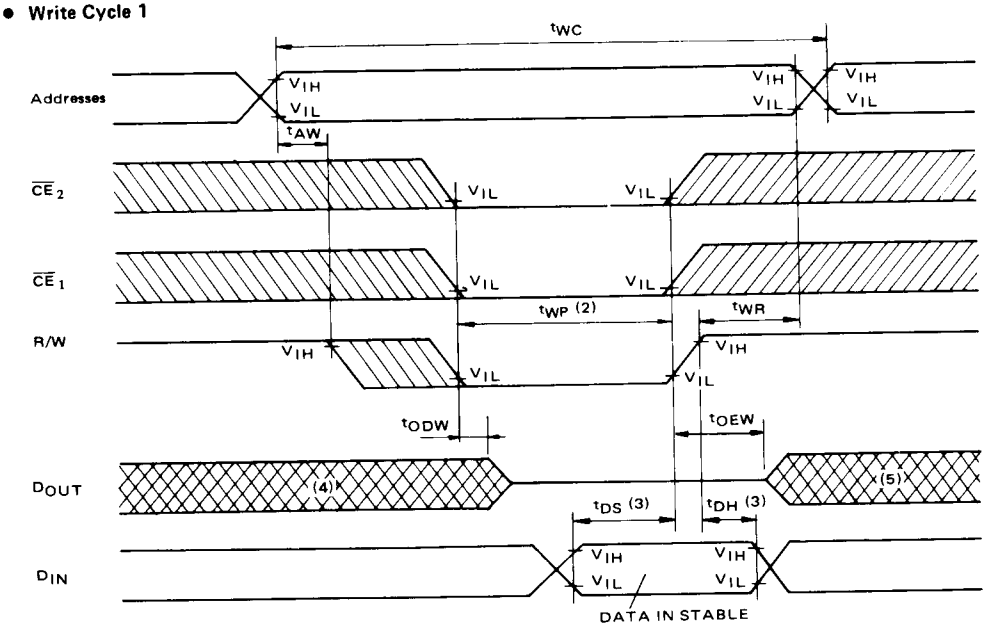
Output Load : 100 pF + ITTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10ns

TIMING WAVE FORMS

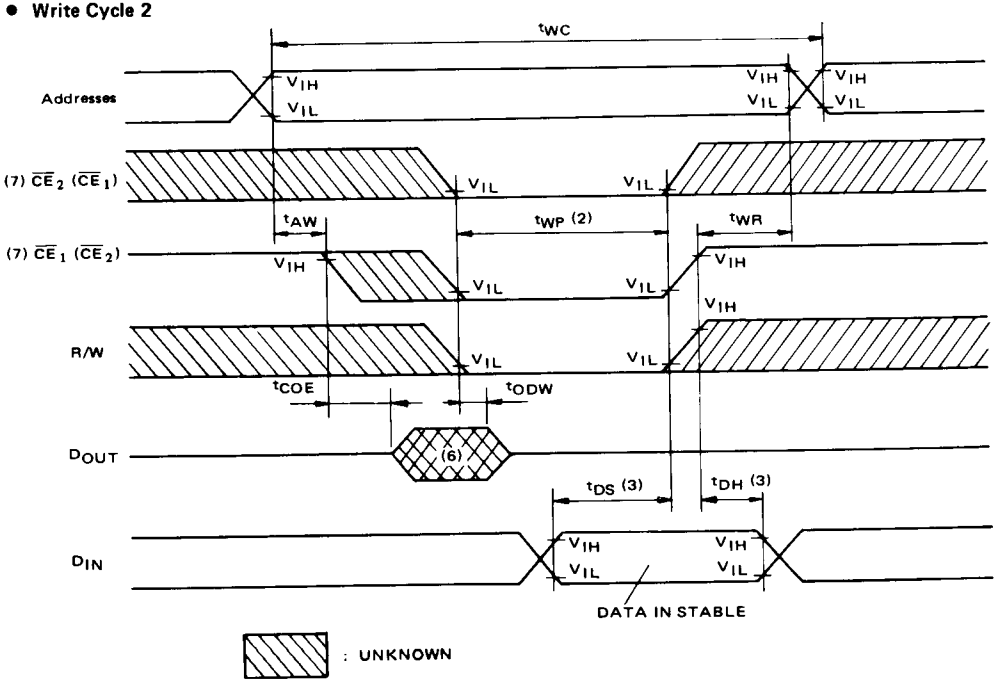
- **Read Cycle**



- **Write Cycle 1**



- **Write Cycle 2**

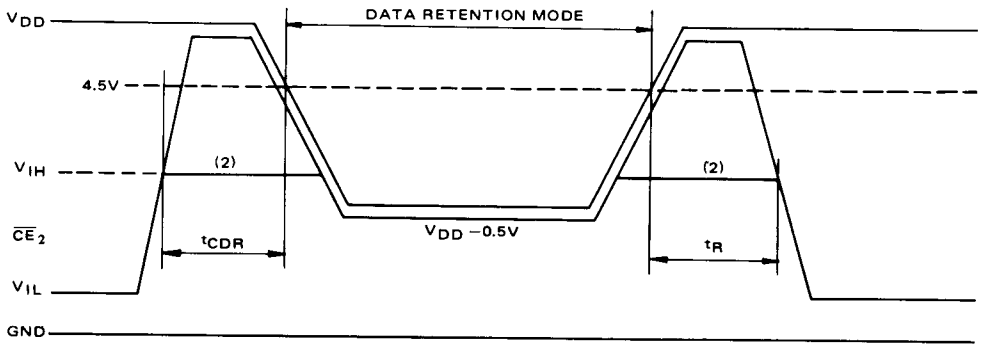


NOTE: (1) R/W is high for a Read Cycle.
(2) t_{WP} is specified as the logical "AND" of $\overline{CE}_1$, $\overline{CE}_2$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going low to the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
(3) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
(4) If the $\overline{CE}_1$, or $\overline{CE}_2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(5) If the $\overline{CE}_1$ or $\overline{CE}_2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}_1$ or $\overline{CE}_2$ low transition, the output buffers remain in a high impedance state in this period.
(7) A write occurs during the overlap of a low $\overline{CE}_1$, low $\overline{CE}_2$ and low R/W. In write cycle 2, write is controlled by either $\overline{CE}_1$ or $\overline{CE}_2$.

DATA RETENTION CHARACTERISTICS (Ta = −30 ~ 85°C)

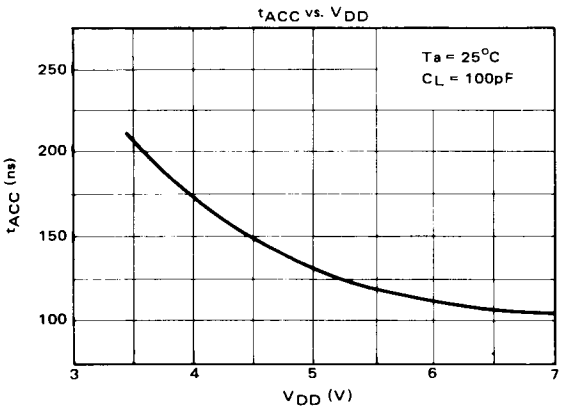
SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5516APL/AFL	Ta = 25°C	–	0.005	0.2	μA
			Ta = 60°C	–	–	1.0	
		TC5516AP/AF	Ta = 25°C	–	0.05	1.0	
			Ta = 60°C	–	–	5.0	
			Ta = 85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recover Time			t_{RC} (1)	–	–	μs

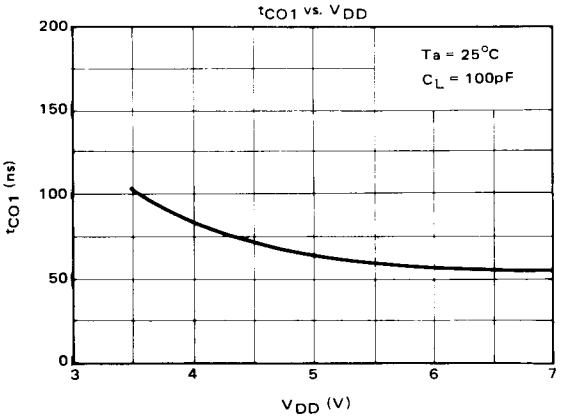
Note (1) t_{RC} : Read Cycle Time.

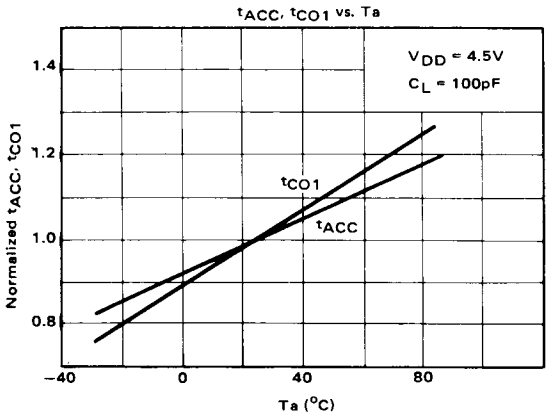


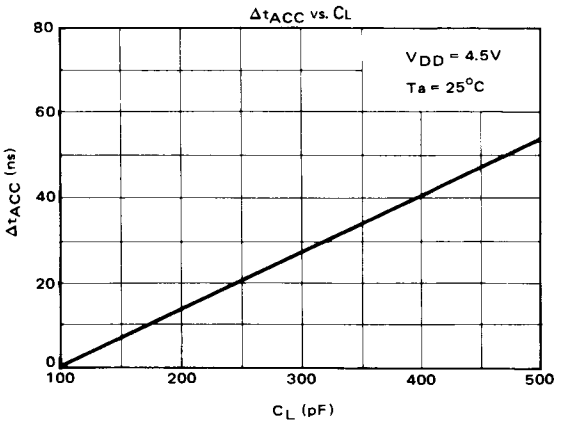
Note: (2) If the V_{IH} level of $\overline{CE}_2$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{SSD1} current flows. (Refer to D.C. CHARACTERISTICS or TYPICAL CHARACTERISTIC FIGURES.)

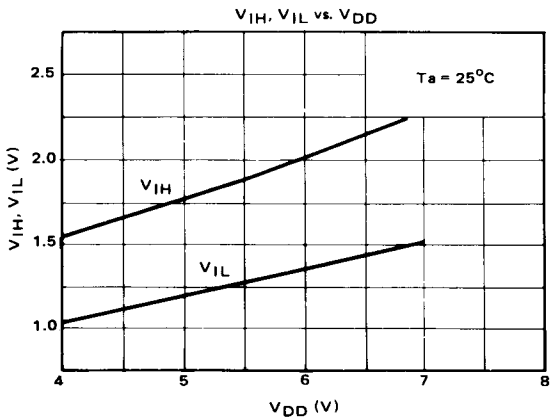
TYPICAL CHARACTERISTICS

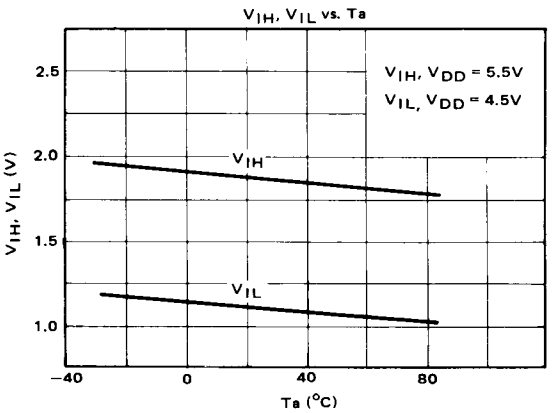


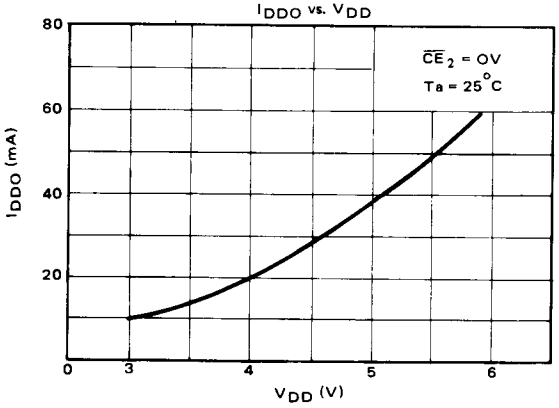


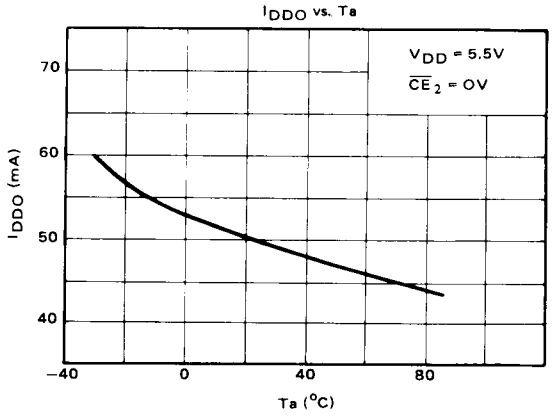


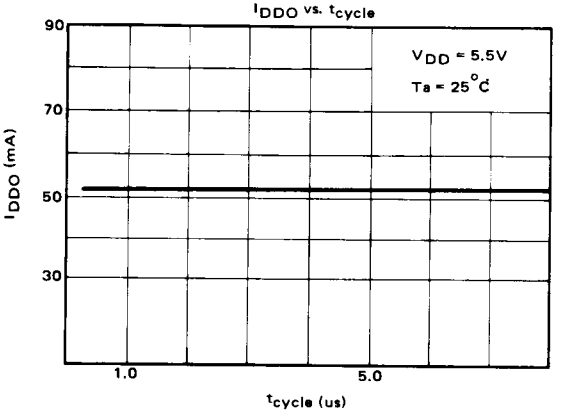


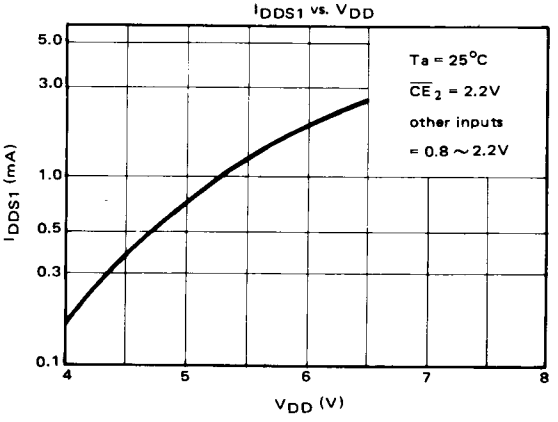


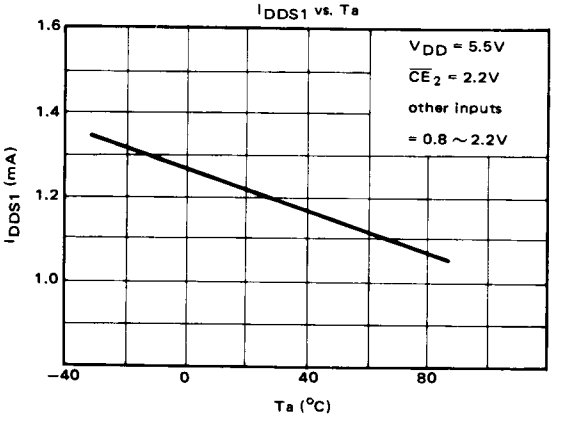


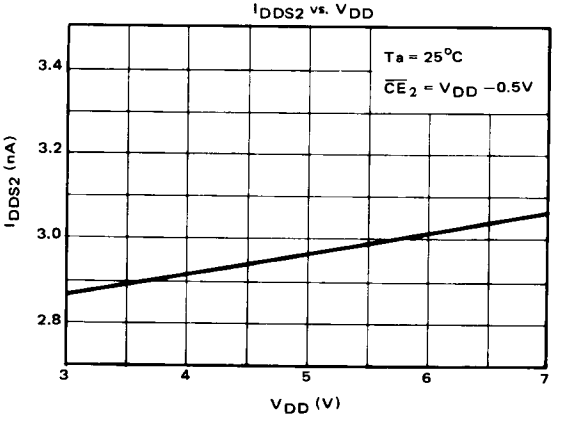

I_{DDO} vs. V_{DD}
$\overline{CE}_2$ = OV
Ta = 25°C
I_{DDO} (mA)
80
60
40
20
0
3
4
5
6
V_{DD} (V)

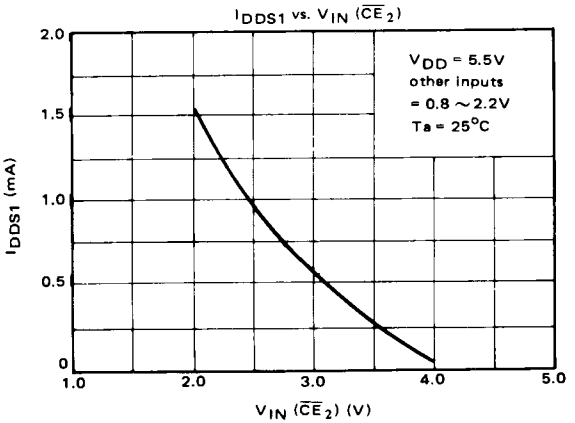

I_{DDO} vs. Ta
V_{DD} = 5.5V
$\overline{CE}_2$ = OV
I_{DDO} (mA)
70
60
50
40
−40
0
40
80
Ta (°C)

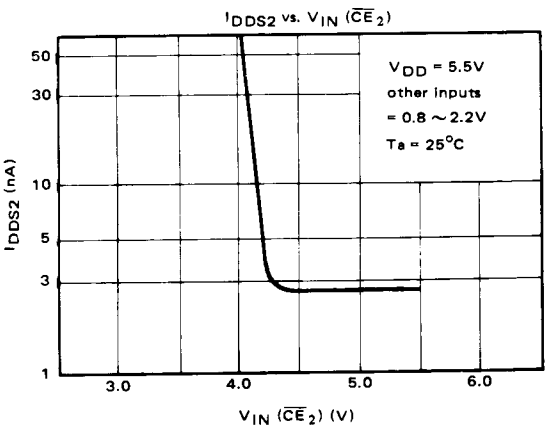

I_{DDO} vs. t_{cycle}
V_{DD} = 5.5V
Ta = 25°C
I_{DDO} (mA)
90
70
50
30
1.0
5.0
t_{cycle} (us)

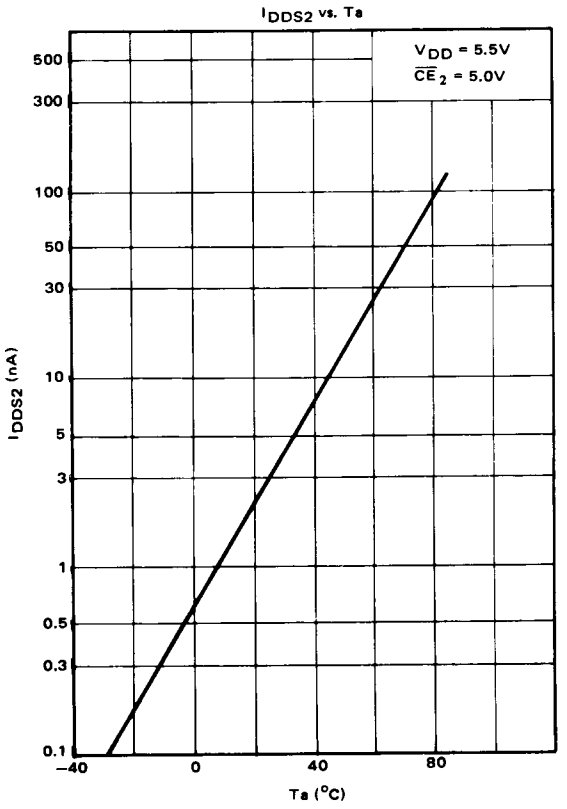

I_{DDS1} vs. V_{DD}
Ta = 25°C
$\overline{CE}_2$ = 2.2V
other inputs
= 0.8 ~ 2.2V
I_{DDS1} (mA)
5.0
3.0
1.0
0.5
0.3
0.1
4
5
6
7
8
V_{DD} (V)

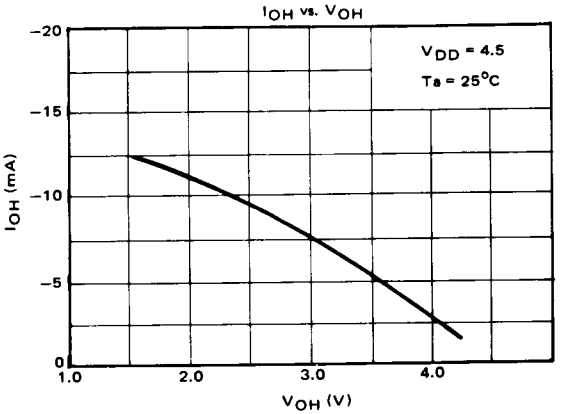

I_{DDS1} vs. Ta
V_{DD} = 5.5V
$\overline{CE}_2$ = 2.2V
other inputs
= 0.8 ~ 2.2V
I_{DDS1} (mA)
1.6
1.4
1.2
1.0
−40
0
40
80
Ta (°C)

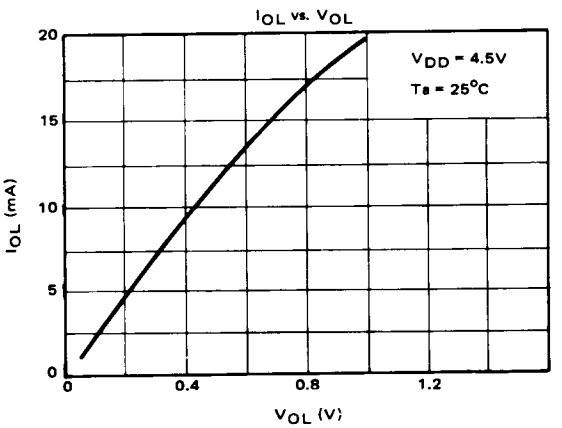

I_{DDS2} vs. V_{DD}
Ta = 25°C
$\overline{CE}_2$ = V_{DD} −0.5V
I_{DDS2} (nA)
3.4
3.2
3.0
2.8
3
4
5
6
7
V_{DD} (V)


I_{DDS1} vs. V_{IN} ($\overline{CE}_2$)
V_{DD} = 5.5V
other inputs
= 0.8 ~ 2.2V
Ta = 25°C
I_{DDS1} (mA)
V_{IN} ($\overline{CE}_2$) (V)


I_{DDS2} vs. V_{IN} ($\overline{CE}_2$)
V_{DD} = 5.5V
other inputs
= 0.8 ~ 2.2V
Ta = 25°C
I_{DDS2} (nA)
V_{IN} ($\overline{CE}_2$) (V)

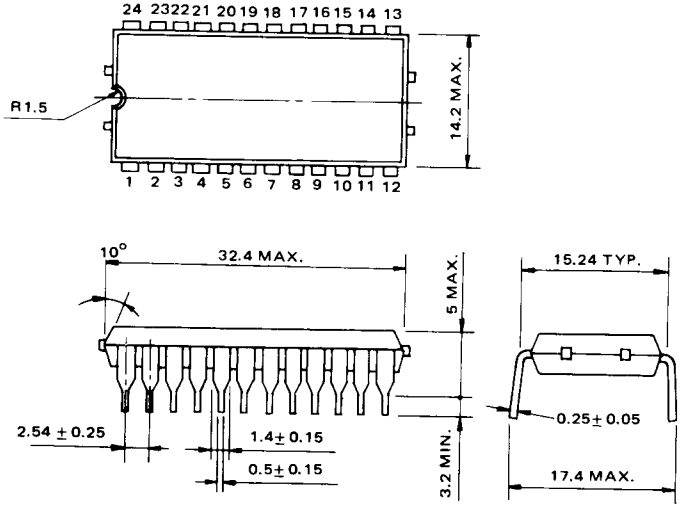

I_{DDS2} vs. Ta
V_{DD} = 5.5V
$\overline{CE}_2$ = 5.0V
I_{DDS2} (nA)
Ta (°C)


I_{OH} vs. V_{OH}
V_{DD} = 4.5
Ta = 25°C
I_{OH} (mA)
V_{OH} (V)


I_{OL} vs. V_{OL}
V_{DD} = 4.5V
Ta = 25°C
I_{OL} (mA)
V_{OL} (V)

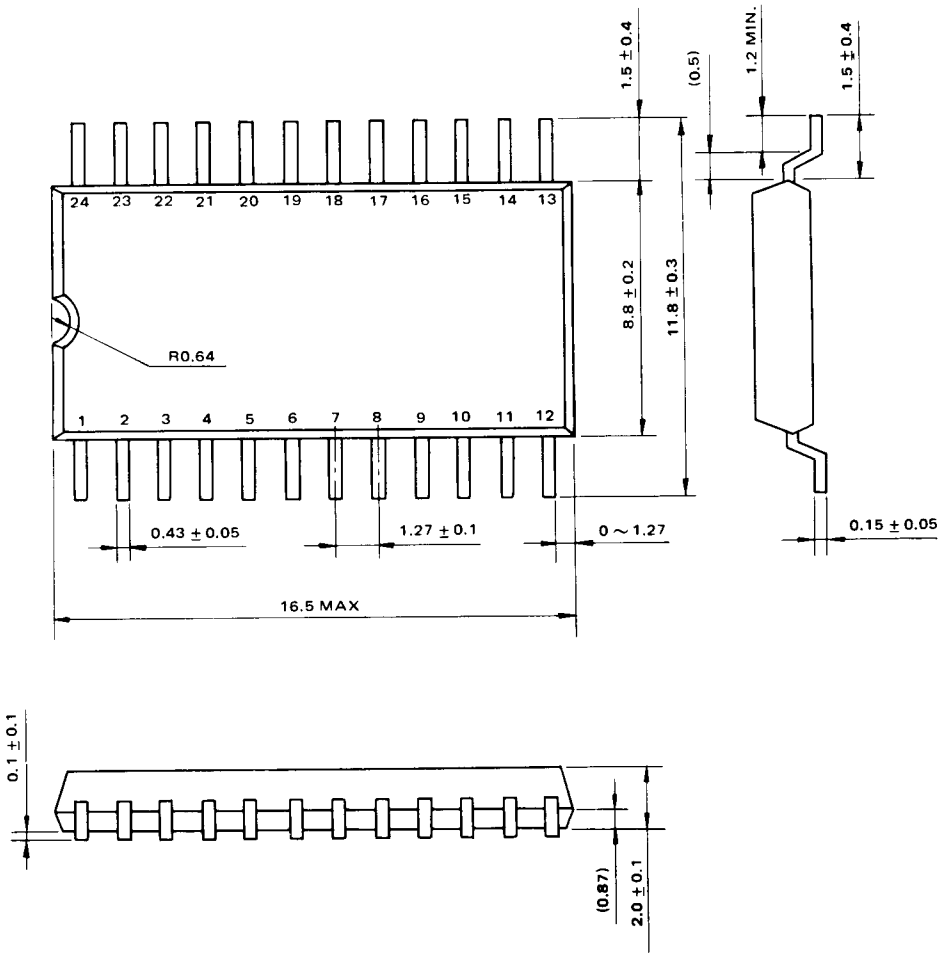
OUTLINE DRAWINGS

- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

- **Plastic FP**



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

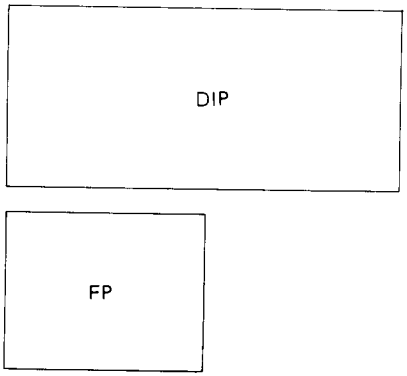
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2. Comparison in occupied space.



3. Advantage of this package

- Small dimensions
- Capability of High Density Assembly
- Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example